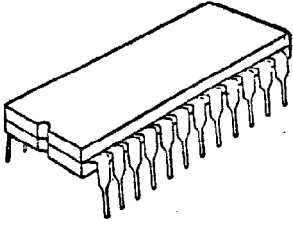


|                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>BRITISH STANDARDS INSTITUTION<br/>2, Park Street, London W1A 2BS</p>                                                                                                                                                                                          | <p>BS CECC 90105 - 018</p> <p>Issue 1</p> <p>September 1984</p> <p>Page 1 of 28</p>                                                                                                                                                                             |
| <p>Specification available from :- As Shown in PD9002,<br/>and CECC 00 200 and<br/>NATIONAL SEMICONDUCTOR (UK) Ltd.<br/>Larkfield Industrial Estate,<br/>Greenock, Scotland</p>                                                                                  | <p>MANUFACTURER'S<br/>TYPE NUMBER</p> <p>DM77S191</p>                                                                                                                                                                                                           |
| <p>ELECTRONIC COMPONENTS OF ASSESSED QUALITY<br/>DETAIL SPECIFICATION IN ACCORDANCE WITH<br/>GS: BS CECC 90000 Issue 2<br/>SS: BS CECC 90100 Issue 2</p>                                                                                                         | <p>For Ordering Information<br/>see clause 5</p>                                                                                                                                                                                                                |
| <p>Outline NOT TO SCALE Isometric projection<br/>For dimensions see IEC 191-2 ( A51E )</p>  <p>Terminal connections: See figure 1<br/>For Marking Information See clause 3</p> | <p>2048 X 8 BIT SCHOTTKY TTL<br/>FUSIBLE LINK PROGRAMMABLE<br/>READ-ONLY MEMORY WITH<br/>THREE STATE OUTPUTS</p> <p>TYPICAL CONSTRUCTION:<br/>SILICON MONOLITHIC<br/>INTEGRATED CIRCUIT,<br/>DUAL-IN-LINE CAVITY<br/>PACKAGE</p> <p>ASSESSMENT LEVEL:<br/>R</p> |

## 1. Functional Description

The DM77S191 is an 16384 bit programmable read-only memory (PROM) organised as 2048, 8 bit words. It features SCHOTTKY clamping for high speed, advanced titanium-tungsten (Ti-W) fuse links, low current PNP inputs to reduce loading, and Three-state outputs. The DM77S191 is TTL compatible.

The address inputs are decoded on-chip. Three Enable inputs are provided to control the output states. When  $\overline{E1}$  is LOW and E2 and E3 are HIGH, the outputs presents the contents of the addressed word. For all other combinations of  $\overline{E1}$  E2 and E3 the output will be in the high impedance state.

In the unprogrammed condition a logic LOW level will be produced at the output.

Refer to Qualified Product List PD 9002 and CECC 00200 for details of manufacturers approved to this specification.

# 1.1 Terminal Function

Refer to para. 1.3.1

## 1.2 Functional Table, Block Diagram and Timing Diagram

### 1.2.1 Functional Table - Not applicable

### 1.2.2 Timing Diagram (Read Mode)

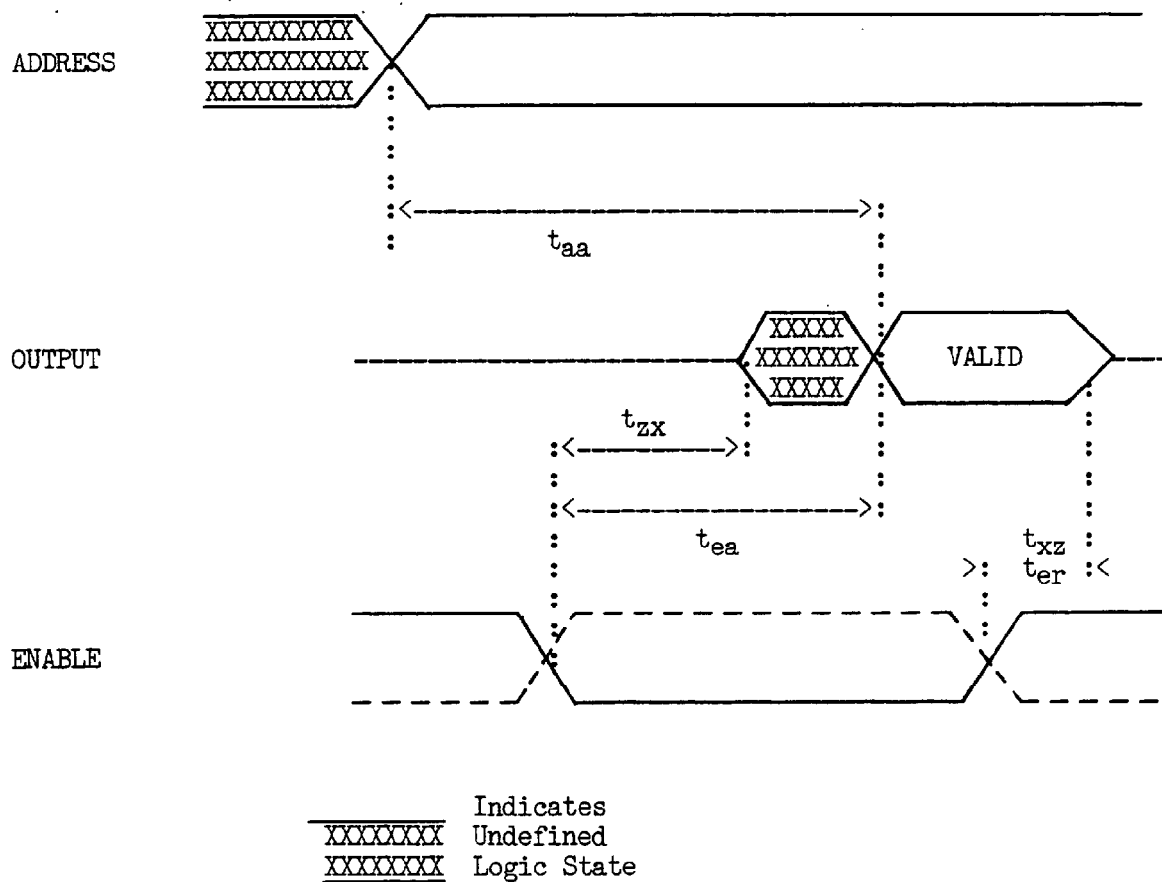


FIG. 1

### 1.2.3 Block Diagram

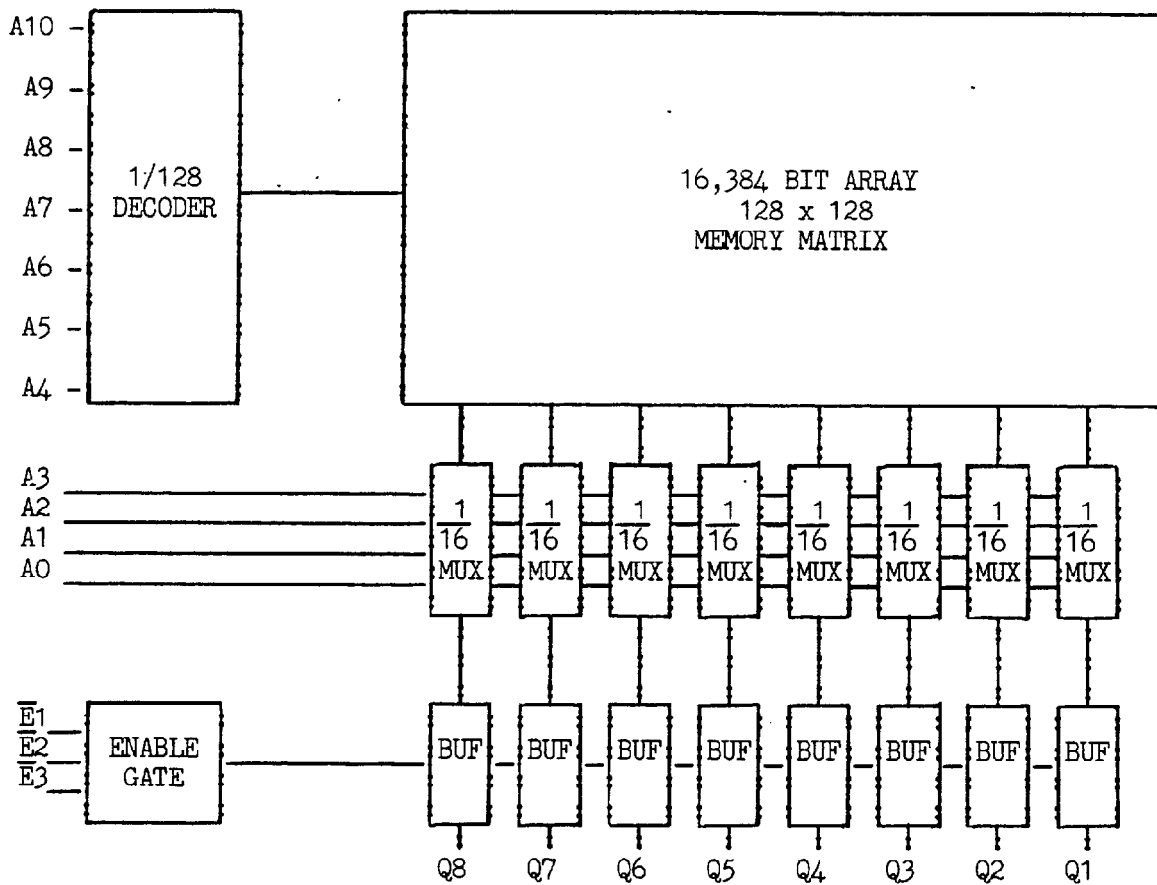
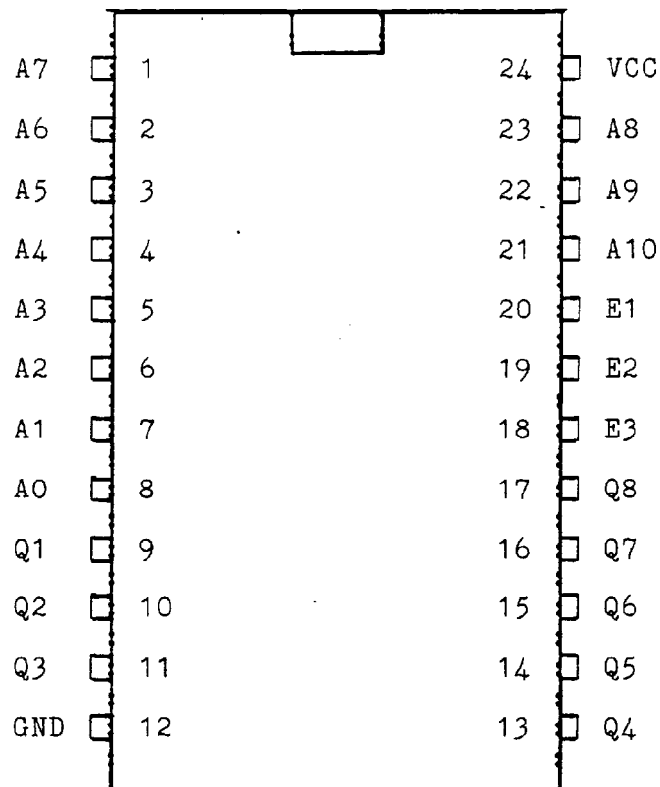


FIG. 2

### 1.3 Terminal Identification, Type Designation, and Marking.

#### 1.3.1 Terminal Identification (top view) and pin definitions.



| <u>Pin</u> | <u>Name</u> | <u>Function</u> |
|------------|-------------|-----------------|
| A0         | to A10      | Address Inputs  |
| Q1         | to Q8       | Data Outputs    |
| E1,        | E2 and E3   | Enable Inputs   |

FIG. 3

#### 1.3.2 Type Designation

DM77S191J

16K-Bit (2048 X 8) Schottky TTL Fusible Link PROM with three-state outputs.

### 1.3.3 Marking

Each Integrated Circuit shall bear the following marking:

- a. Terminal Identification
- b. Type Number
- c. Factory Identification Code
- d. Date Code
- e. Screening Class
- f. Assessment Level

### 1.4 Ordering Information

1. Manufacturer's Part Number
2. Required Quality Assessment Level
3. Required Screening Class ( see addendum 1 to BSCECC 90000 )
4. Relevant DS Number, Issue and Date

## 2. LIMITING CONDITIONS OF USE (not for inspection purposes)

### 2.1 READ MODE

| CHARACTERISTIC         | SYMBOL    | MIN   | MAX    | UNIT |
|------------------------|-----------|-------|--------|------|
| Supply Voltage         | $V_{CC}$  | -0.5  | +7.0   | V    |
| Input Voltage          | $V_I$     | -1.2  | +5.5   | V    |
| Output Voltage appl.   | $V_O$     | -0.5  | +5.5   | V    |
| Max. Power Dissipation | $P_{tot}$ |       | 1.0    | W    |
| Operating Temperature  | $T_{amb}$ | -55.0 | +125.0 | °C   |
| Storage Temperature    | $T_{stg}$ | -65.0 | +150.0 | °C   |

### 2.2 PROGRAMMING MODE

| CHARACTERISTIC         | SYMBOL    | MIN   | MAX   | UNIT |
|------------------------|-----------|-------|-------|------|
| Supply Voltage         | $V_{CCP}$ | 10.0  | 11.0  | V    |
| Input Voltage          | $V_I$     | 0     | +5.5  | V    |
| Output Voltage appl.   | $V_O$     | 10.0  | 11.0  | V    |
| Max. Power Dissipation | $P_{tot}$ |       | 1.0   | W    |
| Operating Temperature  | $T_{amb}$ | +15.0 | +30.0 | °C   |

### 3. RECOMMENDED OPERATING CONDITIONS, PROGRAMMING CHARACTERISTICS AND ASSOCIATED CHARACTERISTICS. (not for inspection purposes)

#### 3.1 Recommended Operating Conditions

The following conditions and characteristics apply over the operating temperature range and supply voltage range specified.

For programming conditions see clause 3.2. For read conditions see clause 3.3.

#### 3.2 Programming Mode.

##### 3.2.1 Programming Conditions and Characteristics.

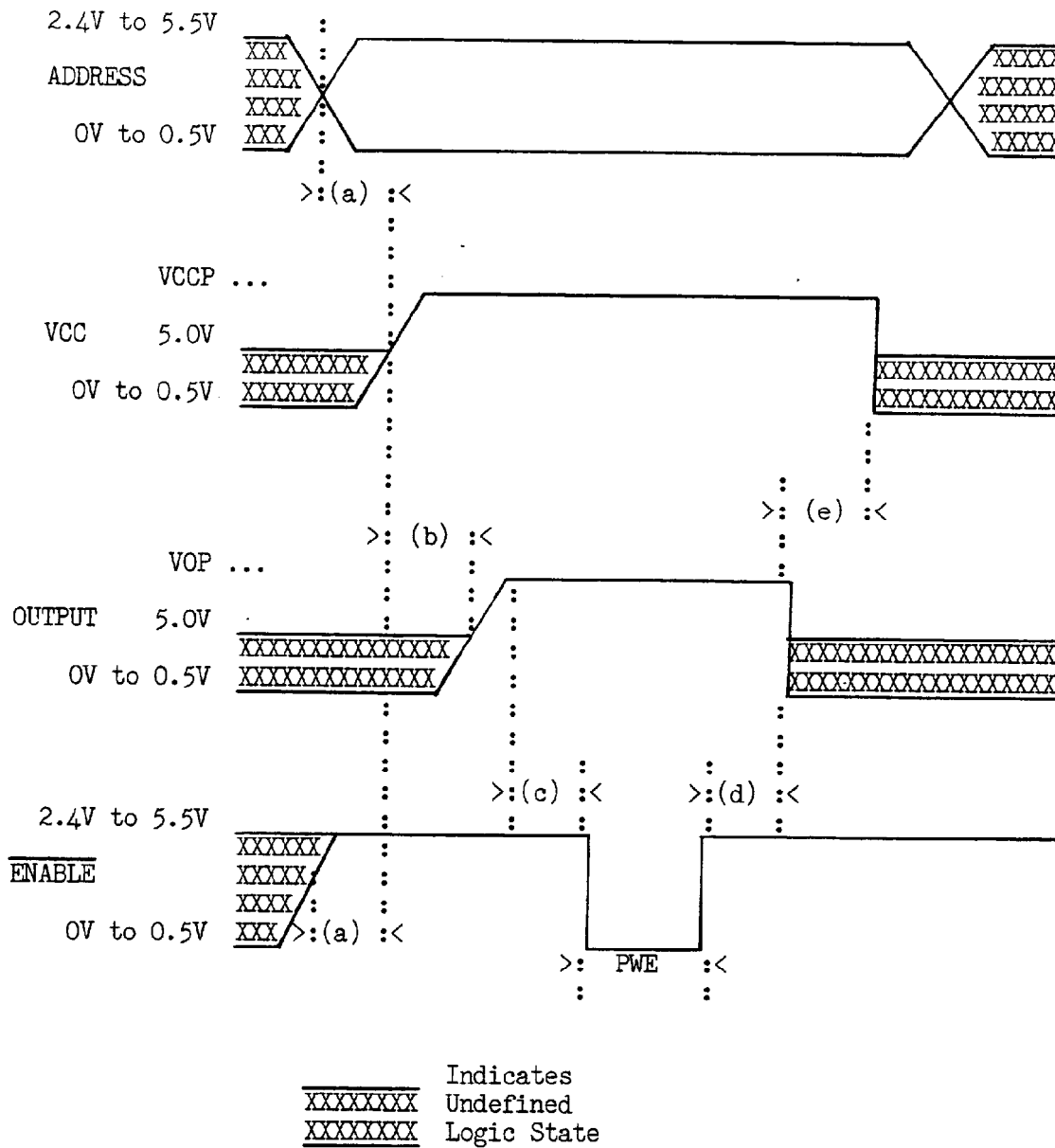
| CHARACTERISTIC                         | CONDITIONS                    | SYMBOL     | MIN  | MAX    | UNIT        |
|----------------------------------------|-------------------------------|------------|------|--------|-------------|
| Operating Temperature                  |                               | $T_{amb}$  | 15.0 | 30.0   | $^{\circ}C$ |
| Power Supply Voltage to Program        |                               | $V_{CCP}$  | 10.0 | 11.0   | V           |
| Power Supply Voltage to Verify         |                               | $V_{CCV}$  | 3.8  | 4.2    | V           |
| Programming Supply Current             | $V_{CCP} = 10.0V$<br>to 11.0V | $I_{CCP}$  | 600  | 750    | mA          |
| Input High Voltage                     |                               | $V_{IH}$   | 2.0  | 5.5    | V           |
| Input Low Voltage                      |                               | $V_{IL}$   | 0    | 0.8    | V           |
| Input High Current                     | $V_{IH} = 2.7V$               | $I_{IH}$   |      | 25.0   | $\mu A$     |
| Input Low Current                      | $V_{IL} = 0.45$               | $I_{IL}$   |      | -250.0 | $\mu A$     |
| Forced Output Voltage                  |                               | $V_{CCP}$  | 10.0 | 11.0   | V           |
| Programming Output Current             |                               | $I_{OPF}$  |      | 20.0   | mA          |
| CE Input High Voltage                  |                               | $V_{IHCE}$ |      | 5.5    | V           |
| CE Input Low Voltage                   |                               | $V_{ILCE}$ | 0.0  |        | V           |
| Applied Output Voltage Pulse Slew Rate |                               | $t_{sr}$   | 1.0  | 10.0   | V/ $\mu s$  |
| CE Programming Pulse Width             |                               | $t_p$      | 9.0  | 11.0   | $\mu s$     |

## 3.1.1. cont.

| CHARACTERISTIC                                                          | CONDITIONS | SYMBOL         | MIN  | MAX  | UNIT |
|-------------------------------------------------------------------------|------------|----------------|------|------|------|
| Pulse Sequence Delay                                                    |            | $t_d$          | 33.0 |      | us   |
| Duty Cycle for $V_{cc}$<br>at $V_{ccp}$                                 |            |                |      | 25.0 | %    |
| Max. fusing attempts<br>per link to achieve<br>the min. yield           |            | $F_L$          |      | 5    |      |
| Minimum Programming<br>Yield                                            |            | $P_y$          | 85   |      | %    |
| Set-Up time of<br>Address                                               |            | $t_{sadd}$     | 100  |      | ns   |
| Set-Up time of<br>Program $V_{cc}$                                      |            | $t_{sV_{ccp}}$ | 5 *  |      | ns   |
| Set-Up time of<br>Output voltage                                        |            | $t_{sV_{op}}$  | 100  |      | ns   |
| Hold time of<br>Output voltage                                          |            | $t_{hV_{op}}$  | 100  |      | ns   |
| Hold time of<br>Program $V_{cc}$                                        |            | $t_{hV_{ccp}}$ | 100  |      |      |
| Total Programming<br>time for each location:<br>(Excluding Verify time) |            |                | 65   |      | us   |

\* May be >0 if  $V_{ccp}$  rises at the same rate or faster than  $V_{op}$

### 3.2.2 Programming Waveforms



- (a)  $t_{sadd}$  Set-up time of address before program  $V_{CC}$  set.  
 (b)  $t_{sVccp}$  Set-up time of program  $V_{CC}$  before output program voltage set.  
 (c)  $t_{sVop}$  Set-up time of output voltage before program pulse.  
 (d)  $t_{hVop}$  Hold time of output after program pulse.  
 (e)  $t_{hVccp}$  Hold time of program  $V_{CC}$  after output program voltage removed.

FIG. 4