

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC



Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION PARTICULIERE CADRE:

**MEMOIRES BIPOLAIRES
A LECTURE SEULE
PROGRAMMABLES PAR FUSION, A
CIRCUIT INTEGRE MONOLITHIQUE
AU SILICIUM**

Harmonized System of Quality Assessment for
Electronic Components

BLANK DETAIL SPECIFICATION:

**FUSIBLE LINK PROGRAMMABLE
BIPOLAR
READ ONLY MEMORIES, SILICON
MONOLITHIC INTEGRATED
CIRCUITS**

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

VORDRUCK FÜR
BAUARTSPEZIFIKATION:

**PROGRAMMIERBARE BIPOLARE
SILIZIUM-FESTWERTSPEICHER
MONOLITHISCHE INTEGRIERTE
SCHALTUNGEN**

2

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Cette page bleue doit être insérée après la page de garde de la CECC 90 105 Edition 2 (1986) AMENDEMENT 2 A LA CECC 90 105 (Edition 2) SPECIFICATION PARTICULIERE CADRE MEMOIRES BIPOLAIRES A LECTURE SEULE PROGRAMMABLES PAR FUSION, A CIRCUIT INTEGRE MONOLITHIQUE AU SILICIUM La modification suivante doit être effectuée: Le paragraphe 9 concernant les exigences de contrôle doit être réécrit car les séquences d'essais sont introduites dans la Spécification Générique CECC 90 000. Remplacer les pages 13/14, 15/16 et 17/18 par les nouvelles pages 13/14, 15/16 et 17/18 ci-jointes; et supprimer les pages 19 à 26. Enregistrer cette modification sur la feuille jaune "Enregistrement des amendements". Le texte de cet amendement a été soumis au vote du CECC dans les documents indiqués ci-dessous et a été ratifié par le Président du CECC pour être publié.	This blue page shall be inserted after the title page of CECC 90 105 Issue 2 (1986) AMENDMENT 2 TO CECC 90 105 (Issue 2) BLANK DETAIL SPECIFICATION FUSIBLE LINK PROGRAMMABLE BIPOLAR READ ONLY MEMORIES, SILICON MONOLITHIC INTEGRATED CIRCUITS The following amendment shall be made: Paragraph 9 related to inspection requirements has to be reworded because the test sequences are now introduced in the Generic Specification CECC 90 000. Replace pages 13/14, 15/16 and 17/18 by new pages 13/14, 15/16 and 17/18; and delete pages 19 to 26. Enter this amendment on the yellow "Record of amendments" sheet. This amendment was circulated to the CECC for voting in the documents listed below and was ratified by the president of the CECC for publication.	Dieses blaue Blatt ist nach dem Titelblatt der CECC 90 105 Ausgabe 2 (1986) einzufügen ÄNDERUNG 2 ZU CECC 90 105 (Ausgabe 2) VORDRUCK FÜR BAUARTSPEZIFIKATION PROGRAMMIERBARE BIPOLARE SILIZIUM-FESTWERTSPEICHER, MONOLITHISCHE INTEGRIERTE SCHALTUNGEN EIN DEUTSCHER TEXT LIEGT NICHT VOR
CECC(Secretariat)2980 Février 1992 CECC(Secretariat)3039	Document Date of voting Report on the voting CECC(Secretariat)2980 February 1992 CECC(Secretariat)3039	CECC 90 105 Issue 2 Amendment 2 1993 CECC 90 105 Ausgabe 2 Änderung 2 1993

KEIN DEUTSCHER

TEXT

This blue page shall be inserted after the title page of CECC 90 105 Issue 2 (1986)

AMENDMENT 1 TO CECC 90 105 (Issue 2):
BLANK DETAIL SPECIFICATION:
FUSIBLE LINK PROGRAMMABLE BIPOLAR READ ONLY MEMORIES, SILICON MONOLITHIC INTEGRATED CIRCUITS

The following amendment shall be made:
Remove page 1 and
insert new page 1
where the EFFECTIVE DATE has been added.

Enter this amendment on the yellow "Record of amendments" sheet.

Cette page bleue doit être insérée après la page de garde de la CECC 90 105 Edition 2 (1986)

MODIFICATION 1 A LA CECC 90 105 (Edition 2):
SPECIFICATION PARTICULIERE CADRE:
MEMOIRES BIPOLAIRES A LECTURE SEULE PROGRAMMABLES PAR FUSION, A CIRCUIT INTEGRE MONOLITHIQUE AU SILICIUM

La modification suivante doit être effectuée:
Supprimer page 1 et
insérer la nouvelle page 1
où la DATE D'EFFET a été ajoutée.

Enregistrer la modification sur la feuille jaune "Enregistrement de modifications".

CECC 90 105 Issue 2 Amendment 1 1987

CECC 90 105 Edition 2 Modification 1 1987

Information about the System may be obtained from:



FEN Secretariat
and
CECC General Secretariat
Stresemannallee 15
D-6000 Frankfurt/Main 70
Telefon: (069) 630 82 83
Telex 4-12871 vdetz d

or from the National Authorized Institutions
of the participating countries listed
who can supply copies of:

- 1 The Internal Regulations of the FEN e.V.
- 2 CECC Specifications of the FEN and National Specifications for the System
- 3 CECC 00 200: Qualified Products List (QPL)
(biannual issues January and July,
with three-monthly amendments)
- 4 CECC 00 300: CECC Publications and their
related national documents (biannual issues
June and December, with three-monthly
amendments)

Austria

Österreichischer Verband
für Elektrotechnik
1, Eschenbachgasse 9
A-1010 Vienna

Belgium

Comité Electrotechnique Belge
Galerie Ravenstein 3
Boîte 11
B-1000 Brussels

Denmark

Dansk Elektroteknisk Komite
Strandgade 36
DK-1401 Copenhagen K

Finland

Finnish Electrotechnical
Standards Association
P.O. Box 134
SF-00211 Helsinki 21

France

Union Technique de l'Electricité
Participation française au CECC
12, Place des Etats-Unis
F-75783 Paris Cedex 16

Germany

Deutsche Elektrotechnische
Kommission im DIN und VDE
Stresemannallee 15
D-6000 Frankfurt/Main 70

Ireland

Institute for Industrial Research
and Standards
Ballymun Road
IRL-Dublin 9

Italy

Comitato Elettrotecnico Italiano
Viale Monza 259
I-20126 Milan

Netherlands

Nederlands Elektrotechnisch Comité
Kalfjeslaan 2
Postbus 5059
NL-2600 GB Delft

Norway

Norsk Elektroteknisk Komite
Postboks 7099
Homansbyen
N-0306 Oslo 3

Portugal

Comissão Electrotécnica Portuguesa
Ministério da Indústria e Tecnologia
Direcção-Geral de Qualidade
Rua Infancia 16 41-2º.
P-1200 Lisbon

Spain

Asociación Electrotécnica y Electrónica Española
Comité Español del CECC
Avda. de Brasil, 7
E-28020 Madrid 20

Sweden

Svenska Elektriska Kommissionen
Box 1284
S-163 14 Spånga-Stockholm

Switzerland

Schweizerischer Elektrotechnischer
Verein
Postfach
CH-8034 Zürich

United Kingdom

British Electrotechnical Committee
British Standards Institution
2 Park Street
GB-London W1A 2BS

FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for FUSIBLE LINK PROGRAMMABLE BIPOLAR READ ONLY MEMORIES SILICON MONOLITHIC INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly-sheet.

PREFACE

This blank detail specification (BDS) was prepared by CECC WG9 "Integrated circuits".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

The text of this second issue consists of the text of CECC 90 105 Issue 1 (1983) amended in accordance with the ratified new material introduced by the following documents :

<u>Documents</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat) 1685	February 1985	CECC(Secretariat) 1850

It is recognized that the layout proposed cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

In accordance with the decision of the CECC Management Committee this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

EFFECTIVE DATE

This second issue of CECC 90 105 shall become effective for all new qualification approvals on 1 January 1987. Issue 1 will continue to remain effective for all past approvals.

GENERAL

The following information is given for guidance.

Scope

This BDS relates to Fusible Link Programmable Bipolar Read Only memories in accordance with IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

Related documents

See 2.1 of CECC 90 100 and 2.2 of CECC 90 000

Structure of Detail Specifications

Clause numbering of DS shall be in accordance with that of this document.

Units, symbols and terminology

See 2.3 of CECC 90 100 and 2.3 of CECC 90 000

Application of Quality Assessment Procedures

See 3 of CECC 90 100 and CECC 90 000.

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FRONT PAGE

The front page of the DS shall be laid out as shown on the previous page.

The numbers between square brackets correspond to the following indications which shall be given :

- Identification of the DS and of the component :

- [1] The name of the National Standards Organization under whose authority the DS is published and, if applicable, the organization from whom the DS is available.
- [2] The CECC Symbol and the CECC number allotted to the DS by the CECC General Secretariat.
- [3] The number and issue number of the CECC generic or sectional specification as relevant ; also national reference if different.
- [4] If different from the CECC number, the national number of the DS, date of issue and any further information required by the national system, together with any amendment numbers.
- [5] Type number, a short description of the type by :
 - function
 - performance, for example variants based on speed, temperature, power etc.

[6] Information on typical construction

- material and type of construction (silicon, monolithic, bipolar, MOS)

For [5] and [6] the text to be given in the DS should be suitable for an entry in CECC 00 200 (QPL) and CECC 00 300 (Library List).

- [7] An outline drawing with main dimensions which are of importance for interchangeability, and/or reference to the appropriate national or international document for outlines. Alternatively, this drawing may be given in an annex to the DS.

[8] Quality assessment level(s)

- [9] Reference data giving information on the most important properties of the component, which allow comparison between the various component types intended for the same, or for similar, applications.

The DS shall give a brief description including the following :

- Structure (words x bits)
- The type of output circuit (for example three state)
- Essential functions

The memories which are described in this BDS are read only and not re-programmable. The logic state of the internal cells is defined by the presence or the absence of link fusion of the related cell.

- Identification of the component and supplementary information :

Description of the materials for the package (for example, glass, ceramic, metal, plastic) and information relating to the mounting (welding, soldering), lead material and finish.

Inside the sketch of the package, the terminal connections to the inputs, outputs or other important points of the circuit shall be identified. This can be shown by a functional block diagram.

Description of the numbering of the terminals with the identification of pin number 1.

Marking on the device in accordance with the GS (see 2.5 of CECC 90 000).

2 OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range unless otherwise specified.

2.1 General description

The following characteristics shall be given if they are not adequately defined in clause 1 :

- Nominal voltage supply level.
- Nominal current consumption.
- Standby current consumption.
- Fuse technology.
- Possible particular operating modes.
- Electrical compatibility (if appropriate) : it shall be stated whether the integrated circuit memory is electrically compatible with other particular integrated circuits or families of integrated circuits, or whether special interfaces are required.
- Block diagram : the block diagram shall be sufficiently detailed to enable the individual functional units within the memory to be identified with their main input and output paths and the identification of their external connections (chip enable, address decode ...).
- The function(s) performed by each terminal.
- The IEC 617-12 symbolic representation shall be given if it exists.
- The programming conditions are described in the annex of the DS.

2.2 Detailed Functional Specification

2.2.1 Function description

This paragraph defines the following characteristics

- memory size : the total number of bits of information capable of being stored in the memory circuit
- memory organisation : the number of bits per word capable of being stored in the memory circuit
- addressing mode (for example multiplexed, latched, etc.)
- chip select (*)
- output enable (*)
- standby mode
- truth table (this table will show the output states versus the different combinations between the address inputs and the select inputs)

The product is designed to be electrically programmed.

The programming operation consists of :

- . opening by fusion the metal link
- or . fusing of junction

This causes the change from the initial logic state to the programmed logic state.

(*) The chip select and the output enable shall be distinguished.

The initial logic state of the whole memory must be specified.

It is possible to modify further the memory content on unprogrammed cells. The normal functioning of the memory does not change its content. The programming conditions are defined in the paragraph 2.2.2.

2.2.2 Programming (writing of a content)

The programming operation consists of :

- . opening by fusion the metal link
- or . fusing of junction

This causes the change from the initial logic state to the programmed logic state. This procedure is irreversible : once altered, the output for that bit location is permanently programmed.

Programming methods and conditions are described by the DS.

It is possible to modify further the memory content on unprogrammed cells. The normal functioning of the memory does not change its content.

The programming parameters specific of each considered device are described in associated annex. In this one the parameters may be shown as organigrams or programming sequences. The different signal configurations and logic levels needed for programming shall be described.

2.2.3 Functional Interchangeability

All products described in the same DS are interchangeable after programming. Different products may be programmed under different methods. Each of these shall be described in an annex to the DS.

2.3 Limiting conditions of use (ratings)

Limiting conditions (ratings) are not for inspection purposes.

Values of limiting conditions of use shall be given as follows :

Any cautionary statement unique to an individual integrated circuit shall be included, for example :

- any difference between the limiting conditions applicable to the programming and read operations shall be given.

Any interdependence of limiting conditions shall be specified.

If externally connected elements have an influence on the values of the ratings, the ratings shall be prescribed for the integrated circuit with the elements connected for example heatsinks.

If transient overloads are permitted, their magnitude and durations shall be specified.

Where minimum and maximum values differ during programming this should be stated.

All voltages are referenced to a reference terminal (GND, etc.).

Characteristics	Symbol	min.	max.	Unit
Supply voltage range	V_{CC}			V
Input voltages	V_I			V
Output voltages	V_O			V
Off-state voltage (Note 1)	V_{OZ}			V
Output currents	I_O			mA
Input currents	I_I			mA
Max. power-dissipation (Note 1)	P_D max.	n.a.		W
Operating temperature	T_{amb} and/or T_{case}			°C
Storage temperature	T_{stg}			°C

Note 1) : Where appropriate.

Note 2) : The values given in this Table are not related to programming conditions.

2.4 Recommended conditions of use and associated characteristics (In accordance with 5.3.8 of CECC 90 100)

Not for inspection purpose.

The characteristics shall apply over the full operating temperature range, unless otherwise specified. Where the stated performance of the circuit varies over the operating temperature range, the values of the input and output voltages and their associated currents shall be stated at 25 °C and at the extremes of the operating temperature range. Values of current and voltage shall be given for each functionally different type of input and/or output.

Special characteristics and timing requirements shall be specified.

2.4.1 Recommended conditions of use

All voltages are referenced to a reference terminal (GND, etc.).

Characteristics	Conditions	Symbols	min.	max.	Unit
Supply voltage		V_{CC} (Note 1)			V
Low level input voltage		V_{IL}			V
High level input voltage		V_{IH}			V
Operating temperature		T_{amb} and/or T_{case}			°C

Note 1) : Where appropriate these values should also be quoted under standby conditions.

2.4.2 Associated characteristics (if applicable)

2.5 Static characteristics

All voltages are referenced to a reference terminal (GND etc.)

Characteristics	Conditions (Note 4)	Symbols	min.*	max.*	Unit
Maximum supply current(s) (Note 1)	V_{CC} max.	I_{CC}			mA
High level input voltage	V_{CC}	V_{IH}			V
Low level input voltage	V_{CC}	V_{IL}			V
High level output voltage	V_{CC} I_{OHA}	V_{OH}			V
Low level output voltage	V_{CC} I_{OLA}	V_{OL}			V
High level input or leakage current	V_{CC} V_{IHB}	I_{IH}			μA
Low level input or leakage current	V_{CC} V_{ILA}	$I_{IL}(1)$			μA
Low level input or leakage current	V_{CC} V_{ILB}	$I_{IL}(2)$			μA
High level output current	V_{CC} V_{OHB}	I_{OH}			μA
Low level output current	V_{CC} V_{OLA}	I_{OL}			mA
High level output current (leakage) (Note 2)	V_{CC} V_{OHA}	I_{OHX}			μA
Low level output current (leakage) (Note 2)	V_{CC} V_{OLB}	I_{OLX}			μA
High level output leakage current at three-state outputs (if applicable)	V_{CC} V_{OHB}	I_{OHZ}			μA

* algebraic values

Characteristics	Conditions (Note 4)	Symbol	min. *	max. *	Unit
Low level output leakage current at three-state outputs (if applicable)	V_{CC} V_{OLA}	I_{OLZ}			μA
Output short circuit current (Note 3)	V_{CC} $V_O = 0$	I_{OS}			mA

* algebraic values

Note 1) : Where appropriate.

Note 2) : I_{OHX} and I_{OLX} apply only to circuits having open-collector (or open source/drain) outputs and in this case replace I_{OH} and I_{OL} .

Note 3) : Duration to be specified

Note 4) : The supply voltages shall be specified to ensure the worst case for the relevant characteristic measurement.

The following shall also be stated where applicable :

- where certain terminals may function as inputs or as outputs, then information shall be given for both these conditions

2.6 Dynamic characteristics

Characteristics	Conditions	Symbol	min.	max.	Unit
ADDRESS ACCESS TIME		$t_a(A)$	-		ns
CHIP ENABLE ACCESS TIME	(Note 1)	$t_a(S)$	-		ns
CHIP DISABLE		$t_{dis}(S)$	-		ns

Note 1) : Test conditions as in Sub-Group A5 of Inspection Requirements.

2.7 Timing diagram

Timing diagrams shall be given, to comprise a complete set of signals which show the operation to each mode of the circuit. Any time intervals which need to be known by the user to ensure the correct operation of the memory should be stated, for example, operation during and after leaving the standby condition.

2.8 Capacitances

Characteristics	Conditions	Symbol	min.	max.	Unit
Input capacitance	-	C_{in}			pF
Output capacitance (if applicable)	-	C_{out}			pF

2.9 Additional information

- Mass
- Thermal resistance
- Burn-in conditions (where appropriate) the following shall be specified :
 - . Ambient temperature : maximum operating temperature
 - . Supply voltage : nominal value
 - . Frequency : to be specified
 - . Circuit diagram and conditions : to be specified
- Noise immunity (inputs, supply voltages etc.)
- Power supplies

Where appropriate, information shall be given for the typical variation of power supply current(s) (or, as applicable, voltage(s)), over the specified range of control signal frequencies (including pulsed supplies where appropriate).

- Loading rules : information on the output loading capability shall be given
- The electrical schematics of input or output circuits (if necessary)

3 IDENTIFICATION OF THE DEVICE TYPES**3.1 Type identification****3.2 Ordering information**

See 2.6 of CECC 90 000

A statement should be made in the ordering information stating that the device will be supplied unprogrammed or programmed with description or specification of acceptable pattern input media.

3.3 Marking

See 2.5 of CECC 90 000

4 TEST AND MEASUREMENT PROCEDURES**4.1 General conditions**

See 4.1 of CECC 90 100 and 4.1 of CECC 90 000.

4.2 Visual and dimensional examinations

See 4.2 and 4.3 of CECC 90 000.

4.3 General conditions for electrical and functional measurements

See 4.5 of CECC 90 000.

Test program is part of the product specification. The manufacturer shall demonstrate to the ONH that the Functional Test Sequence is adequate referring to the definition given by the manufacturer (function, test coverage, etc.).