

UTE

Spécification française harmonisée
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CECC 90 110-032

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Total number of pages : 25

**ELECTRONIC COMPONENTS OF ASSESSED
QUALITY IN ACCORDANCE WITH :**

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 110 (NF C 86-241)

UTE C 86-241 ADD. 8/M 18

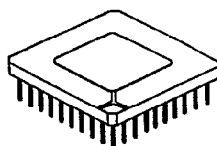
Approved on March 21, 1991

OUTLINE AND DIMENSIONS :

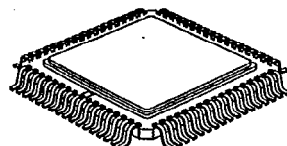
See 2.3.2 and Annex B.

TERMINAL CONNECTIONS :

See 2.3.2.

AVAILABLE CERAMIC PACKAGES :

68 - PGA - UP
Pin Grid Array



68 - QFP
Quad Flat Package

**DETAIL SPECIFICATION FOR
MICROPROCESSOR INTEGRATED CIRCUITS
IN ACCORDANCE WITH CECC 90 110**

68881M-16 68882M-16

68881M-20 68882M-20

68882M-25

32 BIT COPROCESSOR

16,67 MHz, 20 MHz and 25 MHz

Operating temperature range : - 55 °C to + 125 °C

TYPICAL CONSTRUCTION :

Die : Silicon monolithic MOS technology.

Cavity package : ceramic hermetically sealed.

CAUTION :

These are electrostatic sensitive devices.



ASSESSMENT LEVEL : P, Y

TYPE DESCRIPTION

32 bit floating-point coprocessor (FPCP).

Full implementation of the IEEE Standard for Binary Floating-point Arithmetic.

Information about manufacturers who have components qualified to this detail specification is available in the current
CECC 00 200 : Qualified Products List.

**Documents**

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DETAIL SPECIFICATION FOR CECC 32 BIT COPROCESSORS

TYPES NOS: 68881M AND 68882M

1. Object

This document completes the existing CECC detail specifications listed below (sec 2.1) in order to define the type numbering system and, as appropriate, the specific characteristics and requirements, applicable to the relevant products when they are produced by another manufacturer within the CECC system.

It should be modified (or deleted) when the original CECC documents will be updated to allow their direct application to these products.

2. Characteristics and requirements.2.1. List of DS and relevant products.

Basic type and Variant of Product	Max. Clock freq. (MHz)	CECC - DS	
		Relevant CECC product and variant	CECC-DS number
68881 M-16	16,67	68881 C-16	CECC 90110/020 issue 2 (1990)
68881 M-20	20,0	68881 C-20	
68882 M-16	16,67	68882 C-16	CECC 90110/024 issue 1 (1989)
68882 M-20	20,0	68882 C-20	
68882 M-25	25,0	no relevant product	

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2.2. Applicable requirements

The identification (DS/clause 3) is defined in clause 3 of this specification.

All other requirements specified in the CECC detail specifications as listed in 2.1 are applicable to the relevant products with the following specific conditions (the references to the GS apply to Generic Specification CECC 90000/Issue 4/1990):

Clause 5 - Structural similarity procedure
Applicable as prescribed in GS/3.2

Clause 6 - Qualification approval procedure
Applicable as prescribed in GS/clause 3

Clause 8 - Screening procedures
Applicable as prescribed in GS/4.10

Clause 9 - Quality conformance inspection.

- . Subgroup B5 is not applicable to the class B products (see GS/3.6 note 11).
- . Subgroup C6 is not applicable to these cavity packages (see GS/3.6 note 14).
- . Transient Energy test is performed for subgroup D2 instead C14.
- . Input capacitances are measured for subgroup D5 instead C15.

2.3. Specific characteristics

2.3.1 Electrical characteristics

The specific characteristics for 68882 M-25 shall be as defined in appendix A of this document for sub-clauses 2.5, 2.7 and for clause 9 (subgroup A5 only).

The other characteristics for this product and the whole of the characteristics for other products shall be as defined in the relevant CECC-DS given in 2.1.

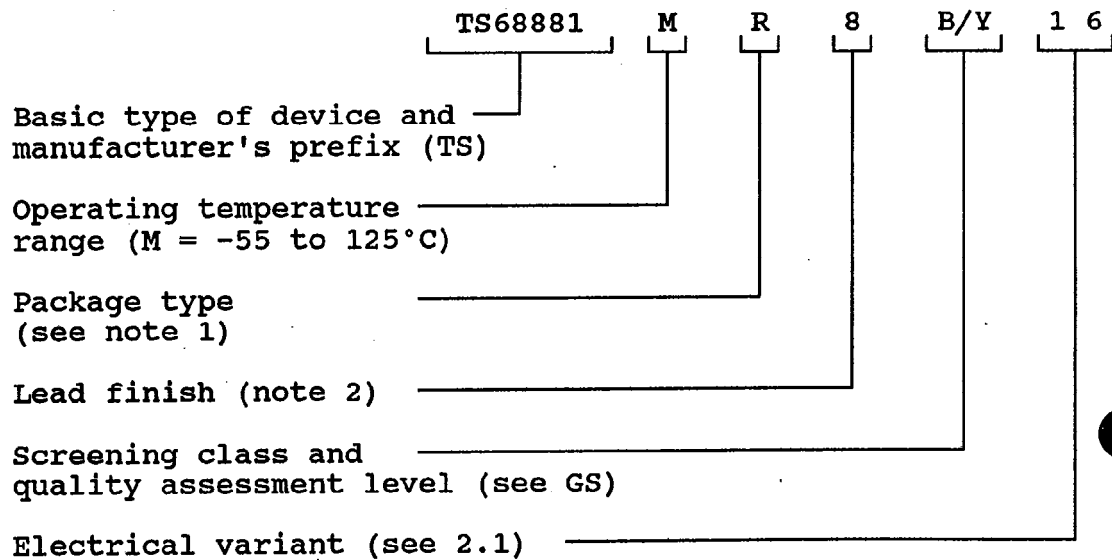
2.3.2 Package characteristics

Referring to the relevant CECC detail Specification listed in 2.1, all the characteristics related to the product packages shall be as follows :

- Pin grid Array package (PGA) : See relevant CECC DS for PGA
- Quad Flat package (CQFP) : See relevant CECC-DS for " Ceramic leaded Chip Carrier" (CLCC) package,excepted for dimensional characteristics : see Appendix B of this document.

3. IDENTIFICATION

3.1 Interpretation of device number



Note 1. Package type (ceramic-metal packages) (see 2.3.2 above)

F = Quad Flat Package (CQFP)

R = Pin Grid Array package (PGA)

Note 2. Lead finish :

7 = Solder dip

8 = Gold

3.2 Marking:

As prescribed in GS/2.5

3.3 Ordering

As prescribed in GS/2.6

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APPENDIX - ASPECIFIC ELECTRICAL CHARACTERISTICS FOR68882M-25

Note 1 In order to facilitate the reading of the product characteristics, the totality of pages 10 to 20 and 27 to 34 from the specification CECC 90110/024 issue 1 are reproduced in this appendix. The specific characteristics for 68882M-25 only appear on pages 10, 13, 14, 27, and 30 to 33.

Note 2 To remain homogeneous, the variant 68882M-25 is pointed out as 68882C-25 in the tables.

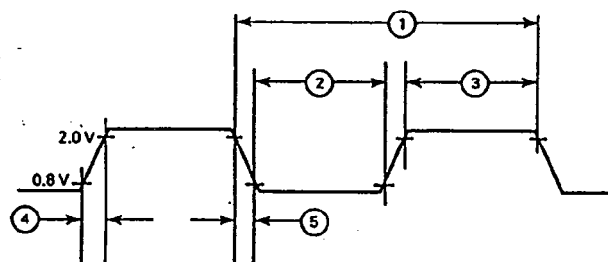
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2.5 RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS (Not for Inspection purposes)

All the characteristics apply over the operating temperature range unless otherwise stated.

TIMING REQUIREMENTS (CLOCK INPUT REQUIREMENTS)

No.	Frequency of Operation	68882 C25		68882 C16		68882 C20		Unit
		t_{in}	t_{2x}	Min	Max	Min	Max	
		12.5	25	8	16.67	12.5	20.0	MHz
1	Cycle Time	40	80	60	125	50	80	ns
2, 3	Clock Pulse Width	15	59	24	95	20	54	ns
4, 5	Rise and Fall Times	—	4	—	5	—	5	ns



NOTE:

Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 4 Clock Input Timing Diagram

2.5.1. RECOMMENDED CONDITIONS OF USE

Supply Voltage 4.5 Volts to 5.5 Volts
Input Voltage 0 Volts to 5.0 Volts
See also Ratings on Page 1.

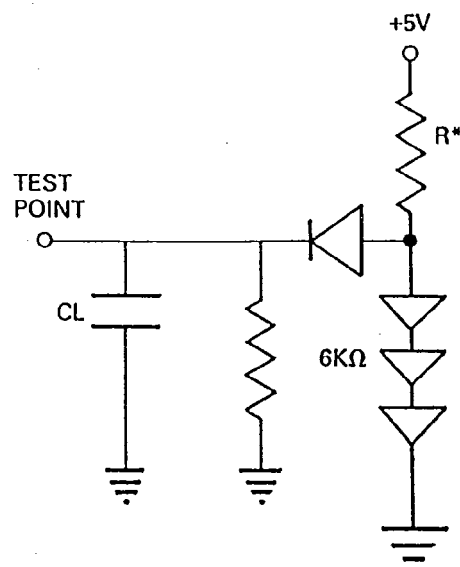
2.6 STATIC ELECTRICAL CHARACTERISTICS

These characteristics apply over the full operating temperature range unless otherwise stated.

VCC = 4.5V to 5.5V

Characteristic	Conditions	Symbol	Min	Max	Units
Maximum Supply Current	VCC = 5.5V CLK = fmax RESET = GND	I _{CC}	–	136	mA
High Level Input Voltage	V _O = 0.5V or 2.4V VCC = 4.5V to 5.5V	V _{IH}	2.0	VCC	V
Low Level Input Voltage	V _O = 0.5V or 2.4V VCC = 4.5V to 5.5V	V _{IL}	–0.5	0.8	V
High Level Output Voltage DSACK0, DSACK1 D0 – D31	I _{OH} = 400µA	V _{OH}	2.4	–	V
Low Level Output Voltage DSACK0, DSACK1 D0-D31	I _{OL} = 5.3 mA Load circuit as Fig. 5 R = 740Ω	V _{OL}	–	0.5	V
Input Leakage Current High and Low State CLK, RESET, R _W A0-A4, CS, DS A5, SIZE	VCC = 5.5V	I _{IN}	–	10	µA
Input Leakage Current High and Low State at 3-state outputs	VCC = 5.5V V _{IN} = 2.4V/0.4V	I _{OZ}	–	20	µA
Low Level Leakage Current at SENSE output	VOL = GND	I _{IL}		500	µA
Output Short-Circuit Current (Any output)	VCC = 5.5V V _O = 0V (Pulsed. Duration 1 mS Duty Cycle 10:1)	I _{OS}	–	200	mA

2.6 continued



CL=130 pF (includes all parasitics)

* Values for R as given in measurement conditions.

FIGURE 5 TEST LOAD

2.7 DYNAMIC ELECTRICAL CHARACTERISTICS (Not for Inspection Purposes)

The limits and values given in this section apply over the full case temperature range -55°C to 125°C and VCC in the range 4.5V to 5.5V VIL=0.5V and VIH=2.4V (See also notes 10 and 11).

The INTERVAL numbers refer to the timing diagrams. See figs 4, 6, 7, 8 and 9.

INTER- VAL No	CHARACTERISTIC	SYMBOL	68882C15		68882C20		68882C25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
2,3	Clock Pulse Width	tCPW	24	95	20	54	15	59	ns	13
6	Address Valid to $\overline{AS}$ Asserted	tAVASL	15	-	10	-	5	-	ns	5, 14
6A	Address Valid to $\overline{DS}$ Asserted (Read)	tAVRDSL	15	-	10	-	5	-	ns	5, 13
6B	Address Valid to $\overline{DS}$ Asserted (Write)	tAVWDSL	50	-	50	-	35	-	ns	5, 13
7	$\overline{AS}$ Negated to Address Invalid	tASHAX	10	-	10	-	5	-	ns	6, 14
7A	$\overline{DS}$ Negated to Address Invalid	tDSHAX	10	-	10	-	5	-	ns	6, 13
8	$\overline{CS}$ Asserted to $\overline{AS}$ Asserted	tCVASL	0	-	0	-	0	-	ns	9, 14
8A	$\overline{CS}$ Asserted to $\overline{DS}$ Asserted (READ)	tCVRDSL	0	-	0	-	0	-	ns	9, 14
8B	$\overline{CS}$ Asserted to $\overline{DS}$ Asserted (WRITE)	tCVWDSL	30	-	25	-	20	-	ns	14
9	$\overline{AS}$ Negated to $\overline{CS}$ Negated	tASHCX	10	-	10	-	5	-	ns	14
9A	$\overline{DS}$ Negated to $\overline{CS}$ Negated	tDSHCX	10	-	10	-	5	-	ns	14
10	$R\overline{W}$ High to $\overline{AS}$ Asserted (Read)	tRVASL	15	-	10	-	5	-	ns	14
10A	$R\overline{W}$ High to $\overline{DS}$ Asserted (Read)	tRVDSL	15	-	10	-	5	-	ns	13
10B	$R\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	tRLSL	35	-	30	-	25	-	ns	13
11	$\overline{AS}$ Negated to $R\overline{W}$ Low (Read) or $\overline{AS}$ Negated to $R\overline{W}$ High (Write)	tASHRX	10	-	10	-	5	-	ns	14
11A	$\overline{DS}$ Negated to $R\overline{W}$ Low (Read) or $\overline{DS}$ Negated to $R\overline{W}$ High (Write)	tDSHRX	10	-	10	-	5	-	ns	13
12	$\overline{DS}$ Width Asserted (Write)	tDSL	40	-	38	-	30	-	ns	10, 13
13	$\overline{DS}$ Width Negated	tDSH	40	-	38	-	30	-	ns	10, 13
13A	$\overline{DS}$ Negated to $\overline{AS}$ Asserted	tDSHASL	30	-	30	-	25	-	ns	4, 10
14	$\overline{CS}$, $\overline{DS}$ Asserted to Data Out Valid (Read)	tDSLDO	-	80	-	45	-	45	ns	2 13

2.7 continued

INTER- VAL No	CHARACTERISTIC	SYMBOL	68882C16		68882C20		68882C25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
15	$\overline{DS}$ Negated to Data-out Invalid (Read)	tDSHDO	0	-	0	-	0	-	ns	13
16	$\overline{DS}$ Negated to Data-Out High Impedance (Read)	tDSHDZ	-	50	-	30	-	30	ns	11
17	Data-In Valid to $\overline{DS}$ Asserted (Write)	tDIDSL	15	-	10	-	5	-	ns	13
18	$\overline{DS}$ Negated to Data-In Invalid (Write)	tDSHDI	15	-	10	-	5	-	ns	13
19	$\overline{START}$ True to $\overline{DSACK0-1}$ Asserted	tSLDAL	-	50	-	35	-	25	ns	2, 8, 13
19A	$\overline{DSACK0}$ Asserted to $\overline{DSACK1}$ Asserted (Skew)	tDADAS	-15	15	-10	10	-10	10	ns	7, 11
20	$\overline{DSACK0}$ or $\overline{DSACK1}$ Asserted to Data-Out Valid	tDALDO	-	50	-	43	-	32	ns	13
21	$\overline{START}$ False to $\overline{DSACK0}$ and $\overline{DSACK1}$ Negated	tSHDAH	-	50	-	30	-	30	ns	8, 13
22	$\overline{START}$ False to $\overline{DSACK0}$ and $\overline{DSACK1}$ High Impedance	tSJDAZ tSJDAZ	- -	70 70	- -	55 40	- -	40 40	ns ns	8 8, 11
23	$\overline{START}$ True to Clock High (synchronous Read)	tDSLCH	0	-	0	-	0	-	ns	3, 8, 13
24	Clock Low to Data-Out Valid (Synchronous Read)	tCLDO	-	105	-	80	-	60	ns	3, 13
25	$\overline{START}$ True to Data-Out Valid (Synchronous Read)	tDSSLDO	0 + 1.5	105 + 2.5	0 + 1.5	80 + 2.5	0 + 1.5	60 + 2.5	ns CLKS	3, 8 14
26	CLOCK Low to $\overline{DSACK0}$ and $\overline{DSACK1}$ Asserted (Synchronous Read)	tCLDAL	-	75	-	55	-	45	ns	3 13
27	$\overline{START}$ True to $\overline{DSACK0}$ and $\overline{DSACK1}$ Asserted (Synchronous Read)	tDSLDA	0 + 1.5	75 + 2.5	0 + 1.5	55 + 2.5	0 + 1.5	45 + 2.5	ns CLKS	3, 8 14
	Frequency of Operation	f	8	16.7	12.5	20	12.5	25	MHz	

2.7 continued

NOTES:

- 1) Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be between 0.8 volts and 2.0 volts.
- 2) These specifications only apply if the FPCP has completed all internal operations initiated by the termination of the previous bus cycle when $\overline{DS}$ was negated.
- 3) Synchronous read cycles occur only when the save or response CIR locations are read.
- 4) This specification only applies to systems in which back-to-back accesses (read-write or write-write) of the operand CIR can occur. When the FPCP is used as a coprocessor to the 68020, this can occur when the addressing mode is immediate.
- 5) If the $\overline{SIZE}$ pin is not strapped to either VCC or GND, it must have the same setup times as do addresses.
- 6) If the $\overline{SIZE}$ pin is not strapped to either VCC or GND, it must have the same hold times as do addresses.
- 7) This number is reduced to 5 nanoseconds if $\overline{DSACK0}$ and $\overline{DSACK1}$ have equal loads.
- 8) $\overline{START}$ is not an external signal; rather, it is the logical condition that indicates the start of an access. The logical equation for this condition is:

$$\overline{START} = \overline{CS} + \overline{AS} + (R/W.\overline{DS})$$
- 9) If a subsequent access is not a FPCP access, $\overline{CS}$ must be negated before the assertion of $\overline{AS}$ and/or $\overline{DS}$ on the non-FPCP access.
- 10) As a minimum, tested initially and after design or process change only.
- 11) Guaranteed by characterisation. Not tested. Provided for system design purposes only.
- 12) $T_c = -55^\circ\text{C}$ and $+130^\circ\text{C}$ in a power off condition under thermal soak for 4 minutes minimum or until thermal equilibrium has been established. Electrical parameters are tested "instant on" 100 milli-sec after power is applied.
- 13) Measured and compared to the specification limit.
- 14) Determined by Go/No-Go (Attribute) testing.

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