

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION PARTICULIERE CADRE:

**MICROPROCESSEURS LOGIQUES
A CIRCUITS INTEGRES**

Harmonized System of Quality Assessment for
Electronic Components

BLANK DETAIL SPECIFICATION:

**DIGITAL MICROPROCESSOR
INTEGRATED CIRCUITS**

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

VORDRUCK FÜR BAUARTSPEZIFIKATION:

**INTEGRIERTE
MIKROPROZESSOR-
SCHALTUNGEN**



2

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Documents



Document Sharing Hub

Information about the System may be obtained from:



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or from the National Authorized Institutions
of the participating countries listed
who can supply copies of:

- 1 The Internal Regulations of the FEN e.V.
- 2 The Rules of Procedure of the System
- 3 CECC Specifications of the FEN and National Specifications for the System
- 4 CECC 00 200: Register of Firms, Products, and Services Approved under the CECC System
- 5 CECC 00 300: Register of National Documents Implementing CECC Publications and CECC European Standards
- 6 CECC 00 301: Register of CECC Specifications and Related Detail Specifications
- 7 Other CECC Publications and publicity documents

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby acceptable in all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for DIGITAL MICROPROCESSOR INTEGRATED CIRCUITS AND ASSOCIATED DIGITAL PERIPHERAL INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification, the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly sheet.

PREFACE

This blank detail specification (BDS) was prepared by CECC WG9: "INTEGRATED CIRCUITS".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747: Semiconductor devices - Discrete devices and integrated circuits and on IEC 748: Semiconductor devices - Integrated circuits.

The text of this second issue consists of the text of CECC 90 110 Issue 1 (1986), amended in accordance with the ratified new material introduced by the following document:

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat)2667	February 1991	CECC(Secretariat)2789

It is recognized that the layout proposed cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

AVIS

In accordance with the decision of the CECC Management Committee, this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

This Issue 2 of CECC 90 110 shall become effective for all new qualification approvals from **15 October 1993**. Issue 1 remains valid for existing qualification approvals.

GENERAL

The following information is given for guidance.

Scope

This BDS relates to:

- digital microprocessors, generally in accordance with IEC 747 and IEC 748 : Semiconductor devices - Discrete devices and integrated circuits
- digital integrated circuits which are primarily designed or intended for use with microprocessors.

Analogue and interface aspects of such devices shall be added to the Detail Specification in accordance with CECC 90 200 and CECC 90 300.

Related documents

See 2.1 of CECC 90 100 and 2.2 of CECC 90 000.

Structure of Detail Specifications

Clause numbering of DS shall be in accordance with that of this document.

Units, symbols and terminology

See 2.3 of CECC 90 100 and 2.3 of CECC 90 000.

Application of Quality Assessment Procedures

See 3 of CECC 90 100 and CECC 90 000.

Layout of front page of detail specification

Specification available from : [1]	CECC 90 110-xxx	
		
	Page 1	Total number of pages :
ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH : [3]		
OUTLINE AND DIMENSIONS [7] TERMINAL CONNECTIONS	DETAIL SPECIFICATION FOR [5]	
	TYPICAL CONSTRUCTION : [6]	
	CAUTION : These are electrostatic sensitive devices.	
	ASSESSMENT LEVEL(S) : [8]	
1 TYPE DESCRIPTION [9]		
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.		

FRONT PAGE

The front page of the DS shall be laid out as shown on the page before.

The numbers between square brackets correspond to the following indications which shall be given:

Identification of the DS and of the component:

- [1] The name of the National Standards Organization under whose authority the DS is published and, if applicable, the organization from whom the DS is available.
- [2] The CECC Symbol and the CECC number allotted to the DS by the CECC General Secretariat.
- [3] The number and issue number of the CECC generic or sectional specification as relevant; also national reference if different.
- [4] If different from the CECC number, the national number of the DS, date of issue and any further information required by the national system, together with any amendment numbers.
- [5] Type number, a short description of the type by:
 - function
 - performance, for example variants based on speed, temperature, power etc.
- [6] Information on typical construction
 - material and type of construction (silicon, monolithic, bipolar, MOS, C MOS, etc.).

For [5] and [6], the text to be given in the DS should be suitable for an entry in CECC 00 200 (QPL) and CECC 00 300 (Library List).

- [7] An outline drawing with main dimensions which are of importance for interchangeability, and/or reference to the appropriate national or international document for outlines. Alternatively, this drawing may be given in an annex to the DS.
- [8] Quality assessment level(s).
- [9] Reference data giving information on the most important properties of the component, which allow comparison between the various component types intended for the same, or for similar, applications.

The DS shall give a brief description including the following:

- technology
- use (if applicable)
- number, type and length of registers (if applicable)
- number, type and width of buses (if applicable)
- word lengths (if applicable)
- addressable memory (if applicable)
- number of terminals
- supply voltage(s)
- any other special feature.

Identification of the component and supplementary information:

Description of the materials for the package (for example, glass, ceramic, metal, plastic) and information relating to the mounting (welding, soldering), lead material and finish.

Inside the sketch of the package, the terminal connections to the inputs, outputs or other important points of the circuit shall be identified. This can be shown by a functional block diagram.

Description of the numbering of the terminals with the identification of pin number 1.

Marking on the device in accordance with the GS (see 2.5 of CECC 90 000).

2 OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range unless otherwise specified.

2.1 General description

The following characteristics shall be given if they are not adequately defined in clause 1.

2.1.1 Internal architecture

Simplified block diagram, with explanatory comments.

2.1.2 Hardware description

- the main features relating to system design and operation shall be given
- clock requirements (if applicable).

2.1.3 Memory organization (if applicable)

Total number of words and total number of bits of the word addressed in each type of memory.

This may be given in the form of a diagram (memory map).

2.1.4 Software main features (if applicable)

2.1.4.1 Addressing modes (if applicable)

List of addressing modes.

2.1.4.2 Arithmetic and logic operations, operations on registers (if applicable)

Number of bits involved in the operation.

2.1.5 Designation of the terminals

The terminals shall be designated in a table as follows:

Symbol	Function	Category

The following categories of terminals apply:

- supply terminals
- input terminals/output terminals
- input/output terminals (bidirectional terminals)
- three state output terminals.

2.2 External components

Characteristics of external components essential to the correct operation of the microprocessor shall be specified (for example clock circuitry).

2.3 Detailed functional specifications

2.3.1 Power supply and initialisation sequences

- power supplies sequencing
- initialisation procedure.

2.3.2 Block diagram

A block diagram shall be given sufficiently detailed to enable the individual functional units which affect its operation to be identified, including any (where appropriate) that are affected by the execution of the microprocessor instructions, and any functional blocks that are user programmable. The main data paths between the functional units, and their connections with external terminals, shall be shown. The identifications of external terminals shall also be shown.

2.3.3 Input and output detailed functions and signals

The function of each input and output signal shall be stated.

The signals may be presented in the following groups:

- DATA signals
- ADDRESS signals
- CONTROL signals (including STATUS).

If necessary explanatory diagrams should be given.

2.3.4 Description of registers (if applicable)

A detailed description including number, types and size in bits, of internal register(s) (program addressable, or otherwise directly affecting the operation of the device) shall be given.

A schematic representation shall also be given for example as follows:

bit n	bit 0	General purpose register(s)
register name		Index and stack pointer register(s)
		Program counter(s) and flag register(s)
		Specific register(s)

2.3.5 Addressing mode(s) (if applicable)

The different possible addressing modes (for example immediate, direct, relative, indexed and indirect) shall be described in detail. Each description shall include a schematic representation of the mechanism of the addressing mode. For more complex modes a table may be necessary.

2.3.6 Instruction set (if applicable)

The instruction format(s) shall be given, for example operation code field, address mode field, register definition field, operand field etc.

A comprehensive list in tabular form of the instructions which may be performed by the microprocessor shall be given. This shall give the instruction code, instruction mnemonic, the operation(s) that result from the execution of the instruction, the number of clock cycles and the number of machines cycles required and, where appropriate, the number of words forming the instruction and the addressing mode(s) associated with each instruction.

Separate tables shall be used for each category of instructions. These categories could be for example :

- transfert instructions
- arithmetic instructions
- logic instructions
- shift and rotate instructions
- branch instructions
- word manipulation instructions
- control instructions.

The bit representation of each instruction shall be given in accordance with the instruction format.

2.3.7 Microprogram (where appropriate)

Microprogram instruction set and method of changing microprogram shall be defined.

2.3.8 External events handling

2.3.8.1 Interrupt handling (where appropriate)

The number, type(s) and priority(ies) of interrupts and their capabilities shall be defined.

2.3.8.2 Input/output handling

The methods of handling the input and output of data including (where applicable) the output of addresses, (for example serial or parallel or a multiplex combination) shall be defined.

2.3.8.3 Timer/counter (where appropriate)

2.4 Limiting conditions of use (ratings)

Limiting conditions (ratings) are not for inspection purposes.

Values of limiting conditions of use shall be given as follows:

Any cautionary statement unique to an individual integrated circuit shall be included, for example the handling of MOS devices.

Any interdependence of limiting conditions shall be specified.

If externally connected elements, for example heatsinks, have an influence on the rating(s), these rating(s) shall be specified for the device with the elements connected.

If transient overloads are permitted their magnitude and duration shall be specified.

For programmable devices (for example those containing EPROM) the limiting condition specific to the programming mode shall be specified.

All voltages are referenced to a reference terminal (V_{SS} , M, etc.).

Characteristics	Symbols	min.	max.	Unit
Supply voltage	$V_{CC}, V_{DD}, V_{BB}, V_{EE}$			V
Input voltages	V_I			V
Output voltages	V_O			V
Off-state voltage (Note)	V_{OZ}			V
Output currents (Note)	I_O			mA
Input current (Note)	I_I			mA
Max. power-dissipation	$P_{Dmax.}$	n.a.		W
Operating temperature	T_{amb} and/or T_{case}			°C
Storage temperature	T_{stg}			°C

Note: Where appropriate.

2.5 Recommended conditions of use and associated characteristics

(In accordance with 5.3.8 of CECC 90 100)

Not for inspection purposes.

The characteristics shall apply over the full operating temperature range, unless otherwise specified. Where the stated performance of the circuit varies over the operating temperature range, the values of the input and output voltages and their associated currents shall be stated at 25 °C and at the extreme of the operating temperature range. Values of current and voltage shall be given for each functionally different type of input and/or output.

Special characteristics and timing requirements shall be specified.

2.5.1 Recommended conditions of use

Characteristics	Conditions	Symbols	min.	max.	Unit
Supply voltage(s)		V_{CC} (Note) V_{DD} (Note) V_{BB} (Note) V_{EE} (Note)		V	V V V V
Low level input voltage		V_{IL}			V
High level input voltage		V_{IH}			V
Operating temperature		T_{amb} and/or T_{case}			°C

Note: Where appropriate, these values should also be quoted under standby conditions.

2.5.2 Associated characteristics (if applicable)

2.6 Static characteristics

All voltages are referenced to a reference terminal (V_{SS} or M, etc.).

Characteristics	Conditions (Notes 1, 2)	Symbols	min.*	max.*	Unit
Maximum supply current(s) (Note 3)	V_{CC} max.	I_{CC} I_{DD} I_{BB} I_{EE} } Where appropriate			mA mA mA mA
High level input voltage	V_{CC}	V_{IH}			V
Low level input voltage	V_{CC}	V_{IL}			V
Input clamping voltage (where appropriate)	V_{CC} I_{IKB}	V_{IK}			V
High level output voltage	V_{CC} I_{OHA}	V_{OH}			V
Low level output voltage	V_{CC} I_{OLA}	V_{OL}			V
High level input or leakage current	V_{CC} V_{IHB}	I_{IH}			μA
Low level input or leakage current	V_{CC} V_{ILA}	$I_{IL(1)}$			μA
Low level input or leakage current	V_{CC} V_{ILB}	$I_{IL(2)}$			μA

* algebraic values

Characteristics	Conditions (Notes 1, 2)	Symbols	min.*	max.*	Unit
High level output current	V_{CC} V_{OHB}	I_{OH}			μA
Low level output current	V_{CC} V_{OLA}	I_{OL}			mA
High level output current (leakage) (Note 4)	V_{CC} V_{OHA}	I_{OHX}			μA
Low level output current (leakage) (Note 4)	V_{CC} V_{OLB}	I_{OLX}			μA
High level output leakage current at three-state outputs (if applicable)	V_{CC} V_{OHB}	I_{OHZ}			μA
Low level output leakage current at three-state outputs (if applicable)	V_{CC} V_{OLA}	I_{OLZ}			μA
Output short circuit current (Note 5)	$V_{CC} = 0$ $V_O = 0$	I_{OS}			mA
Value of output load resistance	-	R_L			Ω
Output loading capacitance	-	C_L			pF
Expander input current (where appropriate)	-	I_{exp}			mA

* algebraic values

Note 1: Where appropriate V_{DD} , V_{BB} or V_{EE} shall be used instead of V_{CC} .

Note 2: The supply voltages shall be specified to insure the worst case for the relevant characteristic measurements.

Note 3: Where appropriate, these values should also be quoted under standby conditions.

Note 4: I_{OHX} and I_{OLX} apply only to circuits having open-collector (or open source/drain) outputs and in this case replace I_{OH} and I_{OL} .

Note 5: Duration to be specified.

The following shall also be stated where applicable:

- where certain terminals may function as inputs or outputs, then information shall be given for both conditions
- current values may be either positive or negative depending on the type of circuit being used
- where clock inputs act as pulsed power supplies, then information shall be given for I_{CC} , I_{SS} etc., as appropriate.