

UTE

Spécification française harmonisée
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CECC 90 111-001

ÉDITION 2
ISSUE 2

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COMPOSANTS ÉLECTRONIQUES SOUS ASSURANCE
DE QUALITÉ CONFORMÉMENT A :

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :

GS : CECC 90 000 (NF C 86-020)
SS : CECC 90 100 (NF C 86-200)
FS : CECC 90 111 (NF C 86-254)

UTE C 86-254 ADD 2/001

Adoptée le 10 octobre 1990

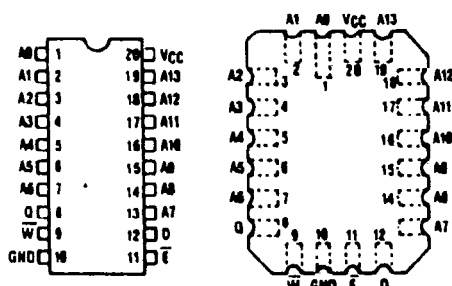
DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 -Types } ●050 G14 - 050 G15
IEC 191-2 -Types } Boîtiers/Packages DC - DP
●Boîtiers PP : voir annexe
Packages PP : see Annex

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Boîtiers DC - DP
DC - DP packages

Boîtier PP
PP package



SPÉCIFICATION PARTICULIÈRE POUR
MÉMOIRES RAM STATIQUES
LECTURE/ÉCRITURE A CIRCUITS INTÉGRÉS

DETAIL SPECIFICATION FOR
MOS READ/WRITE STATIC MEMORIES
SILICON MONOLITHIC CIRCUITS

MODÈLE/TYPE 65 262

●Variétés électriques/Electrical variants

HM 65 262
HM 65 262 B

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique C MOS au silicium.
Silicon monolithic C MOS integrated circuit.

PRÉCAUTION/CAUTION :

Ces dispositifs sont sensibles aux décharges
électrostatiques.
These are electrostatic sensitive devices.

NIVEAUX D'ASSURANCE DE QUALITÉ : γ
ASSESSMENT LEVELS :

1 DESCRIPTION DU MODÈLE TYPE DESCRIPTION

Mémoire organisée en 16 k × 1 éléments binaires
Memory organization 16 k × 1 bits

Mode d'adressage asynchrone
Asynchronous addressing mode

Entrées et sorties compatibles TTL
TTL compatible inputs/outputs

Mode de rétention de données : 20μA/2 V
Data retention mode :

Sorties 3 états
Three state outputs

Se reporter à la Liste des produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

2 OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range unless otherwise specified.

2.1 General description

The 65262 is a 16 k bits static RAM operating in asynchronous mode. Particular functions available are :

- chip select;
- output enable;
- input gating;
- stand-by mode;
- data retention mode.

All inputs and outputs are TTL and CMOS compatible. Output has three state capability.

This memory can operate between 4.5 V and 5.5 V with nominal supply voltage at 5 V. The typical operating consumption is 50 mA with a derating of 5 mA per MHz. Access and cycle times are given below for the 2 categories :

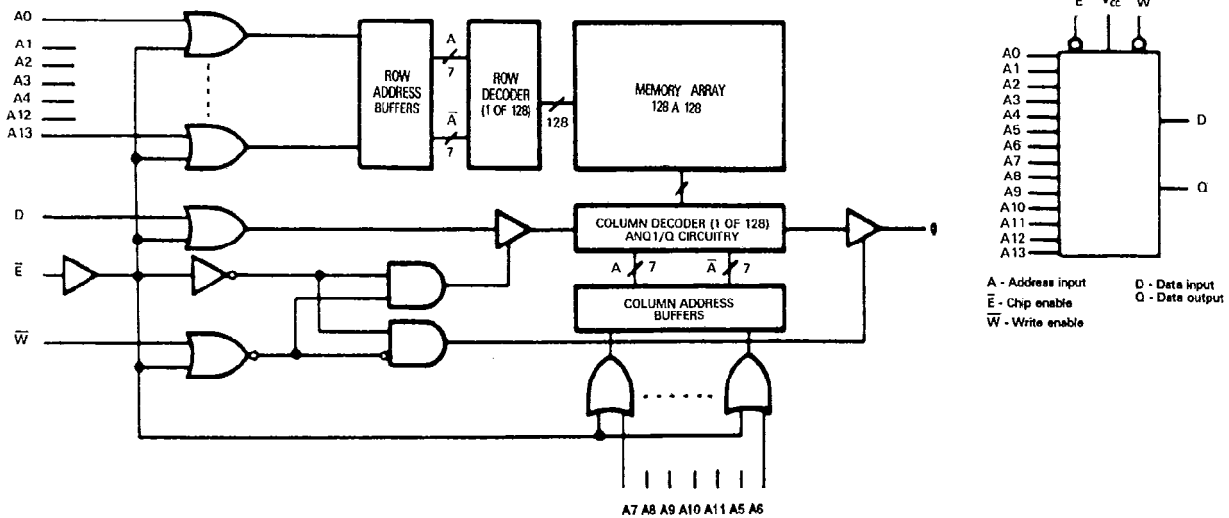
	65 262	65 262B	Unit
Access time	85	70	ns
Cycle time	85	70	ns

Function performed by each terminal is given here after.

Pin number		Symbol	Terminal function
DC - DP packages	PP package		
1 to 7	1 to 1	AO to A 6	Address : AO to A4 and A 12, A 13 used for Row selection
13 to 19	13 to 19	A7 to A13	A5 to all used for column selection
8	8	Q	Data output
9	9	$\bar{W}$	Write enable active fat low level Control of read-write mode
10	10	GND	Ground reference for supply voltage
11	11	$\bar{E}$	Chip enable active at low level control of chip selection and validation
12	12	D	Data input
20	20	V _{cc}	Supply voltage

Block diagram

Logical symbol



2.2 Detailed Function Specification

— Memory size and organization.

The size of the memory is 16 384 bits organized in 1 bank of 16 384 bits.

— Addressing mode :

In asynchronous memory, internal or external signals are not locked or latched. So when chip is selected correct addressing mode requires presence of address levels during all read/write sequence. Address scrambling for internal decoding system is given in block diagram.

Particular functions :

— Chip select and input gating

Chip select is active with a low level. This input validates all inputs (address and data) and authorizes functionality of the circuit. When this pin is at high level, a system called « input gating » authorizes floating states on address bus without change of the memory state and excessive consumption. This system allows also a direct connection to address bus without pull-up or pull-down resistor to maintain levels during de-selection.

— Output enable

A logic command elaborates validation of internal signals using chip select and write levels. Output state is valid only when chip select is at low level and write at high level together. When output is disabled, this output pin is at high impedance (three state level).

— Stand-by mode

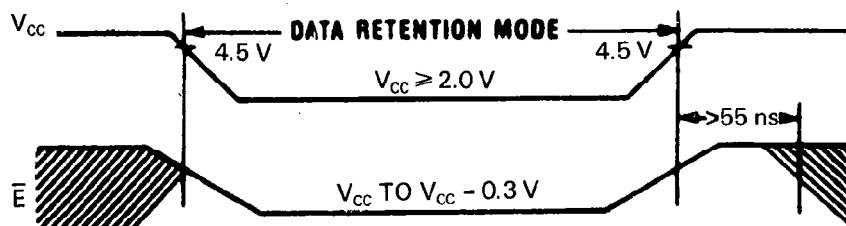
This mode is assured by de-selection of the memory and output. The supply current in this state is low and function of voltage on chip select pin.

— Data retention mode

It is the same that stand-by mode except that supply voltage can go down to 2 V allowing a battery back-up supply. Particular rules for this particular mode are given here after :

- 1 - Chip select ($\bar{E}$) must be held high during data retention within V_{CC} to $V_{CC} - 0.3$ V.
- 2 - $\bar{E}$ must be kept between $V_{CC} + 0.3$ V and 70 % of V_{CC} during the power up and power down transitions. data retention within V_{CC} to $V_{CC} - 0.3$ V.
- 3 - The RAM can begin operations 55 ns after V_{CC} reaches the minimum operating voltage 4.5 V.

DATA RETENTION TIMING



In both operating modes, informations in the memory before the selections are kept.

Truth table :

V	Address	E	W	D	Q	Mode	
Nominal	X	H	X	X	Z	Wait (st. by)	X : indifferent
•	V	L	H	X	V	Read	V. : valid
•	V	L	L	V	Z	Write	Z : three states
> 2 V	X	H	X	X	Z	Wait (data ret)	H : high
							L : low

2.3 Limiting conditions of use (ratings)

Limiting conditions (ratings) are not for inspection purposes.

Memory described in this specification is electrostatic discharge sensitive and has to be handled with all usual protections to avoid this phenomenon. CMOS technology is sensitive to latch-up and precautions during operation must be taken. In particular, when the power is on, it is necessary to put all the accesses at ground level and then, set nominal voltage on supply and chip select pin. A climb of voltage on supply pin must precede a climb of voltage on other input pins.

All voltages are referenced to a reference terminal GND or 0V.

Characteristics	Symbol	min.	max.	Unit
Supply voltage	V_{CC}	- 0,3	+ 7	V
Input voltages (Note 2)	V_i	GND-0,3	$V_{CC} + 0,3$	V
Output voltages	V_o	GND-0,3	$V_{CC} + 0,3$	V
Off-state voltage (Note 1)	V_{oz}			V
Output currents	I_o	- 15	15	mA
Input currents	I_i	- 15	15	mA
Max. power-dissipation (Note 1)	P_D max.			W
Operating temperature	T_{amb}	- 55	+ 125	°C
Storage temperature	T_{stg}	- 65	+ 150	°C

Note 1 : Not appropriate.
 Note 2 : For input voltage, a transient low level voltage of - 1 volt during 50 ns is authorized without destruction.

2.4 Recommended conditions of use and associated characteristics

(In accordance with 5.3.8 of CECC 90 100).

The characteristics apply over the full operating temperature range.

2.4.1 Recommended conditions of use

All voltages are referenced to a reference terminal (V_{SS} , GND, etc.).

Characteristics	Conditions	Symbol	min.	max.	Unit
Supply voltage		V_{CC} (Note 1)	4,5	5,5	V
Data retention voltage		$V_{DD(DR)}$	2	5,5	V
Low level input voltage		V_{IL}	- 0,3	0,8	V
High level input voltage		V_{IH}	2,2	$V_{CC} + 0,3$	V
Operating temperature		T_{amb}	- 55	+ 125	°C

Note 1 : Where appropriate these values should also be quoted under standby conditions.

2.4.2 Associated characteristics : not applicable