

OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range unless otherwise specified.

2.1 General description

The 65664 is a very low power CMOS static RAM organized as 8192 * 8 bits. It is manufactured using the MHS high performance CMOS technology named SCMOS.

Utilizing an array of six transistors (6T) memory cells, the HM 65664 combines an extremely low standby supply current (typical value = 0.1 μ A) with an access time at 45 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft error due to noise.

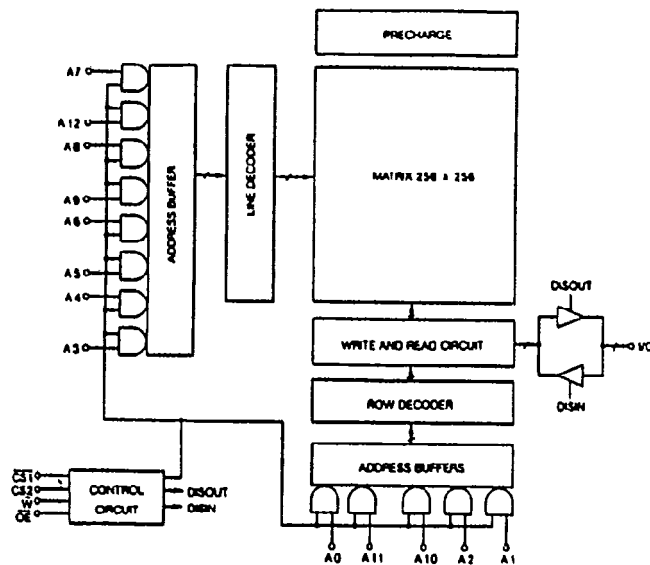
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.

	65664 B	65664 S	65664	65664 C	UNIT
Access time	45	45	55	55	ns
Cycle time	45	45	55	55	ns
Consumption ICCSB1	50	500	50	500	μ A

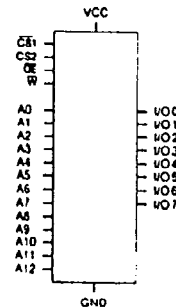
Function performed by each terminal is given here after.

PIN NUMBER		SYMBOL	TERMINAL FUNCTION
DIL .3 & .6	LCC 32P.		
2 to 10 ,21 23,24,25	3 to 11,24 27,28,29	A0 to A12	Address A3 to A9 & A12 used for Row sel. A0,A1,A2,A10,A11 used for column sel.
11,12,13 15 to 19	13,14,15 18 to 22	I/O 0 to I/O 7	Data Input/Output
14	16	GND	Ground reference for supply voltage
20	23	CS1	Chip-Select 1
26	30	CS2	Chip-Select 2
22	25	OE	Output Enable
27	31	W	Write Enable
28	32	V _{CC}	Supply voltage
1	1,2,17,26	NC	no connected

BLOCK DIAGRAM



LOGIC SYMBOL



2.2 Detailed Function Specification

- Memory size and organization.

The size of the memory is 65536 bits organized in 8 bank of 8192 bits.

- Addressing mode.

In asynchronous memory, internal or external signals are not locked or latched. So when chip is selected correct addressing mode requires presence of address levels during all read/write sequence. Address scrambling for internal decoding system is given in block diagram.

- Chip select and input gating.

Chip select 1 is active to low level, Chip select 2 is active to high level. This inputs configuration validates all inputs (address & data) and authorizes functionality of the circuit. When chip select 1 is at high level or chip select 2 is at low level, a system called "input gating" authorizes floating states on address bus without change of the memory state and excessive consumption. This system allows also a direct connection to address bus without pull-up or pull-down resistor to maintain levels during de-selection.

- Stand-by mode

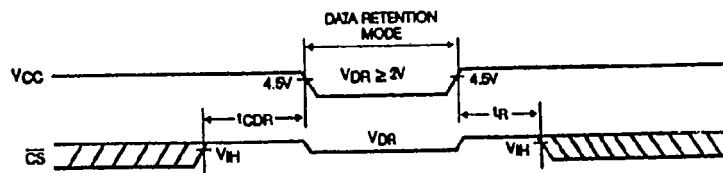
This mode is assured by de-selection of the memory and output. The supply current in this state is low and function of voltage on chip select pins.

- Data retention mode

This CMOS RAM's is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data-retention.

1. Chip select (CS1) must be held high during data retention ; within V_{CC} to $V_{CC} + 0,3$ V.
2. Output Enable (OE) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. CS and OE must be kept between $V_{CC} + 0.3$ V and 70 % of V_{CC} during the power down transitions.
4. The RAM can begin operation > 45 ns after V_{CC} reaches the minimum operating voltage (4.5 V).

Timing



In both operating modes, informations in the memory before the selections are kept.

Truth table

Address	CS1	CS2	OE	W	Inputs/Outputs	Mode
X	1	X	X	X	Z	deselect/Power down
V	0	1	0	1	Data Out	Read
V	0	1	X	0	Data In	Write
X	0	1	1	1	Z	Output disable
X	X	0	X	X	Z	deselect/Power down

2.3 Limiting conditions of use (ratings)

Limiting conditions (ratings) are not for inspection purposes.

Memory described in this specification is electrostatic discharge sensitive and has to be handled with all usual protections to avoid this phenomenon. Even the use of epitaxial base wafer and the good latch-up immunity, CMOS technology is sensitive to latch-up and precautions during operation must be taken. In particular, when the power is on, it is necessary to put all the accesses at ground level and then, set nominal voltage on supply and chip select pin. A climb of voltage on supply pin must precede a climb of voltage on other input pins.

All voltages are referenced to a reference terminal GND or 0 V.

Characteristics	Symbol	min.	max.	Unit
Supply voltage	V_{CC}	- 0.5	+ 7	V
Input voltage (note 1)	V_I	GND - 0.5	$V_{CC} + 0.5$	V
Output voltages	V_O	GND - 0.5	$V_{CC} + 0.5$	V
Output currents	I_O	- 15	+ 15	mA
Input currents	I_I	- 15	+ 15	mA
Operating temperature	T_{amb}	- 55	+ 125	°C
Storage temperature	T_{stg}	- 65	+ 150	°C

Note 1 : For input voltage, a transient low level voltage of - 1 V during 50 ns is authorized without destruction.

2.4 Recommended conditions of use and associated characteristics (In accordance with 5.3.8 of CECC 90 100).

The characteristics apply over full operating temperature range.

2.4.1 Recommended conditions of use

All voltages are referenced to a reference terminal (V_{SS} , GND, etc.).

Characteristics	Symbol	min.	max.	Unit
Supply voltage	V_{CC} (note 1)	4.5	5.5	V
Data retention voltage (note 1)	$V_{DD(DR)}$	2	5.5	V
Low level input voltage	V_{IL}	- 0.5	0.8	V
High level input voltage	V_{IH}	2.2	$V_{CC} + 0.5$	V
Operating temperature	T_{amb}	- 55	+ 125	°C

Note 1 : Where appropriate these values should also be quoted under standby conditions

2.4.2 Associated characteristics : not applicable

2.5 Static characteristics

All voltages are referenced to a reference terminal (V_{SS} , GND, etc.).

HM 65664 and HM 65664 B

Characteristics	Conditions	Symbol	min.	max.	Unit
Maximum supply current(s) for - Normal mode	V_{CC} max. Note 1 Note 2	I_{CC1} I_{CC2}		75 15	mA mA
- Power down	Note 3	I_{CC3}		50	μ A
Maximum supply current for data retention mode	V_{CC} max. V_{IH} $V_{DD(OR)} = 2 V$	$I_{DD(OR)}$		20	μ A
High level input voltage	V_{CC} max.	V_{IH}	2.2	$V_{CC}+0.3$	V
Low level input voltage	V_{CC} min.	V_{IL}	- 0.3	0.8	V
High level output voltage	Note 4	V_{OH}	2.4		V
Low level output voltage	Note 4	V_{OL}		+ 0.4	V
High level input or leakage cur.	V_{CC} max.	I_{IH}	- 1	+ 1	μ A
Low level input or leakage cur.	V_{CC} max.	I_{IL}	- 1	+ 1	μ A
High level output leakage current at three-state outputs	V_{CC} max.	I_{OHZ}	- 1	+ 1	μ A
Low level output leakage current at three-state outputs	V_{CC} max.	I_{OLZ}	- 1	+ 1	μ A

Note 1 : V_{CC} max., $I_O = 0$ mA, $f = \text{max.}$, $V_I = V_{CC}/\text{GND}$

Note 2 : $CS1 \geq V_{IH}$, $CS2 \leq V_{IL}$

Note 3 : $CS1 \geq V_{CC} - 0.3$ V, $CS2 \leq 0.3$ V, Output current = 0 mA

Note 4 : V_{CC} min., $I_{OL} = 4$ mA, $I_{OH} = - 1$ mA