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**UTE**

Spécification française harmonisée  
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**CECC 90 111-C20**

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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE DE  
QUALITE CONFORMEMENT A :

*ELECTRONIC COMPONENTS OF ASSESSED QUALITY  
IN ACCORDANCE WITH :*

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 111 (NF C 86-254)

**UTE C 86-254 ADD. 3/005**

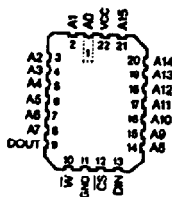
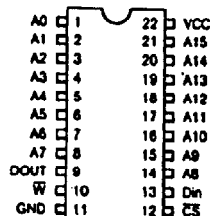
Adoptée le 14 juin 1991

DESSIN ET DIMENSIONS :  
*OUTLINE AND DIMENSIONS*

Voir annexe/See annex

IDENTIFICATION DES CONNEXIONS  
*TERMINAL CONNECTIONS*

Boîtiers/Packages DC - DP



Boîtier/Package PP

SPECIFICATION PARTICULIERE POUR MEMOIRES RAM  
STATIQUES LECTURE ECRITURE A CIRCUITS INTEGRES  
*DETAIL SPECIFICATION FOR MOS READ/WRITE STATIC  
MEMORIES SILICON MONOLITHIC CIRCUITS*

**MODELE/TYPE 65 687**

Variétés électriques/*Electrical variants*

HM 65 687  
HM 65 687 C

HM 65 687 B  
HM 65 687 S

TECHNOLOGIE DE FABRICATION :

*TYPICAL CONSTRUCTION :*

Circuit monolithique C MOS au silicium.

*Silicon monolithic C MOS integrated circuit.*

PRECAUTION/CAUTION :

Ces dispositifs sont sensibles aux décharges  
électrostatiques.

*These are electrostatic sensitive devices.*



NIVEAU D'ASSURANCE DE LA QUALITE : γ  
ASSESSMENT LEVEL :

### 1 - DESCRIPTION DU MODELE *TYPE DESCRIPTION*

Mémoire organisée en 65 536 x 1 éléments binaires/*Memory organization 65 536 x 1 bits.*

Mode d'adressage asynchrone/*Asynchronous addressing mode.*

Entrées et sorties compatibles TTL/*TTL compatible inputs/outputs.*

Temps d'accès/*Access time : 45/55 ns.*

Faible consommation/*Very low power consumption :*

- en fonctionnement/*active : 175 mW (typ.)*
- en mode repos/*standby : 2 μW (typ.)*
- en mode rétention de données/*data-retention : 0.8 μW (typ.)*

Sorties 3 états/*Three state outputs.*

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants  
conformes à cette spécification particulière sont homologués.

*Information about manufacturers who have components qualified to this detail specification is available in the current  
CECC 00 200 : Qualified Products List.*

Editée par l'Union technique de l'Electricité, Cedex 64, 92052 PARIS LA DEFENSE - Tél. : 33 (1) 46 91 11 11

## 2 OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range unless otherwise specified.

### 2.1 General description

The 65687 is a very low power CMOS static RAM organized as 65536 \* 1 bit. It is manufactured using the MHS high performance CMOS technology named SCMOS.

Utilizing an array of six transistors (6T) memory cells, the HM 65687 combines an extremely low standby supply current (typical value = 0.1  $\mu$ A) with an access time at 45 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft error due to noise.

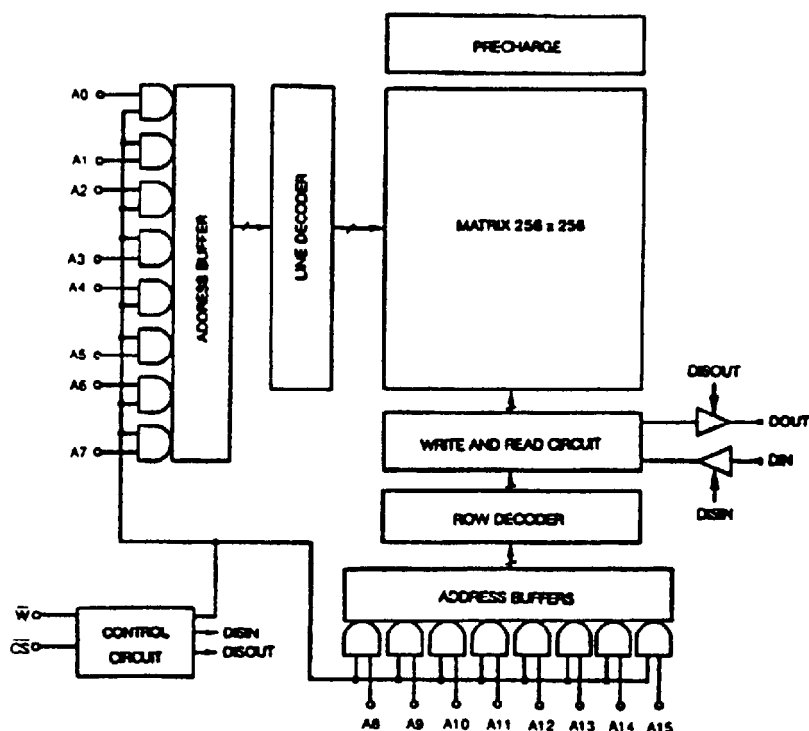
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.

|                       | 65687 B | 65687 S | 65687 | 65687 C | UNIT    |
|-----------------------|---------|---------|-------|---------|---------|
| Access time           | 45      | 45      | 55    | 55      | ns      |
| Cycle time            | 45      | 45      | 55    | 55      | ns      |
| consumption<br>ICCSB1 | 50      | 500     | 50    | 500     | $\mu$ A |

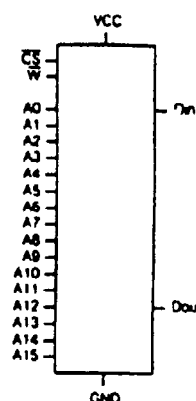
Function performed by each terminal is given here after.

| PIN NUMBER         |                    | SYMBOL          | TERMINAL FUNCTION                                                                 |
|--------------------|--------------------|-----------------|-----------------------------------------------------------------------------------|
| DIL 22P.           | LCC 22P.           |                 |                                                                                   |
| 1 to 8<br>14 to 21 | 1 to 8<br>14 to 21 | A0 to A15       | Address A0 to A7 used for Row selection<br>Address A8 to A15 used for Column sel. |
| 9                  | 9                  | Dout            | Data Output                                                                       |
| 10                 | 10                 | W               | Write Enable                                                                      |
| 11                 | 11                 | GND             | Ground                                                                            |
| 12                 | 12                 | CS              | Chip-Select                                                                       |
| 13                 | 13                 | Din             | Data Input                                                                        |
| 22                 | 22                 | V <sub>CC</sub> | Supply voltage                                                                    |

## BLOCK DIAGRAM



## LOGIC SYMBOL



## 2.2 Detailed Function Specification

- Memory size and organization.

The size of the memory is 65536 bits organized in 1 bank of 65536 bits.

- Addressing mode.

In asynchronous memory, internal or external signals are not locked or latched. So when chip is selected correct addressing mode requires presence of address levels during all read/write sequence. Address scrambling for internal decoding system is given in block diagram.

- Chip select and input gating.

Chip select is active to low level. This inputs configuration validates all inputs (address & data) and authorizes functionality of the circuit. When chip select is at high level, a system called "input gating" authorizes floating states on address bus without change of the memory state and excessive consumption. This system allows also a direct connection to address bus without pull-up or pull-down resistor to maintain levels during de-selection.

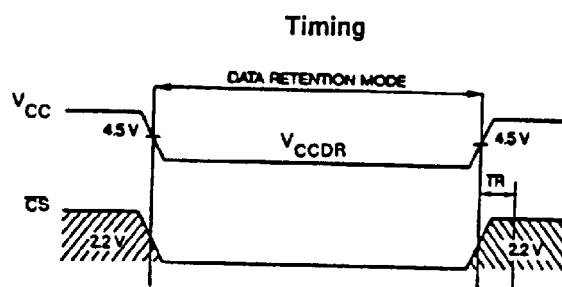
- Stand-by mode

This mode is assured by de-selection of the memory and output. The supply current in this state is low and function of voltage on chip select pins.

## - Data retention mode

This CMOS RAM's is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data-retention.

1. Chip select ( $\overline{CS}$ ) must be held high during data retention ; within  $V_{CC}$  to  $V_{CC} + 0.3$  V.
2. CS must be kept between  $V_{CC} + 0.3$  V and 70 % of  $V_{CC}$  during the power down transitions.
3. The RAM can begin operation  $> T_r$  after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).



In both operating modes, informations in the memory before the selections are kept.

Truth table

| Address | CS | W | Data-in | Data-out | Mode     |
|---------|----|---|---------|----------|----------|
| X       | 1  | X | Z       | Z        | Deselect |
| V       | 0  | 1 | Z       | Valid    | Read     |
| V       | 0  | 0 | Valid   | Z        | Write    |

L = low, H = high, X = H or L, Z = High Impedance

### 2.3 Limiting conditions of use (ratings)

Limiting conditions (ratings) are not for inspection purposes.

Memory described in this specification is electrostatic discharge sensitive and has to be handled with all usual protections to avoid this phenomenon. Even the use of epitaxial base wafer and the good latch-up immunity, CMOS technology is sensitive to latch-up and precautions during operation must be taken. In particular, when the power is on, it is necessary to put all the accesses at ground level and then, set nominal voltage on supply and chip select pin. A climb of voltage on supply pin must precede a climb of voltage on other input pins.