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Specification available from:
Siemens AG, Balanstr. 73
D-8000 Muenchen 80

CECC 90 112-005



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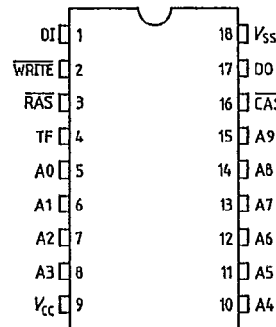
ELECTRONIC COMPONENTS OF ASSESSED
QUALITY IN ACCORDANCE WITH:
CECC 90 000: Generic Specification
for Monolithic Integrated Circuits
CECC 90 100: Sectional Specifica-
tion for Digital Monolithic
Integrated Circuits

OUTLINE AND DIMENSIONS:

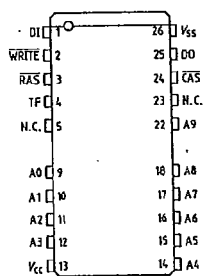
P-DIP-18 or P-SOJ-26-20

TERMINAL CONNECTIONS:

P-DIP-18



P-SOJ-26/20



DETAIL SPECIFICATION FOR:

HYB 511000A-70/-80/-10

1 048 576 x 1 Bit
Dynamic RAM

TYPICAL CONSTRUCTION: CMOS

CAUTION: These are electrostatic
sensitive devices

ASSESSMENT LEVEL(S): P,Y,L

1 - TYPE DESCRIPTION:

- 1 048 576 words by 1-bit organization
- Fast access and cycle time
 - 70 ns access time
 - 130 ns cycle time (HYB 511000A-70)
 - 80 ns access time
 - 150 ns cycle time (HYB 511000A-80)
 - 100 ns access time
 - 180 ns cycle time (HYB 511000A-10)
- Fast page mode cycle time
 - 40 ns (HYB 511000A-70)
 - 45 ns (HYB 511000A-80)
 - 55 ns (HYB 511000A-10)
- Single +5V ($\pm 10\%$) supply with a built-in V_{BB} generator

- Low power dissipation
 - max. 440 mW active (HYB 511000A-70)
 - max. 385 mW active (HYB 511000A-80)
 - max. 330 mW active (HYB 511000A-10)
 - max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read-modify-write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, fast page mode capability and test mode capability
- All inputs and output TTL-compatible
- 512 refresh cycles/8 ms
- Plastic Packages: P-DIP-18, P-SOJ-26/20

Information of components qualified to this detail specification is
available in the current CECC 00 200 : Qualified Products List.

2 OPERATING CHARACTERISTICS

The following characteristics are applied over the full operating temperature range (0 to 70 °C) and over the whole power supply range (5V $\pm$ 10 %).

2.1 General Descriptions

The HYB 511000A is a 1Mbit dynamic RAM which utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user.

- Nominal voltage supply:

The HYB 511000A has a single + 5V power supply with a built-in VBB generator.

- Types of refresh modes:

Three different refresh modes are possible: RAS-Only Refresh Cycle, Hidden Refresh Cycle (read / write) and CAS-Before-RAS Refresh Cycle. The first two modes require nine external refresh addresses. In the CAS-Before-RAS Refresh mode no external refresh addresses are required. If the chip detects a CAS-Before-RAS Cycle, a refresh counter is incremented by one supplying the row decoders with the new internally generated refresh addresses.

- Operating modes:

The basic operation (read cycle, write cycle and read-write cycle) is fully compatible with conventional DRAMs. In addition the HYB 511000A can operate in the fast page mode (fast page mode read cycle, fast page mode write cycle and fast page mode read-write cycle). This mode is a fast serial mode with 40 ns (HYB 511000A-70), 45 ns (HYB 511000A-80) and 55 ns (HYB 511000A-12) cycle time. 1024 bits can be addressed along the selected row in any address sequence.

- Electrical compatibility:

The HYB 511000A has multiplexed address inputs and is packaged in a standard 18-pin (DIL) or 20-pin (SOJ) plastic package as all 1Mbit DRAMs. In the basic operation the HYB 511000A is fully compatible with all other 1Mbit DRAMs. The devices can be handled with commonly used automatic testing and insertion equipment. Direct interfacing can be done with high performance logic devices such as Schottky TTL.

- Block Diagram:

In Figure 1 a block diagram of the HYB 511000A is shown.

2.2 Detailed Functional Specifications

- Memory size / organisation:

The HYB 511000A is a 1Mbit dynamic RAM with fast page mode possibility organized as 1 048 576 words by 1 bit.

- Addressing mode:

In order to decode 1 of 1 048 576 memory cells twenty binary address inputs are required. The HYB 511000A have ten multiplexed address inputs (A0 - A9). Ten row address bits are latched with the row address strobe ($\overline{RAS}$), all row address must be stable on or before the falling edge of $\overline{RAS}$ and during the row address hold time. The ten column address bits are latched with the column address strobe ($\overline{CAS}$), all column addresses must be stable on or before the falling edge of $\overline{CAS}$ and during the column address hold time.

- Write enable:

The read or write mode is selected with the $\overline{WRITE}$ input. High on $\overline{WRITE}$ selects the read mode, low the write mode. In the read mode the data input is disabled.

Data is written in with the last falling edge of $\overline{WRITE}$ or $\overline{CAS}$. If $\overline{WRITE}$ goes low before $\overline{CAS}$ transition to low, data-in is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If $\overline{WRITE}$ goes low after $\overline{CAS}$ transition to low, data-in is strobed by $\overline{WRITE}$ and set-up and hold times are referenced to $\overline{WRITE}$.

- Output enable:

The output buffer is three-state TTL compatible. The output buffer is controlled by the state of $\overline{WRITE}$ when $\overline{CAS}$ ($\overline{CS}$) goes low. The output buffer is in the high impedance state until $\overline{CAS}$ goes low and returns to the high impedance state when $\overline{CAS}$ goes high.

When $\overline{WRITE}$ is in the low state before a $\overline{CAS}$ transition to low the early-write mode is selected, in which the output floats and a common I/O capability exists.

The unlatched output at the cycle end allows two-dimensional chip selection.

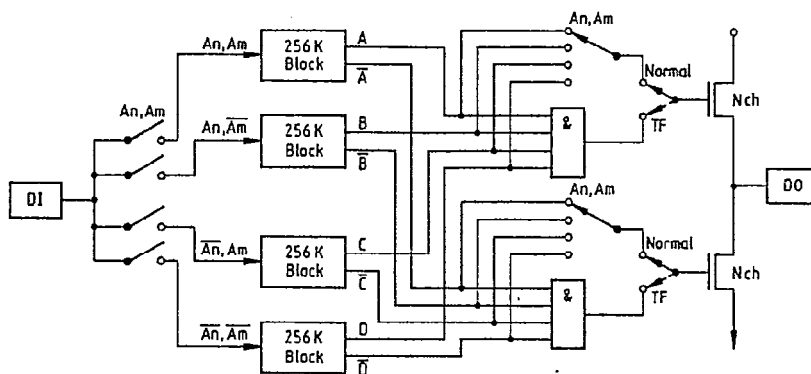
- Test mode

The HYB511000A is internally organized 262 144 words by 4 bit. In "test mode", data would be written into a number of sectors (4 sectors) in parallel and retrieved the same way. If upon reading, all bits are equal (all "H" or "L"), the data output pin indicates the same data as the 4 bits. In this case, the data output pin indicates the expected data for good parts. If any of the bits differed, the data output pin would indicate

a high impedance state for bad parts. In figure 2 the block diagram is shown including its truth table when test mode is used.

In test mode 1M DRAM can be tested as if it were 256k DRAM by the following method.

Figure 2:



TF = Super voltage; Test Mode
TF = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test mode Function

A	B	C	D	DO
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

Test mode function is performed on any of the timing cycles including fast page mode when TF pin is held on supervoltage ($V_{CC} + 4.5$ V) for the specified period (see 2.6 dynamic characteristics and 2.7 timing diagram). The address input A9 is ignored in the test mode.

On the other hand, normal operation requires the TF pin be connected to V_{IL} (TF) level, or left unconnected on the printing wiring board. The test mode function reduces test times (1/4 in case of using N test pattern). This test mode function is implemented from revision C.

2.3 Limiting Conditions of Use (Absolute Maximum Ratings)

The limiting conditions of use are not for inspection purposes. The values of limiting conditions of use are given in the table 2. All voltages are referred to $V_{SS} = GND$.

Table 2:

Characteristics	Symbol	min	max	Unit
Supply voltage	V_{CC}	-1	+7	V
Input voltages	V_I	-1	+7	V
Test function input voltages	V_I	-1	10.5	V
Output voltages	V_O	-1	+7	V
Output currents (note 1)	I_O	-50	+50	mA
Input currents	I_I	-15	+15	mA
Max. power dissipation	$P_D \text{ max}$	--	0,6	W
Operating temperature	T_{amb}	0	+70	$^{\circ}C$
Storage temperature	T_{stg}	-55	+150	$^{\circ}C$

Note 1: Short circuit

Stresses above those listed under limiting rating conditions may cause permanent damage to the device. Exposure to absolute rating conditions for extended periods may effect device reliability.

Warning: These are electrostatic sensitive devices.

2.4 Recommended Conditions of Use and Associated Characteristics (In accordance with 5.3.8 of CECC 90 100)

The values of recommended conditions of use are given in the table 3. All voltages are referred to $V_{SS} = GND$.

Table 3:

Characteristics	Condition	Symbol	min	max	Unit
Supply voltage		V_{CC}	4.5	5.5	V
Low level input voltages		V_{IL}	- 1	0.8	V
High level input voltages		V_{IH}	2.4	6.5	V
Test enable input high voltage		$V_{IH(TF)}$	$V_{CC} + 4.5$	10.5	V
Test disable input low voltage		$V_{IL(TF)}$	- 1	$V_{CC} + 1.0$	V
Operating temperature		T_{amb}	0	+70	$^{\circ}C$

2.5 Static Characteristics

All voltages are referred to $V_{SS} = 0\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$,
 $T_{amb} = 0\text{ to }70\text{ }^{\circ}\text{C}$.

Table 4:

Characteristics	Test condition	Symbol	min	max	Unit
Average V_{CC} supply current HYB 511000A-70 HYB 511000A-80 HYB 511000A-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling $t_{RC} = t_{RC\ min}$)	Note 2,3 Note 2,3 Note 2,3	I_{CC1}	-	80 70 60	mA mA mA
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}	-	2	mA
Average V_{CC} supply current during $\overline{RAS}$ -only Refresh cycles: HYB 511000A-70 HYB 511000A-80 HYB 511000A-10 ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC\ min}$)	Note 2 Note 2 Note 2	I_{CC3}	-	80 70 60	mA mA mA
Average V_{CC} supply current during fast page mode HYB 511000A-70 HYB 511000A-80 HYB 511000A-10 ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling, $t_{PC} = t_{PC\ min}$)	Note 2,3 Note 2,3 Note 2,3	I_{CC4}	-	60 50 40	mA mA mA
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2\text{ V}$)		I_{CC5}	-	1	mA
Average V_{CC} supply current during $\overline{CAS}$ before $\overline{RAS}$ refresh mode HYB 511000A-70 HYB 511000A-80 HYB 511000A-10 ($\overline{RAS}$, $\overline{CAS}$, cycling $t_{RC} = t_{RC\ min}$)	Note 2 Note 2 Note 2	I_{CC6}	-	80 70 60	mA mA mA
Test function input current $V_{CC} + 4.5\text{ V} < V_{IN(TF)} < 10.5\text{ V}$		I_{ITF}	-	1	mA

For notes see page 9

Table 4 (continued):

Characteristics	Test condition	Symbol	min	max	Unit
Input high voltage		V_{IH}	2.4	6.5	V
Input low voltage		V_{IL}	- 1	0.8	V
Test enable input high voltages		$V_{IH(TF)}$	$V_{CC} + 4.5$	10.5	V
Test disable input low voltages		$V_{IL(TF)}$	- 1	$V_{CC} + 1.0$	V
Output high voltages ($I_{OUT} = - 5$ mA)		V_{OH}	2.4	-	V
Output low voltages ($I_{OUT} = 4.2$ mA)		V_{OL}	-	0.4	V
Input leakage current, any input except TF ($0\text{ V} \leq V_{IN} < 6.5\text{ V}$, all other pins = 0 V)		I_{IL}	-10	10	uA
Input leakage current, only TF ($0\text{ V} \leq V_{IN(TF)} < V_{CC} + 0.5\text{ V}$, all other pins = 0 V)		$I_{IL(TF)}$	-10	10	uA
Output leakage current (DO is disabled, $0\text{ V} < V_{OUT} < V_{CC}$)		I_{OL}	-10	10	uA

Note 2 - I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate

Note 3 - I_{CC1} , I_{CC4} depend on output loading. Specified values are measured with the output open.

2.6 Dynamic Characteristics

All voltages are referred to $V_{SS} = 0\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$,
 $T_{amb} = 0\text{ to }70\text{ }^{\circ}\text{C}$, $t_T = 5\text{ ns}$.

Table 5:

Characteristics	Conditions	Symbol	HYB 511000A -70		HYB 511000A -80		HYB 511000A -10		Unit
			min	max	min	max	min	max	
TRANSITION TIME	Note 4, 5								
.Rise and fall time		t_T	3	50	3	50	3	50	ns
CYCLE TIMES	Note 4, 5								
.Read		t_{RC}	130	-	150	-	180	-	ns
.Write		t_{RC}	130	-	150	-	180	-	ns
.Read-write		t_{RWC}	155	-	175	-	210	-	ns
.Fast page mode read		t_{PC}	40	-	45	-	55	-	ns
.Fast page mode write		t_{PC}	40	-	45	-	55	-	ns
.Fast page mode read-write		t_{PRWC}	65	-	70	-	85	-	ns
.Refresh period		t_{REF}	-	8	-	8	-	8	ms
ACCESS TIMES	Note 4, 5								
-Read operation:									
.from $\overline{RAS}$	Note 6, 11	t_{RAC}	-	70	-	80	-	100	ns
.from $\overline{CAS}$	Note 6, 11	t_{CAC}	-	20	-	20	-	25	ns
.from column address	Note 6, 12	t_{AA}	-	35	-	40	-	50	ns
-Read-write operation:									
.as for read operation									
-Fast page mode read operation:									
.from $\overline{CAS}$	Note 6, 11	t_{CAC}	-	20	-	20	-	25	ns
.from column address	Note 6, 12	t_{AA}	-	35	-	40	-	50	ns
.from $\overline{CAS}$ precharge	Note 6	t_{CPA}	-	35	-	40	-	50	ns
PULSE DURATION	Note 4, 5								
-Read operation:									
. $\overline{CAS}$ pulse width		t_{CAS}	20	10^4	20	10^4	25	10^4	ns
. $\overline{RAS}$ pulse width		t_{RAS}	70	10^4	80	10^4	100	10^4	ns
. $\overline{RAS}$ precharge time		t_{RP}	50	-	60	-	70	-	ns
-Write operation:									
. $\overline{RAS}$ pulse width		t_{RAS}	70	10^4	80	10^4	100	10^4	ns
. $\overline{RAS}$ precharge time		t_{RP}	50	-	60	-	70	-	ns
. $\overline{CAS}$ pulse width		t_{CAS}	20	10^4	20	10^4	25	10^4	ns
.WRITE pulse width		t_{WP}	15	-	15	-	20	-	ns
-Read-write operation:									
.as for write operation									

For notes see page 17

Table 5 (continued):

Characteristics	Conditions	Symbol	HYB 511000A -70		HYB 511000A -80		HYB 511000A -10		Unit
			min	max	min	max	min	max	
-Fast page mode read operation:									
.RAS pulse width		t_{RASP}	70	10^5	80	10^5	100	10^5	ns
.CAS pulse width		t_{CAS}	20	10^4	20	10^4	25	10^4	ns
.CAS precharge time		t_{CP}	10	-	10	-	10	-	ns
.RAS precharge time		t_{RP}	50	-	60	-	70	-	ns
-Fast page mode write operation:									
.RAS pulse width		t_{RASP}	70	10^5	80	10^5	100	10^5	ns
.CAS pulse width		t_{CAS}	20	10^4	20	10^4	25	10^4	ns
.CAS precharge time		t_{CP}	10	-	10	-	10	-	ns
.RAS precharge time		t_{RP}	50	-	60	-	70	-	ns
.WRITE pulse width		t_{WP}	15	-	15	-	20	-	ns
-Fast page mode read-write operation:									
.as for fast mode write operation									
-RAS only refresh operation:									
.as for read operation									
-CAS before RAS refresh operation:									
.RAS pulse width		t_{RAS}	70	10^4	80	10^4	100	10^4	ns
.RAS precharge time		t_{RP}	50	-	60	-	70	-	ns
.CAS precharge time		t_{CPN}	10	-	10	-	15	-	ns
-Hidden refresh read operation:									
.as for read operation									
-Hidden refresh write operation:									
.as for write operation									
-CAS before RAS refresh counter operation:									
.CAS pulse width		t_{CAS}	20	10^4	20	10^4	25	10^4	ns
.CAS precharge time		t_{CPT}	40	-	40	-	50	-	ns
.RAS pulse width		t_{RAS}	70	10^4	80	10^4	100	10^4	ns
.RAS precharge time		t_{RP}	50	-	60	-	70	-	ns
.WRITE pulse width		t_{WP}	15	-	15	-	20	-	ns
-Test mode operation:									
.as for read, write, read-write or fast page operation									

For notes see page 17