

UTE

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COMPOSANTS ELECTRONIQUES SOUS ASSURANCE
DE QUALITE CONFORMEMENT A :
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :

GS : CECC 90 000 (NF C 86-020)

SS : CECC 90 100 (NF C 86-200)

FS : CECC 90 113 (NF C 86-252)

UTE C 86-252-001

Adoptée le 2 juillet 1987

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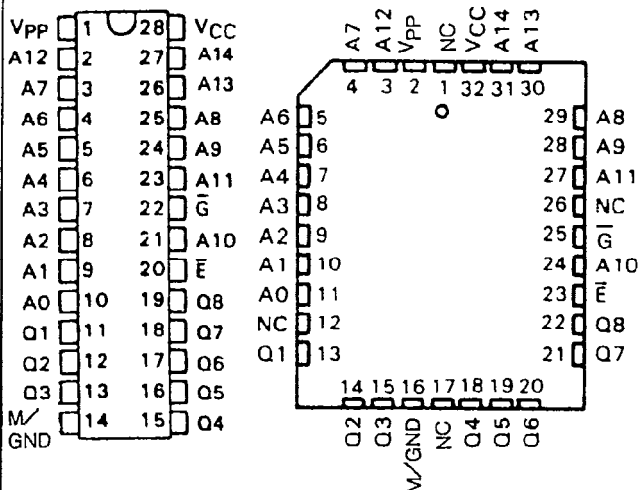
DESSIN ET DIMENSIONS :
OUTLINE AND DIMENSIONS :

CEI 191-2 - Types } 051 G 05 - 051 G 06 :
IEC 191-2 - Types } Boîtier/Package DC
Boîtier PC : voir annexe
Package PC : see Annex

IDENTIFICATION DES CONNEXIONS
TERMINAL CONNECTIONS

Boîtier DC
DC package

Boîtier PC
PC package



SPECIFICATION PARTICULIERE POUR
MEMOIRES MORTES MOS A CIRCUITS
INTEGRES, EFFACABLES AUX UV,
PROGRAMMABLES ELECTRIQUEMENT

DETAIL SPECIFICATION FOR MOS ULTRA-
VIOLET LIGHT ERASABLE, ELECTRICALLY
PROGRAMMABLE READ ONLY MEMORIES
SILICON MONOLITHIC CIRCUITS

MODELE/TYPE 27C256

- Variétés électriques/Electrical variants
 - 27C256-17 / 27C256-20 / 27C256-25
 - 27C256-30 / 27C256-35

- Variétés température/boîtier
Temperature/package variants

Boîtiers Packages	Températures/Temperatures	
	0 °C, + 70 °C - 40 °C, + 85 °C	- 55 °C, + 125 °C
DC	X	X
PC		X

TECHNOLOGIE DE FABRICATION :
TYPICAL CONSTRUCTION :

Circuit monolithique HVC MOS au silicium.
Silicon monolithic HVC MOS integrated circuit.

PRECAUTION/CAUTION :

Ces dispositifs sont sensibles aux décharges
électrostatiques.

These are electrostatic sensitive devices.

NIVEAUX D'ASSURANCE DE QUALITE :

ASSESSMENT LEVELS :

Y, L

1 - DESCRIPTION DU MODELE TYPE DESCRIPTION

Mémoire organisée en 32 k x 8 éléments binaires, entrées et sorties compatibles TTL, sorties 3 états.
Memory organization 32 k x 8. All inputs/outputs fully TTL compatible. 3-state outputs.

Se reporter à la Liste des Produits Homologués CECC 00 200 en vigueur pour connaître les fabricants dont les composants conformes à cette spécification particulière sont homologués.

Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.

2 OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range $V_{CC} = 5\text{ V} \pm 10\%$.

2.1 General description

The 27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The 27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C .

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C256. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C256 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 210 mW at 5 V.

Maximum standby power dissipation : 1,40 mW at 5 V.

This memory has static operation : no clocks no refresh.

Max Access/Min Cycle Time :

27C256-17 170 ns

27C256-20 200 ns

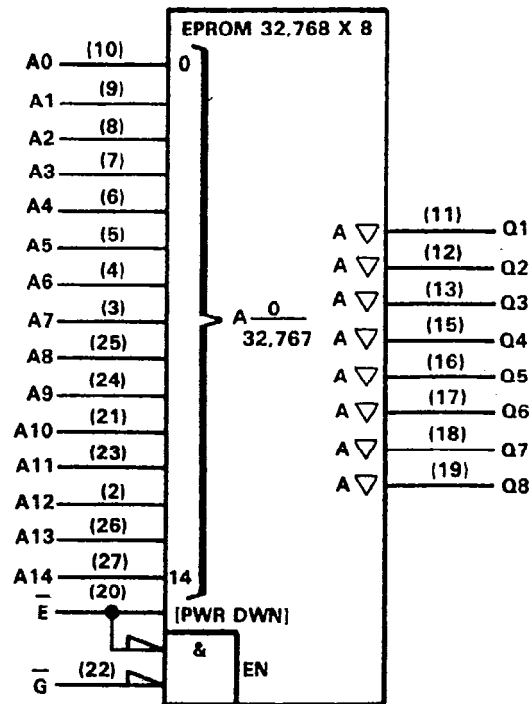
27C256-25 250 ns

27C256-30 300 ns

27C256-45 450 ns

This memory is fully compatible with TTL families S, LS, AS, ALS.

Logic symbol



PIN NOMENCLATURE	
A0-A14	Addresses
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
Q1-Q8	Outputs
VCC	5-V Power Supply
Vpp	12.5-V Power Supply
GND	Ground

2.2 Detailed Functional Specification

2.2.1 Function description

The 27C256 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 262, 144 bits organized as 32,768 words of 8 bits length.

When the outputs of two or more 27C256's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the 27C256, a low-level signal is applied to the $\bar{E}$ and $\bar{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

Output data is accessed at pins Q1 to Q8.

Active I_{CC} current can be reduced by applying a high TTL signal to the $\bar{E}$ pin. In this mode all outputs are in the high-impedance state.

Program inhibit

Programming may be inhibited by maintaining a high-level input on the $\bar{E}$ pin.

Program verify

Programmed bits may be verified with $V_{PP} = 12.5 \text{ V}$ when $\bar{G} = V_{IL}$ and $\bar{E} = V_{IH}$.

Signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to $12 \text{ V} \pm 0.5 \text{ V}$. Two identifier bytes are accessed by A0 (pin 10) i.e., $A0 = V_{IL}$ - manufacturer; $A0 = V_{IH}$ - device. All other addresses must be held at V_{IL} . Each byte possesses odd parity on bit Q8.

Initial logic state of the memory is state « 1 ».

Function table

FUNCTION (PINS)	MODE						
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode
$\bar{E}$ (20)	0	0	1	0	1	1	0
$\bar{G}$ (22)	0	1	X*	1	0	1	0
A9 (24)	X	X	X	X	X	X	V_H^*
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11-13, 15-19)	Q	HI-Z	HI-Z	D	Q	HI-Z	Code

* $V_H = 12 \text{ V} \pm 0.5 \text{ V}$.

2.2.2 Programming (writing of a content)

The programming operation is the storage of a sufficient quantity of negative electrical charges in the floating gate of a memory cell. This causes the change from the initial logic state to the programmed logic state.

Programming methods and conditions are described in Annex of this DS.

It is possible to modify further the memory content on unprogrammed cells. The normal functioning of the memory does not change its content.

In this one the parameters may be shown as organigrams or programming sequences. The different signal configurations and logic levels needed for programming are described in the Annex of this DS.

2.2.3 Erasing (return to the initial logic state)

The erasing operation is the removing of all the negative electrical charges which were in the floating gate of the memory cell. This unlatches the memory cell and sets it back to the initial logic state.

Erasing bringing back to the initial logic state is performed on all the memory cells.

The erasing methods, the erasing conditions, the UV source characteristics (wavelength and spectrum bandwidth of ultraviolet light) and the minimum erasure dosage to insure erasure are stated in the Annex of this DS.

2.2.4 Erasing/programming operations

The maximum number of erasing/programming operations is 100. This number is checked in the memory cells wear out test (see 4.11 of the BDS).

2.2.5 Data retention time

Data retention time is verified during Data retention test (see 4-10 of the BDS).

Test conditions for data retention test : see burn-in conditions in 2.9 of this DS.

2.3 Limiting conditions of use (ratings)

Limiting conditions (ratings) are not for inspection purposes.

Values of limiting conditions of use shall be given as follows :

All voltages are referenced to GND.

Characteristics	Symbol	min.	max.	Unit
Supply voltage	V_{CC}	-0,6	7	V
Programming supply voltage	V_{PP}	-0,6	14	V
Input voltages	(Except A9) V_I	-0,6	6,5	V
	(A9)	-0,6	13,5	
Output voltages	V_O	-0,6	$V_{CC} + 1$	V
Off-state voltage	V_{OZ}	-0,6	$V_{CC} + 1$	V
Output currents	I_O		5	mA
Input currents	I_I		15	mA
Max. power-dissipation	P_D max.	n.a.	0,14	W
Operating temperature	T_{amb}	Cat L	0	+ 70 °C
		Cat E	-40	+ 85 °C
		Cat M	-55	+ 125 °C
Storage temperature	T_{stg}	-65	+ 150	°C

Note 1): Where appropriate.