

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION PARTICULIERE CADRE:

CIRCUITS INTEGRES PREDIFFUSES

Harmonized System of Quality Assessment for
Electronic Components

BLANK DETAIL SPECIFICATION:

**DIGITAL GATE ARRAY
INTEGRATED CIRCUITS**

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

VORDRUCK FÜR BAUARTSPEZIFIKATION:

**INTEGRIERTE DIGITALSCHALTUNGEN,
GATE ARRAYS**



1

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or from the National Authorized Institutions
of the participating countries listed
who can supply copies of:

- 1 The Internal Regulations of the FEN e.V.
- 2 The Rules of Procedure of the System
- 3 CECC Specifications of the FEN and National Specifications for the System
- 4 CECC 00 200: Register of Firms, Products, and Services Approved under the CECC System
- 5 CECC 00 300: Register of National Documents Implementing CECC Publications and CECC European Standards
- 6 CECC 00 301: Register of CECC Specifications and Related Detail Specifications
- 7 Other CECC Publications and publicity documents

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby acceptable in all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for DIGITAL GATE ARRAY INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification, the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly sheet.

PREFACE

This blank detail specification (BDS) was prepared by CECC WG 9: "INTEGRATED CIRCUITS".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747: Semiconductor devices - Discrete devices and integrated circuits, and IEC 748: Semiconductor devices - Integrated circuits.

The text of this specification was circulated to the CECC for voting in the documents listed below and was approved for publication:

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat)2648	January 1991	CECC(Secretariat)2788

It is recognized that the layout proposed cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

AVIS

In accordance with the decision of the CECC Management Committee, this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

GENERAL

This document represents a new concept for BDSs, different from the other BDSs published by Working Group 9.

This is necessary, because it is related to non-finished products, where the customer is involved in their design, layout and specification. As a consequence, this BDS describes requirements for "tools" (e.g. for design, verification, test, and measurement), rather than requirements for components.

The application of this specification requires that the relevant process technology and the associated manufacturing line are already qualified.

The following information is given for guidance.

Scope

This BDS relates to Integrated Gate Arrays in accordance with IEC 748 : Semiconductor devices - Integrated circuits.

A gate array is a circuit having a design methodology based on a technological process and function library which elements have been prediffused. The set of such gate arrays shall be defined in terms of complexity:

- maximum number of equivalent gates
- maximum percentage of usable gates (where appropriate)
- die size
- I/O number.

Related documents

See 2.1 of CECC 90 100 and 2.2 of CECC 90 000.

Structure of Detail Specifications

Clause numbering of DSs shall be in accordance with that of this document.

Units, symbols and terminology

See 2.3 of CECC 90 100 and 2.3 of CECC 90 000.

Application of Quality Assessment Procedures

See 3 of CECC 90 100 and CECC 90 000.

1 GENERAL DESCRIPTION

1.1 Definition

- **TTV: Technology Test Vehicle:** (see CQC of ASF)
- **LTV: Library Test Vehicle:** the content and use of this vehicle are described in 2.3.
LTVs are intended for qualification of library cells and design tools.
- **CD: Demonstrator IC:** a circuit implemented with the gate array. The functions of this circuit are to be defined by the IC manufacturer. It is intended for performance evaluation by users.
- **CC: Customer circuit:** a circuit based on the gate array to implement customer circuits.

1.2 Technology

The technology employed shall either be defined in a Detail Specification (DS), or, where there is no suitable DS, by means of a concise description.

2 GENERAL DESCRIPTION OF THE ARRAYS AND TEST VEHICLE

2.1 Description of family, arrays, and/or demonstrators

The following shall be specified:

- power supplies and limiting conditions
- number of physical gates or cells
- number of usable gates or cells
- maximum dynamic power dissipation for the device and per MHz or per functional unit
- number of available buffers per output
- percentage or number of I/O buffers usable as output
- number of outputs which can be simultaneously switched under specified conditions (supply voltage, loading, etc.)
- for each array of a family:
 - 1) physical layout information including (where appropriate):
 - identification and position of power supply and ground pads
 - identification and position of special pads (oscillators, test pads, etc.)
 - position of the I/O stages
 - locations of active, and interconnection, zones
 - description of interconnection capability (number of levels, horizontal and vertical grids routing over active areas, etc.)
 - 2) locations of bus or other techniques for supply distribution and prohibited regions
 - 3) die size(s)
 - 4) packaging availability
 - 5) functional description of the test vehicle of customer circuits
 - 6) static characteristics: see library
 - 7) dynamic characteristics: see library and simulation.