

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC



Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION PARTICULIERE CADRE:

COMMUTATEURS ANALOGIQUES INTEGRES

Harmonized System of Quality Assessment for
Electronic Components

BLANK DETAIL SPECIFICATION:

INTEGRATED ANALOGUE SWITCHING CIRCUITS

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

VORDRUCK
FÜR BAUARTSPEZIFIKATION:

INTEGRIERTE ANALOGSCHALTER

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for INTEGRATED ANALOGUE SWITCHING CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly-sheet.

PREFACE

This blank detail specification (BDS) was prepared by CECC WG9 "INTEGRATED CIRCUITS".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 147 : Essential ratings and characteristics of semiconductor devices and general principles of measuring methods.

The text of this BDS was circulated to the CECC for voting in the document indicated below and was ratified by the President of the CECC for printing as a CECC Specification.

DocumentsDate of votingReport on the voting

CECC(Secretariat) 1405

August 1983

CECC(Secretariat) 1513

It is recognized that the layout proposed cannot apply to all detail specifications based on this document. For example when several similar devices are covered by the same detail specification, it may be convenient to give the limiting values in a table.

NOTICE

In accordance with the decision of the CECC Management Committee this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

1 Front page

The front page of the DS shall be laid out as shown on the following page.

The numbers between square brackets correspond to the following indications which shall be given :

Identification of the DS and of the component :

- [1] The name of the National Standards Organization under whose authority the DS is published and, if applicable, the organization from whom the DS is available.
- [2] The CECC Symbol and the CECC number allotted to the DS by the CECC General Secretariat.
- [3] The number and issue number of the CECC generic or sectional specification as relevant ; also national reference if different.
- [4] If different from the CECC number, the national number of the DS, date of issue and any further information required by the national system, together with any amendment numbers.
- [5] Type number, a short description of the type by :
 - function (for example single pole, double throw switch)
 - number of independent circuits per package
 - number and kind of inputs and outputs
 - material and type of construction (silicon, monolithic, multichip, bipolar, MOS)
 - performance, for example low resistance, high speed, low power consumption
 - electrostatic sensitivity (where appropriate).

[6] Information on typical construction (if applicable)

For [5] and [6] the text to be given in the DS should be suitable for an entry in CECC 00 200 or CECC 00 300.

[7] An outline drawing with main dimensions which are of importance for interchangeability, and/or reference to the appropriate national or international document for outlines. Alternatively, this drawing may be given in an appendix to the DS.

[8] Quality assessment level(s)

[9] Reference data giving information on the most important properties of the component, which allow comparison between the various component types intended for the same, or for similar, applications.

Identification of the component and supplementary information :

Description of the materials for the package (for example, glass, ceramic, silicone) and information relating to the mounting (welding, soldering), lead material and finish.

Inside the sketch of the package, the terminal connections to the inputs, outputs or other important points of the circuit shall be identified. This can be shown by a functional block diagram.

Description of the numbering of the terminals with the identification of pin number 1.

Marking on the device in accordance with the GS (see 2.5 of CECC 90 000).

Layout for front page of detail specification

Specification available from : [1]	CECC 90 203-xxx [2] E <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <tr> <td style="width: 20%; padding: 2px;">Page</td> <td style="padding: 2px;">Total number of pages :</td> </tr> </table>	Page	Total number of pages :
Page	Total number of pages :		
ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH : [3]	[4]		
OUTLINE AND DIMENSIONS [7] (First angle projection)	[5] [6] [8]		
[9]			
Information about manufacturers who have components qualified to this detail specification is available in the current CECC 00 200 : Qualified Products List.			

2 RATINGS (LIMITING VALUES) (Not for inspection purposes)

These apply over the operating temperature range, unless otherwise stated (see SS 90 200).

- | | | |
|------|---|------------|
| 2.1 | Maximum (and where appropriate minimum) value of voltage between the reference terminal and each other terminal. | |
| 2.2 | Any other limiting value(s) of voltage between any specified terminals as appropriate. | |
| 2.3 | Maximum continuous output current | I_O |
| 2.4 | Maximum continuous internal power dissipation with reference to a derating curve or factor related to the reference point temperature or ambient temperature, if appropriate maximum power dissipation per switch | P_D |
| 2.5 | Maximum pulsed analogue current | I_{peak} |
| 2.6 | Maximum and minimum ambient or reference point operating temperature | T_{amb} |
| 2.7 | Maximum and minimum storage temperature | T_{stg} |
| 2.8 | Any specific mechanical or environmental ratings peculiar to the device | |
| 2.9 | Any interdependence of limiting conditions | |
| 2.10 | Maximum value of short circuit time, where appropriate | t_{OS} |

3 RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS (Not for inspection purpose)

The following characteristics shall apply over the full ambient operating temperature range unless otherwise specified. Where the stated performance of the circuit varies over the ambient operating temperature range the values of the input and output voltages and their associated currents shall be stated at 25 °C and at the extremes of the operating temperature range.

Where it is necessary to use external elements to ensure stable operation of the switch, the values of the characteristics specified refer to the switch with such elements connected.

CHARACTERISTICS	SYMBOL	METHOD (See SS 90 200, 4.1.3)
3.1 Input voltage(s)	$V_I, V_i (V_S)$	
3.2 Output voltage	$V_O, V_o (V_D)$	
3.3 Output current	$I_O, I_o (I_D)$	
3.4 Low level control input current	I_{IL}	
3.5 High level control input current	I_{IH}	
3.6 Power supply currents (static conditions)	$I_S (I_{CC}, I_{DD}, I_{EE}, I_{GND} I_{REF})$	

CHARACTERISTICS	SYMBOL	METHOD (See SS 90 200 4.1.3)
3.7 Leakage current(s)	$I_{l(OFF)}$, $(I_{S(OFF)})$ $I_{O(OFF)}$, $(I_{D(OFF)})$ $I_{lO(ON)}$, $(I_{DS(ON)})$	
3.8 Switch-ON resistance	$R_{(ON)}$, $(R_{DS(ON)})$	S-02
3.9 OFF-STATE switch insulation (if applicable)	$a(OFF)$	S-03
3.10 Harmonic distortion (if applicable)	D	S-04
3.11 Crosstalk attenuation between any two channels (where appropriate)	a_{ct}	S-05
3.12 Feedthrough between control input and analogue output	ΔV_O	S-06
3.13 Turn-ON time	$t_{(ON)}$	S-07
3.14 Turn-OFF time	$t_{(OFF)}$	S-07
3.15 Transition time (if applicable)	t_T	S-07
3.16 Propagation time (if applicable)	t_P	S-07
3.17 MAKE-BEFORE-BREAK time (where appropriate)	t_{MBB}	S-08
3.18 BREAK-BEFORE-MAKE time (where appropriate)	t_{BBM}	S-08
		(See SS 90 200, 4.1.1)
3.19 Cut-off frequency (if applicable)	f_a , f_b	A-10

The following additional information shall be given as design data.

- 3.20 A graph, or graphs showing switching times against V_O and temperature.
- 3.21 A graph, or graphs showing a normalised supply current I_S against the switching frequency.
- 3.22 A graph showing $R_{(ON)}$ versus analogue input voltage V_i (if applicable)
- 3.23 A schematic diagram of the device shall be given, in the case of complex devices, a schematic for one typical channel may be given.

4 TEST CONDITIONS AND INSPECTION REQUIREMENTS

These are given in the following tables, where the values and exact test conditions to be used shall be specified as required in the detail specification relevant to a given type, in line with the indications given in CECC 90 200 for the relevant test.

NOTES : 1 - All tests are performed at $T_{amb.} = 25 \pm 5 \text{ }^{\circ}\text{C}$, unless otherwise prescribed.

2 - In the tables the paragraph numbers refer to the generic or sectional specifications with the following code :

G : Generic specification : Monolithic integrated circuits
(CECC 90 000, issue 2)

S1 : Sectional specification : Digital monolithic integrated circuits
(CECC 90 100, issue 2)

S2 : Sectional specification : Analogue integrated monolithic circuits
(CECC 90 200, issue 1)

Example : S2/4.2.2 = 4.2.2 of CECC 90 200.
or S2/S-07 = electrical test method n° 7 for an analogue switch

External elements necessary to ensure stable operation shall be specified and shall be connected for all electrical tests.

4.1 Explanation of quality assessment levels R, T and V.

See S2/5.7.1.

4.2 Key of abbreviations

See S2/5.7.2.

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
GROUP A INSPECTION : The following electrical inspection requirements shall be given. Additional characteristics to be inspected may be given for specific circuit(s) in accordance with 3 of this specification				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A1</u> Visual examination G/4.2.2	ND	See G/4.2.2	None	I	1,5	I	1,5	I	1,5
<u>Sub-group A2</u> Verification of the function Method S2/S-01	ND	Supply voltages and/or currents = specified values All input signals and resultant output levels as well as combina- tions necessary to verify the functional operation of the device shall be specified Loading conditions shall be specified Each switch shall be tested in turn	S2/4.1.3	II	0,15	II	0,25	II	0,25
<u>Sub-group A3</u> Static characteristics at 25 °C	ND		-	II	0,65	II	0,65	II	0,65
Low level control input current I_{IL} Method S1/4.1.2(3)		Supply voltages as specified Control input voltage = V_{ILA} Each control input shall be tested in turn	I_{ILA}						
High level control input current I_{IH} Method S1/4.1.2(4)		Supply voltages as specified Control input voltage = V_{IHB} Each control input shall be tested in turn	I_{IHA}						
Positive supply current $I_{S(1)}$ (or I_{CC}) (if applicable) Method S1/4.1.6(1)		Supply voltages as specified Control input voltages as specified	$I_{S(1)A}$ (or I_{CCA})						

EXAMINATION OR TEST	D NO	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A3 (contd)</u>									
Negative supply current $I_{S(2)}$ (or I_{EE}) (if applicable) Method S1/4.1.6(1)		Supply voltages as specified Control input voltages as specified	$I_{S(2)}A$ (or $I_{EE}A$)						
Logic supply current $I_{S(3)}$ (or I_L) (if applicable) Method S1/4.1.6(1)		Supply voltages as specified Control input voltages as specified	$I_{S(3)}A$ (or $I_{LA}A$)						
Reference or ground supply current $I_{S(4)}$ (or I_{REF} or I_{GND}) (where appropriate) Method S1/4.1.6(1)		Supply voltages as specified Control input voltages as specified	$I_{S(4)}A$ (or I_{REFA} or I_{GNDA})						
Switch input (source) (OFF) leakage current $I_{I(OFF)}$ (or $I_{S(OFF)}$) Method S1/4.1.8		Supply voltages as specified Analogue voltage(s) as specified The sequence and com- bination of control input signals necessary to turn OFF the measured channel shall be specified Each switch shall be tested in turn	$I_{I(OFF)}A$ (or $I_{S(OFF)}A$)						
Switch output (drain) (OFF) leakage current $I_{O(OFF)}$ (or $I_{D(OFF)}$) Method S1/4.1.8		Supply voltages as specified Analogue voltage(s) as specified The sequence and com- bination of control input signals necessary to turn OFF the measured channel shall be specified Each switch shall be tested in turn	$I_{O(OFF)}A$ (or $I_{D(OFF)}A$)						

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A3 (contd)</u>									
Switch on leakage current $I_{IO(ON)}$ (or $I_{DS(ON)}$) Method S1/4.1.8		Supply voltages as specified Analogue voltage(s) as specified The sequence and com- bination of control input signals necessary to turn ON the measured channel shall be specified Each switch shall be tested in turn	$I_{IO(ON)A}$ (or $I_{DS(ON)A}$)						
Switch-ON Resistance $R_{(ON)}$ or $(R_{DS(ON)})$ Method S2/S-02		V_{CC} , V_{EE} as specified V_{IN} shall be speci- fied stating the levels of channels V_{REF} (or V_{GND}) = 0 V V_L , V_D as specified I_S as specified Each switch shall be tested in turn	$R_{(ON)A}$ (or $R_{DS(ON)A}$)						
<u>Sub-group A4a</u> Static characteristics at maximum operating temperature As in sub-group A3	ND	$T = T_{amb} \text{ max.}$ Electrical conditions as for sub-group A3	Limits may be different from those in sub-group A3	S4	1,0	na	na	na	na
<u>Sub-group A4b</u> Static characteristics at minimum operating temperature As in sub-group A3	ND	$T = T_{amb} \text{ min.}$ Electrical conditions as for sub-group A3	Limits may be different from those in sub-group A3	S4	1,0	na	na	na	na
<u>Sub-group A5</u> Dynamic characteristics at 25 °C	ND			S4	1,5	S4	2,5	na	na
Frequency of signal being switched (cut-off frequencies) f_a , f_b (if applicable) Method S2/A-10		Supply voltages as specified Amplitude of analogue input signals as spe- cified Output load impedance as specified Each channel shall be tested in turn	f_{aB} , f_{bA}						

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A5 (contd)</u> SWITCH-OFF isolation $a_{(OFF)}$ (if applicable) Method S2/S-03		Supply voltages as specified Amplitude and frequen- cy of analogue input signal as specified Output load impedance as specified Each channel shall be tested in turn	$a_{(OFF)B}$						
Harmonic distortion of analogue signal D (if applicable) Method S2/S-04		Supply voltages as specified Amplitude and frequen- cy of analogue input signal as specified Output load impedance as specified Each channel shall be tested in turn	D_A						
Crosstalk attenuation between any two switched ON channels $a_{ct(1)}$ (where appropriate) Method S2/S-05		Supply voltages as specified Amplitude and frequen- cy of analogue input signal as specified Input and output networks as specified All combinations of channels shall be tested in turn	$a_{ct(1)B}$						
Crosstalk attenuation between a switched ON channel and a switched OFF channel $a_{ct(2)}$ (where appropriate) Method S2/S-05		Supply voltages as specified Amplitude and frequen- cy of analogue input signal as specified Input and output networks as specified All combinations of channels shall be tested in turn	$a_{ct(2)B}$						

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A5 (contd)</u> Feedthrough between control input and an analogue output ΔV_O Method S2/S-06		Supply voltages as specified Input and output networks as specified Characteristics of control input pulse as specified Each channel shall be tested in turn	ΔV_{O1A} ΔV_{O2A}						
TURN ON time $t_{(ON)}$ Method S2/S-07		Supply voltages as specified Amplitude and frequen- cy of analogue input voltage as specified Input and output networks as specified Characteristics of control input pulse as specified Each channel shall be tested in turn	$t_{(ON)A}$ $t_{(ON)B}$						
TURN OFF time $t_{(OFF)}$ Method S2/S-07		Supply voltages as specified Amplitude and frequen- cy of analogue input voltage as specified Input and output networks as specified Characteristics of control input pulse as specified Each channel shall be tested in turn	$t_{(OFF)A}$ $t_{(OFF)B}$						

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A5 (contd)</u> Transition times t_{THL} , t_{TLH} (if applicable) Method S2/S-07		Supply voltages as specified Amplitude and frequency of analogue input voltage as specified Input and output networks as specified Characteristics of control input pulse as specified Each channel shall be tested in turn	t_{THLA} t_{TLHA}						
Propagation times t_{PHL} , t_{PLH} (if applicable) Method S2/S-07		Supply voltages as specified Amplitude and frequency of analogue input voltage as specified Input and output networks as specified Characteristics of control input pulse as specified Each channel shall be tested in turn	t_{PHLA} t_{PLHA}						
MAKE-BEFORE-BREAK time t_{MBB} (where appropriate) Method S2/S-08		Supply voltages as specified Amplitude and frequency of analogue voltage at each channel input as specified Input and output networks as specified Characteristics of control input pulse as specified All specified combinations of channels shall be tested	t_{MBBA} t_{MBBB}						

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
				ASSESSMENT LEVELS					
				R		T		V	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-group A5 (contd)</u> BREAK-BEFORE-MAKE time t_{BBM} (where appropriate) Method S2/S-08		Supply voltages as specified Amplitude and frequen- cy of analogue voltage at each channel input as specified Input and output networks as specified Characteristics of control input pulse as specified All specified combina- tions of channels shall be tested	t_{BBMA} t_{BBMB}						
GROUP B INSPECTION : See S2/5.7									