

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

**Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques**

SPEZIFICATION INTERMEDIAIRE:

**CIRCUITS INTEGRES
MONOLITHIQUES
D'INTERFACE**

**Harmonized System of Quality Assessment for
Electronic Components**

SECTIONAL SPECIFICATION:

**INTERFACE MONOLITHIC
INTEGRATED CIRCUITS**

**Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik**

RAHMENSPEZIFIKATION:

**INTEGRIERTE
ANPASSUNGS-
SCHALTUNGEN**



2 Edition
Issue
Ausgabe

CECC 90 300

1987

Documents



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Dieses blaue Blatt ist nach dem Titelblatt der CECC 90 300 Ausgabe 2 (1987) einzufügen

This blue page shall be inserted after the title page of CECC 90 300 Issue 2 (1987)

Cette page bleue doit être insérée après la page de garde de la CECC 90 300 Edition 2 (1987)

ÄNDERUNG 1 ZU CECC 90 300 (Ausgabe 2)

AMENDMENT 1 TO CECC 90 300 (Issue 2)

AMENDEMENT 1 A LA CECC 90 300 (Edition 2)

RAHMENSPEZIFIKATION

SECTIONAL SPECIFICATION

SPECIFICATION INTERMEDIAIRE

INTEGRIERTE ANPASSUNGS-SCHALTUNGEN

INTERFACE MONOLITHIC INTEGRATED CIRCUITS

CIRCUITS INTEGRES MONOLITHIQUES D'INTERFACE

EIN DEUTSCHER TEXT LIEGT NICHT VOR

The following amendments shall be made :

Les modifications suivantes doivent être effectuées :

1) Replace pages 1/2 with new pages 1/2 "Contents".

1) Remplacer les pages 1/2 par les nouvelles pages 1/2 "Sommaire".

2) Page 5 - Clause 1 - Scope, delete the fourth line :

2) Page 5 - Paragraphe 1 - Domaine d'application, 3ème ligne, supprimer :

"- structural similarity procedures".

"les procédures d'associations de modèles,".

3) Pages 7/8 - Clause 3.1 - Structurally similar circuits

3) Pages 7/8 - Paragraphe 3.1 - Modèles associables

Keep the title and delete the rest of paragraph 3.1 because all material necessary to define structural similarity in all cases is included in 3.2 of CECC 90 000.

Conserver le titre et supprimer le reste du paragraphe puisque toutes les informations concernant les procédures d'associativité sont contenues en 3.2 de la CECC 90 000.

4) Replace pages 13/14 with new pages 13/14.

4) Remplacer les pages 13/14 par les nouvelles pages 13/14.

5) Replace page 17 with new page 17.

5) Remplacer la page 17 par la nouvelle page 17.

6) Delete pages 18 to 26; paragraph 5.7 related to test sequences has to be deleted because the test sequences are now introduced in the Generic Specification CECC 90 000.

6) Supprimer les pages 18 à 26; le paragraphe 5.7 concernant les séquences d'essais doit être supprimé car celles-ci sont introduites dans la Spécification Générique CECC 90 000.

CECC 90 300 Ausgabe 2 Änderung 1 1994

CECC 90 300 Issue 2 Amendment 1 1994

CECC 90 300 Edition 2 Amendement 1 1994



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- B L A N K P A G E -

FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for INTERFACE MONOLITHIC INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly sheet.

PREFACE

This sectional specification (SS) was prepared by CECC WG 9 "Integrated circuits".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747 : Semiconductor devices : Discrete devices and Integrated circuits, IEC 748 : Semiconductor devices : Integrated circuits, IEC 749 : Semiconductor devices : Mechanical and climatic test methods.

The text of this second issue consists of the text of CECC 90 300 Issue 1 (1985) amended in accordance with the ratified new material introduced by the following document.

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat)1946	September 1986	CECC(Secretariat)2009

In accordance with the decision of the CECC Management Committee this specification is published initially in French and English. The German text will follow as soon as it has been prepared.

EFFECTIVE DATE

This second issue shall become effective for all new qualification approvals from 15 June 1987.

Issue 1 will remain valid for existing qualification approvals until further notice, but it is recommended that current qualifications should be modified in accordance with Issue 2 during a transition period of 2 years.

SCOPE

This specification applies to interface monolithic integrated circuits examples of which are listed in 4.1 and shall be read in conjunction with CECC 90 000.

It defines :



- electrical measurement methods
- electrical endurance tests.

The common blank detail specification (BDS), contained in this SS, comprises those requirements which are common for all interface circuits.

2 GENERAL

2.1 Related documents

In each case the latest issue of the documents prior to the date of issue of this document is valid.

IEC 148 : Letter symbols for semiconductor devices and integrated microcircuits. (Chapter XI).

IEC 617 : Graphical symbols for diagrams.

IEC 617-12 : Part 12 : Binary logic elements

IEC 617-13 : Part 13 : Analogue elements.

IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

IEC 747-1 : Part 1 : General.

IEC 747-10 : Part 10 : Generic specification for discrete devices and integrated circuits.

IEC 748 : Semiconductor devices - Integrated circuits.

IEC 748-1 : Part 1 : General.

IEC 748-2 : Part 2 : Digital integrated circuits.

IEC 748-3 : Part 3 : Analogue integrated circuits.

IEC 748-4 : Part 4 : Interface integrated circuits.

CECC 90 000 : GS : Monolithic integrated circuits.

CECC 90 100 : SS : Digital monolithic integrated circuits.

CECC 90 200 : SS : Analogue monolithic integrated circuits.

2.2 Preferred voltages for interface monolithic integrated circuits.

Preferred values are given in IEC 748-1, Chapter VI, sub-clause 6.1.b for analogue part of the device.

Preferred values are given in sub-clause 2.2 of 90 100 for digital part of the device.

2.3 Symbols and terminology.

2.3.1 Letter symbols

The letter symbols shall be used in accordance with IEC 148, Chapter X and XI.

To indicate a defined value of an electrical quantity denoted by a basic letter, the following system shall be used :

- A for the most positive (least negative) value of the range.
- B for the least positive (most negative) value of the range.

Examples (see Fig. 1).

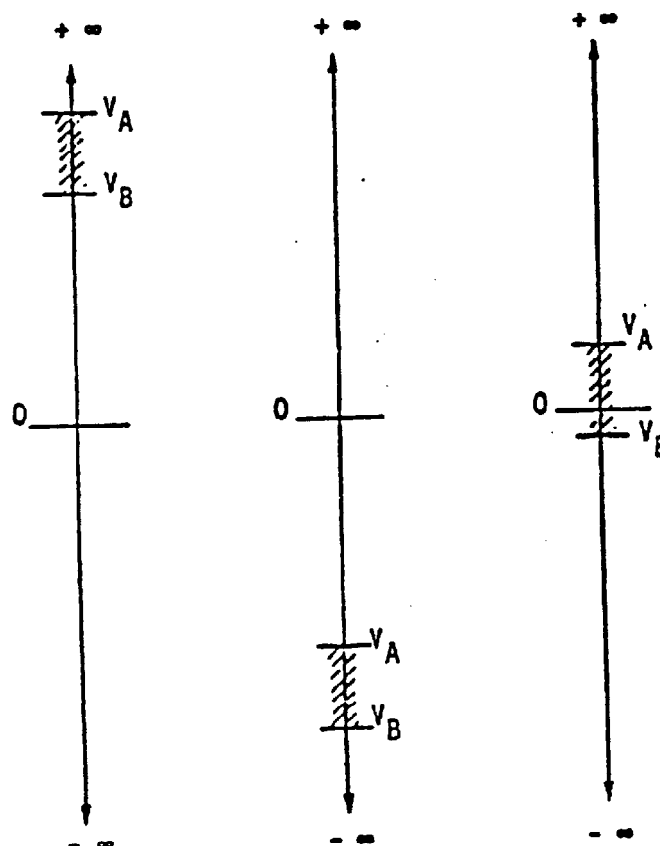


Fig. 1

2.3.2 Graphical symbols

Graphical symbols shall be used in accordance with IEC 617-12 and 617-13.

2.3.3 Terminology

For terminology, IEC 748-1 shall be used, and in particular Chapter IV.

QUALITY ASSESSMENT PROCEDURES

1 Structurally similar circuits (see 3.2 of CECC 90 000)



3.1.1 For testing of Sub-Groups :

- B1 - dimensions
- B2 - solderability
- C1 - dimensions not included in B1
- C2 - immersion in cleaning solvents
- C3 - robustness of terminations
- C13 - salt mist

The devices are structurally similar provided that they have identical packages, and that they come from the same assembly and encapsulation line using the same assembly techniques and piece parts.

3.1.2 For testing of Sub-Groups :

- B3 - sealing test
- B4 - change of temperature
- C4 - resistance to soldering heat followed by change of temperature
- C5 - shock, vibration, acceleration
- C6, C7 - damp heat, steady state

The devices are structurally similar provided that they have identical packages, and that they come from the same assembly and encapsulation line using the same assembly techniques and piece parts and that the maximum ratio in chip area shall not exceed 2.

3.1.3 For testing of Sub-Groups :

- B5 - electrical endurance (168 h)
- C8 - electrical endurance (1 000 h or 2 000 h)

Note : Test duration 1 000 h, or 2 000 h if prescribed by the DS.

The devices are structurally similar even if the chip lay-out differs, provided that all the following criteria are satisfied :

- they operate at the same recommended operating voltage(s) applied to equivalent terminal(s) including "open-terminal" (for example open collector or drain) devices and a power dissipation within a 20 % range ;
- they have been designed to the same design rules ;
- they have been manufactured on the same production line including identical packages, using the same technical processes starting from the primary stage ;
- the devices with the highest power dissipation and recommended operating temperature shall be chosen.

3.1.4 For testing of Sub-Groups :

C9 - storage, dry heat
C10 - storage, cold

The devices are structurally similar provided that all the following criteria are satisfied :

- they have been designed to the same design rules ;
- they have been manufactured on the same production line including identical packages, using the same technical processes starting from the primary stage.

3.1.5 For testing of Sub-Group D1 - electrical endurance (8 000 h)

Integrated circuits produced concurrently in the same production line up to and including final sealing in their encapsulations using the same types of machines and apparatus and using the same integrated circuit design rules may be grouped together for the purpose of obtaining samples. The claim for grouping shall be declared in the qualification approval test report to the satisfaction of the ONS.

Integrated circuits may be grouped together for the purpose of obtaining samples for electrical endurance tests under the same or similar test conditions, provided that the same basic design rules (for example, element geometry, spacing, thickness of the chip, etc.) and internal sub-circuits (for example, multi-emitter input, phase splitter, totem pole output, etc.) are used.

When the above conditions apply, manufacturers may take a single sample of any one type to assess the lot if it can be demonstrated to the satisfaction of the ONS that the characteristic(s) being tested are not significantly dependent upon the selection. If there is a significant difference, the type selected for the common electrical endurance tests shall be represented by the more complex circuit or that with a critical rating giving the greatest risk of failure.

3.2 Certified test records

Certified test records shall give the following information, unless otherwise specified :

- attributes information for tests in Sub-Groups : B2, B3, B4, B5, C3, C4, C5, C6, C7, C8, C9, C10 ;
- measurement information before and after endurance test : C8 and D1.



TEST AND MEASUREMENT PROCEDURES

Electrical measurement procedures (see 4.1 and 4.5 of CECC 90 000)

The procedures apply to line transmitters, line receivers, sense amplifiers, peripheral drivers and level shifters, voltage comparators.

1.1 Measuring methods common to digital circuits

(1) IEC methods :

The hereafter listed electrical measuring methods, with reference to the relevant IEC documents, shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters Designation	Symbol	IEC 748-2	
			Chapter IV Clause n°	Section 3 Method n°
D-01	Total current drawn from the power supplies under dynamic conditions		1	1
D-02	Power supplied through the clock line		2	2
D-03	Input and output impedances : Current measurements : input and output capacitances for large signal operation		3.1	6
D-04	Input and output impedances : Voltage measurement : equivalent input and output capacitances, equivalent input and output resistances : Large signal method Bridge method (small signal)		3.2 3.2.1 3.2.2	11
D-05	Propagation times : Bipolar circuits (active load networks)	t_p	4.1.1	3
D-06	Propagation times : MOS circuits (passive load networks)	t_p	4.1.2	7
D-07	Delay and transition times : Bipolar circuits	t_D, t_T	4.2.1	4, 5
D-08	Transition times : MOS circuits	t_T	4.2.2	5
D-09	Set up and hold times	t_{su}, t_h	4.3	8, 9
D-10	Resolution time	t_{res}	4.4	36
D-11	Switching frequency of a sequential circuit		5	10
			Chapter IV	Section 2
D-12	Static characteristics : Output voltages		1	37
D-13	Static characteristics : Input currents		2	38



(2) CECC Methods :

The hereafter listed electrical measuring methods, with reference to the relevant CECC documents, shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters		CECC 90 100	
	Designation	Symbol	Sub-clause	Method
D-14	Propagation time : Bipolar circuits (passive load network)	t_p	4.1.3(2)	1
D-15	Output short circuit current	I_{OS}	4.1.4	
D-16	Breakdown voltage	$V_{(BR)}$	4.1.5	A, B
D-17	Transient energy rating		4.1.9	

1.2 Measuring methods common to analogue circuits

(1) IEC methods :

The hereafter listed electrical measuring methods, with reference to the relevant IEC documents, shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters Designation	Symbol	IEC 748-3	
			Chapter IV Clause n°	Section 2 Method n°
A-01	Power supply currents	I_S	2	22
A-02	Full signal input impedance	Z_i	3	23
A-03	Output impedance	Z_o	4	24
A-04	Input offset voltage of a differential input integrated linear amplifier and	V_{IO}	5	25, 26
	Bias voltage of a single-ended input integrated linear amplifier	V_{IB}		
A-05	Input offset current	I_{IO}	6	27
A-06	Input bias current	I_{IB}	7	28
A-07	Input offset voltage temperature coefficient	α_{VIO}	8	29
A-08	Input offset current temperature coefficient	α_{IIO}	9	30
A-09	Open-loop voltage amplification	A_v	10	31
A-10	Cut-off frequency (frequencies)	f_a, f_b	11	32
A-11	Common mode rejection ratio	k_{CMR}	12	33
A-12	Supply voltage rejection ratio	k_{SVR}	13	34
A-13	Output voltage range for differential amplifiers (d.c. measurement only)	V_{OPP}	14	35
A-14	Response times		15	39
	delay time	t_d		
	rise time	t_r		
	fall time	t_f		
	ripple time	t_{rip}		
	total response time	t_{tot}		

(2) CECC methods

The hereafter listed electrical measuring methods, with reference to the relevant CECC document, shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters		CECC 90 200
	Designation	Symbol	Clause n°
A-15	Noise measurements		A2.1
	noise voltage	V_n	
	noise current	I_n	
	and burst noise	V_{br}	
A-16	Average rate of change of the output voltage (Slew-rate)	S_{VOAV}	A2.2

4.1.3 Specific method for interface circuits

(1) IEC methods

The hereafter listed electrical measuring methods, with reference to the relevant IEC documents, shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters		IEC 748-4 *	
	Designation	Symbol	Chapter IV Section 2 Category Clause n°	Method n°
I-01	Common mode input triggering voltage <u>or</u>	V_{ICT}	1	61
	Common mode input voltage range	V_{IC}		
I-02	Average bias current <u>and</u>	I_{IB}	2	62
	Input offset current	I_{IO}		
I-03	Differential mode input overload recovery time <u>and</u>	t_{ord}	3	63
	Common mode input overload recovery time	t_{orc}		

(2) Additional methods

The hereafter listed electrical measuring methods shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters		Annex A
	Designation	Symbol	Clause n°
I-04	Differential input voltage range <u>and</u>	V_{ID}	A2.1
	Differential input threshold voltage	V_{IDT}	

* To be published : document 47A(Central Office)95, paragraph n° 1 to 3.



4.2 Electrical endurance testing

See GS/4.8.

5 COMMON BLANK DETAIL SPECIFICATION FOR INTERFACE MONOLITHIC INTEGRATED CIRCUITS

5.1 Introduction

The blank detail specification given in this section describes the requirements for technical content and format of DS for devices intended to be CECC approved, except that, in particular conditions described below, the requirements are included in, and may be modified by, a particular BDS which shall be published separately.

