

Description of a parametrized European mini test chip

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Committees responsible for this Draft for Development

The preparation of this Draft for Development was entrusted to Technical Committee GEL/93, Design automation, upon which the following bodies were represented:

- British Aerospace plc
- Department of Trade and Industry
- Federation of the Electronics Industry
- Institution of Electrical Engineers
- Manchester Metropolitan University
- University of Manchester
- University of Southampton

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National foreword

This Draft for Development has been prepared by Technical Committee GEL/93 and is the English language version of European Prestandard ENV 50218:1996 *Description of a parametrized European mini test chip* published by the European Committee for Electrotechnical Standardization (CENELEC).

The document is part of a series of six closely-related documents describing a technology assessment cycle of submicron CMOS technologies. The other five cover:

- steps and objectives of the assessment cycle;
- transistor model relating to the effects of submicron CMOS technologies;
- test structures for the extraction of MOS transistor parameters;
- documentation of the extraction of the model parameters;
- a data exchange format which can be used with existing data evaluation programs.

This publication is not to be regarded as a British Standard.

It is being issued in the Draft for Development series of publications and is of a provisional nature. It should be applied on this provisional basis so that information and experience of its practical application may be obtained.

Comments arising from the use of this Draft for Development are requested so that UK experience can be reported to the European organization responsible for its conversion to a European Standard. A review of this publication will be initiated 2 years after its publication by the European organization so that a decision can be taken on its status at the end of its three-year life. The commencement of the review period will be notified by an announcement in *BSI News*.

According to the replies received by the end of the review period, the responsible BSI Committee will decide whether to support the conversion into a European Standard, to extend the life of the prestandard or to withdraw it. Comments should be sent in writing to the Secretary of BSI Technical Committee GEL/93 at 389 Chiswick High Road, London W4 4AL giving the document reference and clause number and proposing, where possible, an appropriate revision of the text.

Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the ENV title page, pages 2 to 16, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

English version

Description of a parametrized European mini test chip

Description d'un mini composant européen
paramétrisable de test

This European Prestandard (ENV) was approved by CENELEC on 1995-10-16 as a prospective standard for provisional application. The period of validity of this ENV is limited initially to three years. After two years the members of CENELEC will be requested to submit their comments, particularly on the question whether the ENV can be converted into a European Standard (EN).

CENELEC members are required to announce the existence of this ENV in the same way as for an EN and to make the ENV available promptly at national level in an appropriate form. It is permissible to keep conflicting national standards in force (in parallel to the ENV) until the final decision about the possible conversion of the ENV into an EN is reached.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

This European Prestandard was prepared by CENELEC Technical Committee TC 217, Electrical Design Automation.

The text of the draft was submitted to the CENELEC members for comments and was approved as ENV 50218 during the CLC/TC 217 meeting on 1995-10-16.

The following date was fixed:

- latest date by which the existence of the ENV has be to announced at national level (doa) 1996-04-01

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1 Introduction

This document is part of a series of documents describing a technology assessment cycle of submicron CMOS technologies. The series consists of six closely related documents [1, 2, 3, 4, 5] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle¹⁾ is the contents of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS technologies is presented in [2]. Test structures usable for the extraction of MOS transistor parameters are described in this document. The documentation of the measurements of these test structures is the objective of [3]. The document [4] contains the techniques used for the extraction of transistor model parameters. The purpose of document [5] is the presentation of a data exchange format which can be used with existing data evaluation programs. The test structures of the European Mini Test Chip (ETC) are developed in co-operation with the participants of the ESPRIT projects *ADCIS*, *APBB*, *CANDI*, *ACCESS* and the JESSI *Joint European Submicron Silicon Initiative* projects *Joint Logic* and *Technology Assessment*.

The test structures are implemented and verified as a part of the work of the JESSI AC 41 consortium²⁾. The usefulness of the test structures of the European Mini Test Chip documented here were verified by means of three JESSI test chips. The European Mini Test Chip is processed with at least five different CMOS technologies and one BiCMOS technology of the JESSI AC 41 and JESSI Joint Logic projects. The feature sizes of the CMOS technologies range from $0.8\ \mu\text{m}$ down to $0.5\ \mu\text{m}$. The feature size of the BiCMOS technology is $0.8\ \mu\text{m}$. Additionally, the test structures were implemented into in-house chips which are not part of the JESSI projects. Consequently, the base of the verification of the test structures is even wider than the three (grand) JESSI test chips indicate.

1.1 Scope

This publication documents the parameterized MOS test structures of the device model **Parameter extraction Test Chip** (PTC) of the **European Mini Test Chip** (ETC). The devices of the PTC are a subset of the devices of the ETC. The modules of the ETC provide a minimum set of test structures used to characterize a MOS technology. The test structures of the ETC are generated automatically by a computer program for a given MOS technology. The program also generates test structures which are designed to characterize reliability aspects of a MOS technology (**Reliability Test Chip, RTC**) [6, 7, 8].

2 Basic Modules

The modular concept of the ETC gives the possibility to arrange subsets of the modules of the ETC within Process Control Monitors (PCM) and other supplier specific test chips. The test structures of the ETC can be used as scribe lane inserts by replacing the standard pad group of the ETC (see section 2.1). The test structures of the modules of the ETC are implemented into a CAD (Computer Aided Design) program. This program is named *Parametric Test structure Generator (PTG) System*. By means of the PTG program the test structures are automatically generated for different CMOS processes and different technology generations. The program generates the test structures including the connections to the standard pad group by means of a rule file which contains the design rules of the given CMOS technology. The test structures generated this way can be included into any test chips. In addition, the test structures can be utilized for *scribe lane inserts*. The standard pad group has to be replaced by a special pad group which is adapted for the use with scribe lanes.

¹⁾ The Technology Assessment Support Center (TASC) provides detailed informations about the computer programs which support the measurement and extraction routines. Send a FAX or an E-Mail to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart
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E-Mail: tasc@svlsi1.mikro.uni-stuttgart.de

²⁾ This work is part of the JESSI Program "Application"-Project AC 41 "Technology Assessment" and is sponsored by the national Public Authorities of Belgium, France, and Germany.