

Performance guide for single- and double-sided flexible printed wiring boards

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National foreword

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A review of this Draft for Development will be carried out not later than 3 years after its publication.

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Observations which it is felt should receive attention before the official call for comments will be welcomed. These should be sent to the Secretary of the responsible BSI Technical Committee at British Standards House, 389 Chiswick High Road, London W4 4AL.

The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic assembly technology.

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printed wiring boards**



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PERFORMANCE GUIDE FOR SINGLE- AND DOUBLE-SIDED FLEXIBLE PRINTED WIRING BOARDS

1 Scope

This PAS provides the requirements for the single- and double-sided flexible printed wiring boards (hereinafter designated as "flexible printed board" or FPC).

In this document, an FPC means a single- or double-sided FPC prepared by lamination of a film of polyester or polyimide with copper foil(s) on one or both sides of a board including the type with no adhesive layer, and with conductor pattern formed by the subtractive method (etching of the copper foil), or possibly by the build-up method.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60326-7:1981, *Printed boards – Part 7: Specification for single- and double-sided flexible printed boards without through connections*

IEC 60326-8:1981, *Printed boards – Part 8: Specification for single- and double-sided flexible printed boards with through connections*

JPCA-TD01:2000, *Terms and definitions for printed circuits*

JPCA-BM03:2003, *Flexible printed wiring boards (adhesive and adhesiveless types)*

JIS C 5016:1994, *Test methods for flexible printed wiring boards*

JIS C 5017:1994, *Single- and double-sided flexible printed wiring boards*

JIS C 5603:1993, *Terms and definitions for printed circuits*

JIS C 6471:1995, *Test methods of copper-clad laminates for flexible printed wiring boards*

JIS C 6472:1995, *Copper-clad laminates for flexible printed wiring boards (polyester film, polyimide film)*

JIS C 6515:1998, *Copper foil for printed wiring boards*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in JIS C 5603, JIS C 5017, JIS C 5016, and JPCA-FC03 apply.

4 Test methods

The test methods used in this document as specified below shall be in conformance with JIS C 5016.

- a) Test methods requiring complicated referencing procedures are reproduced in this document.
- b) Tests on through connection apply only to double-sided FPCs.

- c) External appearance is the only requirement specified in this document for stiffeners affixed to FPCs.

5 Performance levels

The FPCs are classified into three levels, Levels 1, 2, and 3, and an additional special level, Level X, for applications requiring special attention. They are defined as:

Level 1 – FPCs requiring "ordinary" performance;

Level 2 – FPCs requiring "high" performance;

Level 3 – FPCs requiring "extra-high" performance;

Level X – FPCs requiring special performances which do not belong to the above-mentioned three levels, and the specifications requiring an agreement between user and supplier.

A relevant level of the board is chosen for a specific application of the board. A different level can be selected for a specific section of the board when the required specification of the section is different from that of another part of the board.

6 Base materials

The base materials used in FPCs shall satisfy the requirements specified in JPCA-BM03.

7 Visual inspection

7.1 Test environment

The test environment shall meet the requirements of JIS C 5016, Clause 3.

7.2 Test specimens

The test specimens shall meet the requirements of JIS C 5016, Clause 4.

7.3 Tools for testing

A magnifying glass having a magnification of 3× to 10× shall be used for examining the appearance and the surface finish conditions of the product. Dimensions shall be measured with a scaled magnifying glass or an instrument capable of two-dimensional coordinate measuring, if necessary. Thickness shall be measured with a micrometer having an accuracy of 1 µm or better.

7.4 Preparation of limit samples

Limit samples showing the required criteria to make technical judgments may be prepared under agreement between user and supplier for the application of this document.

7.5 Description of inspection

Requirements, procedures, and illustration for visual inspections are given in 7.5.1 through 7.5.6. Requirements that are not designated for a specific performance level shall apply to all the performance Levels 1, 2 and 3.

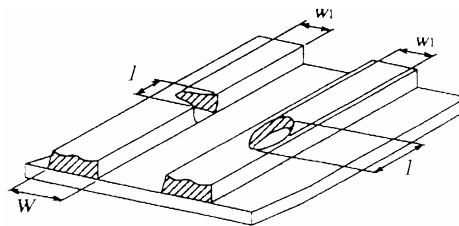
7.5.1 Visual inspection of conductor

7.5.1.1 Open and short circuit

There shall be no open and/or short circuit on FPCs.

7.5.1.2 Nicks and pinholes on conductor

- a) The allowable width (w_1) and length (l) of a nick and a pinhole of the conductor reducing conductor width, as shown in Figure 1, shall meet the requirement given in Table 1 for the finished conductor width (W) (see Note 1).



NOTE 1 The width of the finished conductors should be measured at the bottom of the conductor.

Figure 1 – Nicks and pinholes in conductor

Table 1 – Allowable nicks and pinholes

Level	Nicks and pinholes
1 and 2	$w_1 \leq 1/2 W$ $l \leq 2 W$
3	$w_1 \leq 1/3 W$ $l \leq W$

- b) The void area on a land, as illustrated in Figure 2, shall not exceed 10 % of the effective exposed land area.

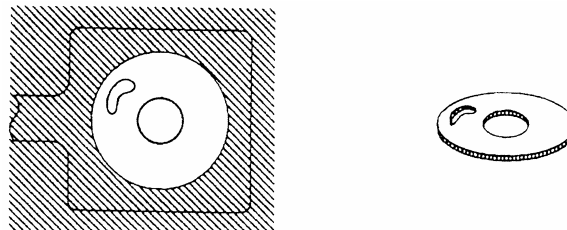


Figure 2 – Reduced area on land

- c) The circumferential void of a lead insertion hole, as illustrated in Figure 3, shall not exceed one-third of the total circumference.

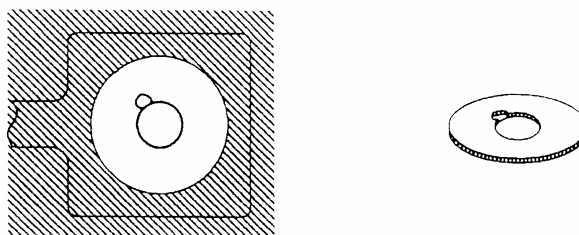


Figure 3 – Circumferential void at the component hole

7.5.1.3 Distance between conductor/spur and nodule of conductor

The distance (s_1) or ($s_2 + s_3$) in Figure 4 relative to the finished conductor spacing(s) shall meet the requirement given in Table 2.

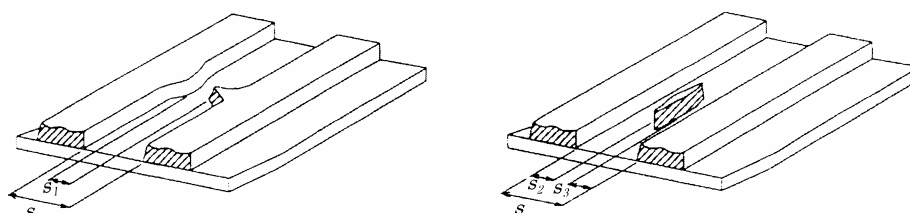


Figure 4 – Unnecessary copper between conductor/spur and nodule of conductor

Table 2 – Allowable unnecessary copper, spur and nodule between conductors

Level	Unnecessary copper, spurs and nodules, s_1 or ($s_2 + s_3$)
1 and 2	$1/2 s_1 \leq a$ or ($s_2 + s_3$)
3	$2/3 s_1 \leq a$ or ($s_2 + s_3$)

7.5.1.4 Unnecessary copper between conductor/spur and nodule of conductor in an open area

The spacing(s) between the board edges and the unnecessary copper or spur and nodule shall be larger than 0,125 mm in an open area where no conductor pattern is routed, as illustrated in Figure 5. The spacing(s) between the board edge and the unnecessary copper or spur and nodule shall be larger than 0,125 mm. The open area as stated in this clause shall have a width of no less than 0,375 mm.

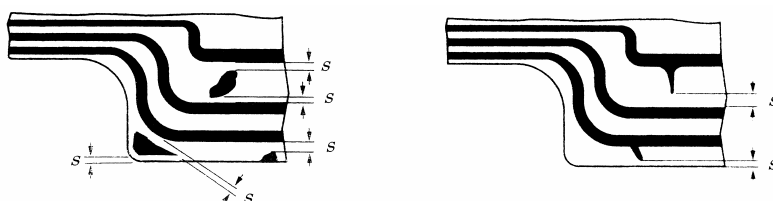


Figure 5 – Unnecessary copper, spurs and nodules in an open area and nodules of conductor corners

7.5.1.5 Etched concave surface of the conductor

Etched concave surface (d) of the conductor relative to the conductor thickness (t), as illustrated in Figure 6, shall meet the requirement given in Table 3. The concave surface shall not run across the entire width of a conductor.

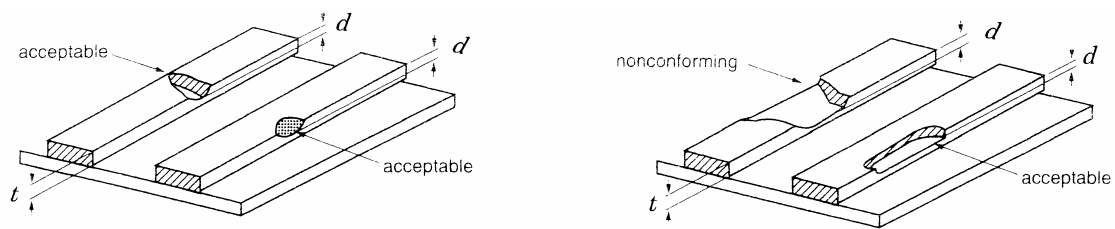


Figure 6 – Etched concave surface of the conductor and nodule at a conductor corner

Table 3 – Allowable etched concave of the surface conductor

Level	Etched concave surface of the conductor, d (t : conductor thickness)
1 and 2	$d \leq 1/3 t$
3	$d \leq 1/5 t$

7.5.1.6 Conductor delamination

The width (w_1) and length (l) of conductor delamination relative to the finished conductor width (W), as illustrated in Figure 7, shall meet the requirement given in Table 4.

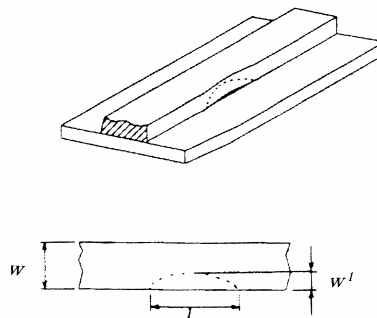


Figure 7 – Conductor delamination

Table 4 – Allowable conductor delamination

Level	Conductor delamination, length (l), width (w_1)
1	Coverlay laminated area $l \leq W$ and $w_1/W \leq 1/3$ for flexing area $l \leq W$ and $w_1/W \leq 1/2$ for other area
	No coverlay laminated area $l/W \leq 1/4$ and $w_1/W \leq 1/4$
2 and 3	There shall be no delamination in the conductor which can be observed by the naked eye

7.5.1.7 Conductor crack

There shall be no crack in the conductor.

7.5.1.8 Scratch on conductor

A scratch on a conductor surface, as illustrated in Figure 8, indicates the damage made by a sharp metal point and is harmful to the performance of the printed circuit. The depth (d) of a scratch shall meet the requirement given in Table 5 relative to the conductor thickness (t). The scratch shall not damage the bending property of the repeatedly flexing portion.

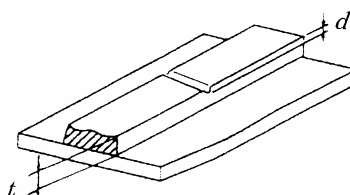


Figure 8 – Scratch on conductor

Table 5 – Allowable scratch on conductor

Level	Depth of scratch on conductor, d
1 and 2	$d \leq 1/3 t$
3	$d \leq 1/5 t$

7.5.1.9 Discoloration

Discoloration shall meet the requirement given in Table 6.

Table 6 – Allowable discoloration

Level	Discoloration
1 and 2	When discoloration is observed on a conductor laminated with coverlay, the discoloration shall be acceptable unless it is remarkably noticeable after conditioning at 40 °C with 90% RH for 96 h
3	The acceptable discoloration shall be agreed upon between user and supplier by means of a limit sample

7.5.2 Visual inspection of coverlay and covercoat

7.5.2.1 Void

Void, as illustrated in Figure 9, shall meet the requirement given in Table 7.

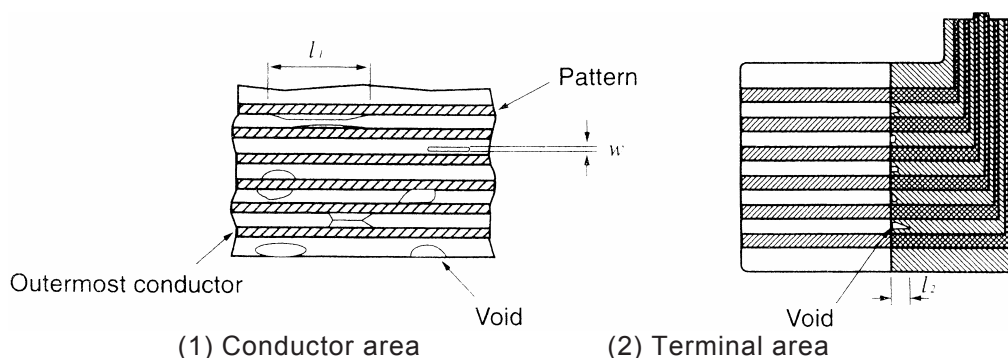


Figure 9 – Voids

Table 7 – Allowable void

Level	Voids
1	A void extending over two or more conductors shall not exist. A void both on the outline edge and to a conductor shall not exist. (A void at the terminal area, as illustrated in Figure 9 (2), shall be acceptable even if it extends to two conductors) The maximum length (l_2) of a void shall be 0,3 mm
2	The length of a void (l_1) shall be no longer than 10 mm. The width of a void (w) shall be no longer than one-third of the spacing between the conductors. There shall be no void in a contact extending to two neighbouring conductors. The maximum length (l_2) of a void shall be 0,3 mm. A void at the repeatedly bending area shall not damage the flexibility of the board
3	There shall be no void

7.5.2.2 Foreign substance

Foreign substance, as illustrated in Figure 10, shall meet the following requirements.

- Conductive foreign substance:** Requirements 7.5.1.3 and 7.5.1.4 of this specification shall apply to conductive foreign substances.
- Non-conductive foreign substance:** Non-conductive foreign substances shall meet the requirement given in Table 8.

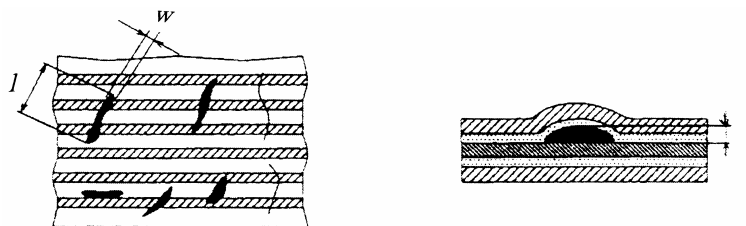


Figure 10 – Foreign substance

Table 8 – Allowable non-conductive foreign substance

Unit: mm

Level	Thickness t	Width w	Length l
Level 1	$t \leq 0,1$	$w \leq 0,3$	$l \leq 3$
Level 2	$t \leq 0,05$	$w \leq 0,2$	$l \leq 2$
Level 3	$t \leq 0,05$	$w \leq 0,05$	$l \leq 1$

A foreign substance shall not extend to three or more conductors

7.5.2.3 Blistering and delamination

There shall be no visible blistering and delamination of coverlay or covercoat along the edge of the FPC, as illustrated in Figure 11. The covercoat shall not be peeled off when using the test tape specified in JIS C 5016, 8.5.1.

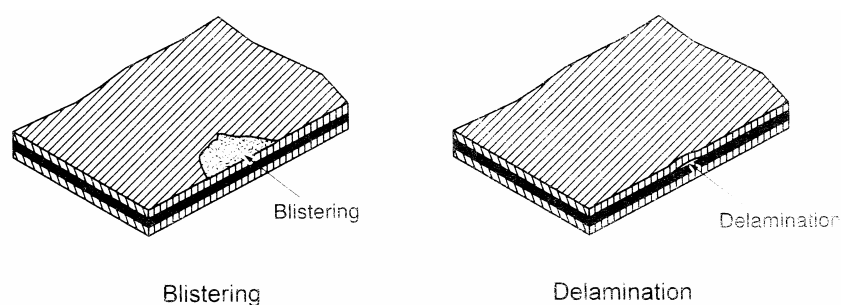


Figure 11 – Lifting and delamination of coverlay and covercoat

7.5.2.4 Squeeze-out of adhesive of coverlay, ooze-out of covercoat and photosensitive register strike

Squeeze-out of adhesive, ooze-out (l) of covercoat and photosensitive register strike, as illustrated in Figure 12, shall comply with the specification given in Table 9.

The squeeze-out and ooze-out at a land as illustrated in Figure 12-1 shall comply with the specification given in Table 10 for the effective land width (w), including possible printing and/or punching errors.

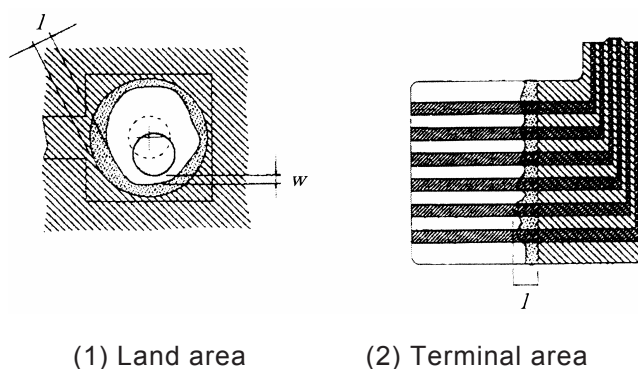


Figure 12 – Allowable squeeze-out of coverlay adhesive and ooze-out of covercoat and photosensitive resist

Table 9 – Allowable squeeze-out of coverlay adhesive, and ooze-out of covercoat and photosensitive register strike

Unit: mm

Level	Squeeze-out of coverlay adhesive and ooze-out of covercoat	Ooze-out of a photosensitive register strike
1 and 2	$l \leq 0,3$	—
3	$l \leq 0,2$	$l \leq 0,1$
3	$\leq 0,2$	$\leq 0,1$

Table 10 – Effective land width at a land

Level	Effective land width, w
1	Squeeze-out/ooze-out contacting the hole edge is acceptable up to one-third of the terminal hole circumference
2	0,05 mm min.
3	0,1 mm min.