

Integrated circuits — Measurement of impulse immunity —

Part 2: Synchronous transient injection method

ICS 31.200

National foreword

This Draft for Development is the UK implementation of IEC/TS 62215-2:2007.

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Comments arising from the use of this Draft for Development are requested so that UK experience can be reported to the international organization responsible for its conversion to an international standard. A review of this publication will be initiated not later than 3 years after its publication by the international organization so that a decision can be taken on its status. Notification of the start of the review period will be made in an announcement in the appropriate issue of *Update Standards*.

According to the replies received by the end of the review period, the responsible BSI Committee will decide whether to support the conversion into an international Standard, to extend the life of the Technical Specification or to withdraw it. Comments should be sent to the Secretary of the responsible BSI Technical Committee at British Standards House, 389 Chiswick High Road, London W4 4AL.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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TECHNICAL SPECIFICATION

**Integrated circuits – Measurement of impulse immunity –
Part 2: Synchronous transient injection method**

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INTRODUCTION

In future standards, test methods and measurement procedures will be given for transient immunity of integrated circuits:

- ESD pulse with resemblance to IEC 61000-4-2;
- EFT pulse with resemblance to IEC 61000-4-4;
- Surge pulse with resemblance to IEC 61000-4-5.

INTEGRATED CIRCUITS – MEASUREMENT OF IMPULSE IMMUNITY –

Part 2: Synchronous transient injection method

1 Scope

IEC/TS 62215-2, which is a technical specification, contains general information and definitions on the test method to evaluate the immunity of integrated circuits (ICs) against fast conducted synchronous transient disturbances. This information is followed by a description of measurement conditions, test equipment and test set-up as well as the test procedures and the requirements on the content of the test report.

The objective of this technical specification is to describe general conditions to obtain a quantitative measure of immunity of ICs establishing a uniform testing environment. Critical parameters that are expected to influence the test results are described. Deviations from this specification should be explicitly noted in the individual test report.

This synchronous transient immunity measurement method, as described in this specification, uses short impulses with fast rise times of different amplitude, duration and polarity in a conductive mode to the IC. In this method, the applied impulse should be synchronized with the activity of the IC to make sure that controlled and reproducible conditions can be assured.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω /150 Ω direct coupling method*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62215-1 (in preparation), as well as the following, apply.

3.1 auxiliary equipment AE

equipment not under test that is nevertheless indispensable for setting up all the functions and assessing the correct performance (operation) of the equipment under test (EUT) during its exposure to the disturbance

3.2 coupling network

electrical circuit for transferring energy from one circuit to another with well-defined impedance and known transfer characteristics

3.3 device under test DUT

device, equipment or system being evaluated

NOTE In this technical specification, it refers to a semiconductor device being tested.

3.4

electromagnetic compatibility

EMC

ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment

[IEC 60050(161):1990, definition 161-01-07]

3.5

electrical noise

unwanted electrical signals, which produce undesirable effects in the circuits of the control system in which they occur

[IEEE std 100-1992-518-1982]

3.6

immunity (to a disturbance)

ability of a device, equipment or system to perform without degradation in the presence of an electromagnetic disturbance

3.7

jitter (time related)

short-term variations of the significant instants of a digital signal from their ideal positions in time

3.8

RF ambient

totality of electromagnetic phenomena existing at a given location

3.9

transient

pertaining to or designating a phenomenon or a quantity which varies between two consecutive steady states during a time interval which is short compared with the time-scale of interest

[IEC 60050(161):1990, definition 161-02-01]

4 General

4.1 Introduction

This immunity test method describes synchronous transient injection on digital and mixed-signal ICs. In this method an impulse is injected into the V_{SS} -, V_{dd} -pin(s) or I/Os successively on the IC subjected to the test.

4.2 Measurement philosophy

This method is related to the 1 Ω resistor method, see IEC 61967-4. In this method a 1 Ω resistor is added in series with the V_{dd} -, V_{SS} pin(s) of the IC. It is assumed that the voltage drop across the 1 Ω resistor in parallel with the DC by-pass inductance is very small. For injecting the impulse, a broadband coupling network is defined. The impulse injection is synchronized to a program loop signal generated by the IC.

One cycle of this response signal is considered as one program loop. The aim of this measurement method is to insert a synchronous but delayed impulse into the IC, related to the program loop. The total time of one program loop period is calculated and then it is

divided into small time steps. At every delay step, a single impulse per program loop is inserted into the IC and its response is measured.

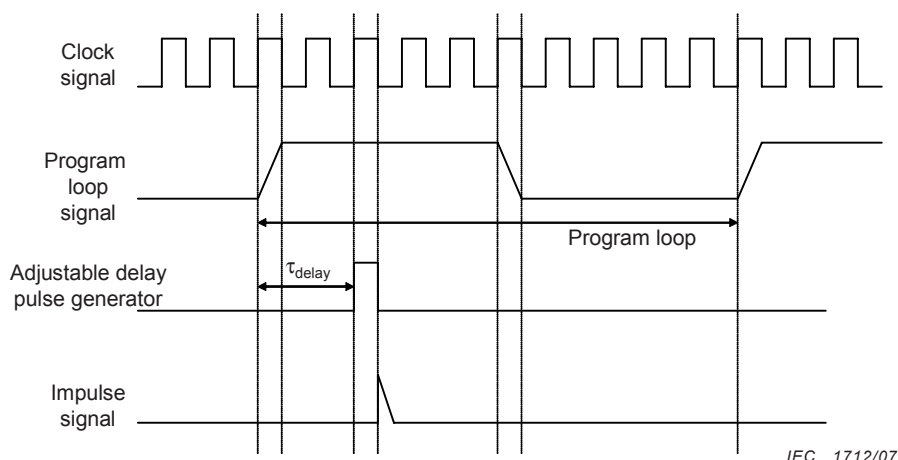


Figure 1 – Synchronous transient injection immunity methodology waveforms

Figure 1 shows the relevant signals occurring in this synchronous transient immunity test. The clock signal is used to run the digital IC and the program loop signal is used as a reference and response signal. A predetermined adjustable delay is used to shift the impulse delay time; τ_{delay} , along the program loop.; τ_{delay} is typically a fraction ($\leq 0,1$) of the rise time of the clock signal. The rising edge of the program loop signal, synchronized with the rising edge of the clock signal, is considered as a fixed reference point, see Figure 1, second line; program loop sync circuitry. Thereafter, the impulse is inserted and the edges of the response signals have to be observed. After every program loop, the delay step is increased and the injection moment of the impulse is shifted. In this way, the full scan can be completed through the program cycle to evaluate the impulse immunity.

The test method will show sensitive time windows, i.e. modes of operation at which the device is sensitive. The non-sensitive time windows can be skipped thereafter while repeating the measurements.

NOTE This measurement methodology is different from the stochastic i.e. random application of impulses.

4.3 Set-up concept

In Figure 2, the block diagram of the test set-up for the synchronous impulse immunity test is given. A trigger signal, e.g. generated by the DUT, is used as an indication to start the measurement. This signal is also used to trigger the delay pulse generator to produce the programmable delay. The delayed pulse triggers the impulse generator that produces an impulse. This impulse is then inserted into the DUT through a suitable coupling network. Measurement equipment such as an oscilloscope or time domain analyser is used to measure the response of the DUT versus the delay of the impulse in the program loop. This measuring equipment is also synchronized with the test signal to acquire the response data over a program loop. A computer interface is used to control the measurement test set-up and to acquire the response data from the test set-up.

In general, the test set-up shall be in accordance with the specific test procedure as described in the future IEC 62215-1. All the test relevant parameters shall be recorded as exactly as possible to ensure that the test results become reproducible.

4.4 Response signal

The response signal is a signal generated by the IC under test (DUT). A clock signal may be externally provided. If the DUT is a microcontroller, then the response signal can be