

Logic digital integrated circuits — Specification for I/O interface model for integrated circuit (IMIC version 1.3)

ICS 31.200

National foreword

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Comments arising from the use of this Draft for Development are requested so that UK experience can be reported to the international organization responsible for its conversion to an international standard. A review of this publication will be initiated not later than 3 years after its publication by the international organization so that a decision can be taken on its status. Notification of the start of the review period will be made in an announcement in the appropriate issue of *Update Standards*.

According to the replies received by the end of the review period, the responsible BSI Committee will decide whether to support the conversion into an international Standard, to extend the life of the Technical Specification or to withdraw it. Comments should be sent to the Secretary of the responsible BSI Technical Committee at British Standards House, 389 Chiswick High Road, London W4 4AL.

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A list of organizations represented on EPL/47 can be obtained on request to its secretary.

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This Draft for Development was published under the authority of the Standards Policy and Strategy Committee on 30 March 2007

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ISBN 978 0 580 50352 8

Amendments issued since publication

Amd. No.	Date	Comments

TECHNICAL SPECIFICATION

IEC TS 62404

First edition
2007-02

**Logic digital integrated circuits –
Specification for I/O interface model
for integrated circuit (IMIC version 1.3)**



Reference number
IEC/TS 62404:2007(E)

CONTENTS

FOREWORD.....	4
INTRODUCTION.....	6
1 Scope.....	7
2 Normative references	7
3 Terms and definitions	7
4 Outline	7
4.1 General.....	7
4.2 Covered range of model	8
4.3 Language for circuits.....	8
4.4 Device model	8
4.5 Structure of model.....	8
4.6 Simulation	8
4.7 Relation to IBIS	8
5 Model structure	9
6 Detailed model description	14
6.1 Description rules	14
6.2 IC model file	16
6.3 Package model file	42
6.4 Module model file	49
7 Levels of models	56
Annex A (informative) Model delivery flow.....	58
Annex B (informative) Example of model description.....	59
Figure 1 – Outline of the model.....	8
Figure 2 – Hierarchy of three models	9
Figure 3 – Data structure of an IMIC model file for IC	11
Figure 4 – Data structure of an IMIC model file for package.....	12
Figure 5 – Data structure of an IMIC model file for module.....	13
Figure 6 – Pad assignment	20
Figure 7 – Example of circuit description.....	24
Figure 8 – Input stimulus	25
Figure 9 – Diode equivalent circuit	29
Figure 10 – Diode characteristics.....	30
Figure 11 – NMOS transistor equivalent circuit	31
Figure 12 – PMOS transistor equivalent circuit.....	31
Figure 13 – Gate channel characteristics of MOS transistor	32
Figure 14 – Characteristics of diode in MOS transistor.....	33
Figure 15 – NPN transistor equivalent circuit	35
Figure 16 – PNP transistor equivalent circuit	35
Figure 17 – Static characteristics of bipolar transistor	35
Figure 18 – NMOS characteristics on regular grid	39

Figure 19 – MOS transistor model with two-terminal model	39
Figure 20 – Relationship between inner terminals and equivalent circuits of package	46
Figure 21 – Relationship between outer terminals and equivalent circuits of package	47
Figure 22 – Example of module circuit	53
Figure 23 – Example of signal source of module	55
Figure A.1 – Delivery flow of model files	58
Figure B.1 – IC structure	59
Figure B.2 – Equivalent circuit	59
Table 1 – Elements of model structures	10
Table 2 – Levels of models	57
Table 3 – Required elements of model for each level	57

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**LOGIC DIGITAL INTEGRATED CIRCUITS –
SPECIFICATION FOR I/O INTERFACE MODEL
FOR INTEGRATED CIRCUIT
(IMIC version 1.3)**

FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62404, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/746/DTS	47A/751/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

With an increase in speed of electronic systems, it becomes necessary to accurately predict electrical performance including noise in electronic systems with integrated circuits.

Simulators have been used for this purpose. Simulators need accurate models for describing electrical properties of integrated circuits. Semiconductor manufacturers and/or suppliers are required by their users to prepare device models for various simulation tools, some of which are not compatible with SPICE. In addition, since SPICE models contain proprietary process parameters, a non-disclosure agreement is typically required to obtain these from the vendor.

IBIS (I/O Buffer Interface Specification) has been proposed as a model for integrated circuits, which, approved as IEC 62014-1, has the following features:

- since electrical properties of I/O buffers are described in table format, disclosure of proprietary information such as process parameters is drastically reduced;
- it is easy to get IBIS models that are supported by many simulation tools;
- a public domain tool can convert SPICE models into IBIS models.

However, IBIS models seem to have the following problems:

- the modeling of power and ground currents is insufficient for accurate power and ground bounce analysis;
- since an IBIS model has only the final stage at output and input, it is difficult to model the effect of loading on circuit boards on output and input waveforms. The fixed model taken by IBIS has little flexibility for describing other circuitry;
- in order to simulate EMI with accuracy, more information such as material constant and three-dimensional structures is needed.

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

1 Scope

The following items are considered to standardize the electrical modeling of input signals, output signals, power supply and ground terminals of integrated circuits, in order to provide for analysis of electrical characteristics of equipment.

- 1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities.
- 2) To define more flexible description rules for electric circuits in order to provide more accurate analysis of printed circuit board.
- 3) To introduce the concept of modeling levels to exchange relevant data for each application.
- 4) To enhance electrical modeling for packages and modules.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62014-1:2001, *Electronic design automation libraries – Part 1: Input/output buffer information specifications (IBIS version 3.2)*

3 Terms and definitions

Under consideration

4 Outline

4.1 General

The outline of this model is shown in Figure 1.

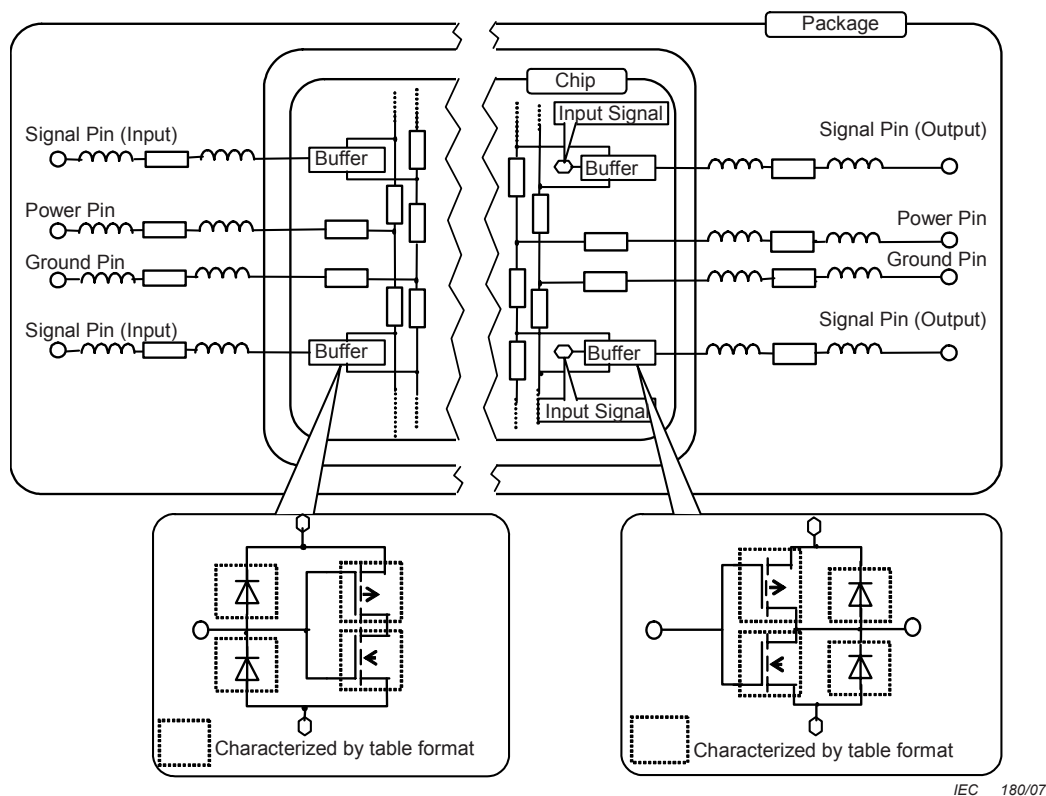


Figure 1 – Outline of the model

4.2 Covered range of model

The model is described as circuits covering the whole or a part of the I/O buffers and the package.

4.3 Language for circuits

The circuits shall be described in extended SPICE format. The structure allows describing simple buffers, complex buffers, power and ground lines, packages and complex memory module boards in a unified format.

4.4 Device model

The characteristics of non-linear devices redescribed in one-dimensional, two-dimensional or three-dimensional table format.

4.5 Structure of model

The data of the model consists of integrated circuit, package and module portions. Therefore each portion can be generated independently.

4.6 Simulation

The netlist of printed circuit board and the I/O buffer model defined by this specification provides accurate circuit simulation results.

4.7 Relation to IBIS

Tools that can extract IBIS data from this model are possible to develop.

5 Model structure

The model shall describe the inside of ICs, packages and module boards as shown in Figure 2.

The models of IC, package and module board consist of the elements given in Table 1.

The data structures of IC, package and module board models are shown in Figure 3, Figure 4, and Figure 5, respectively.

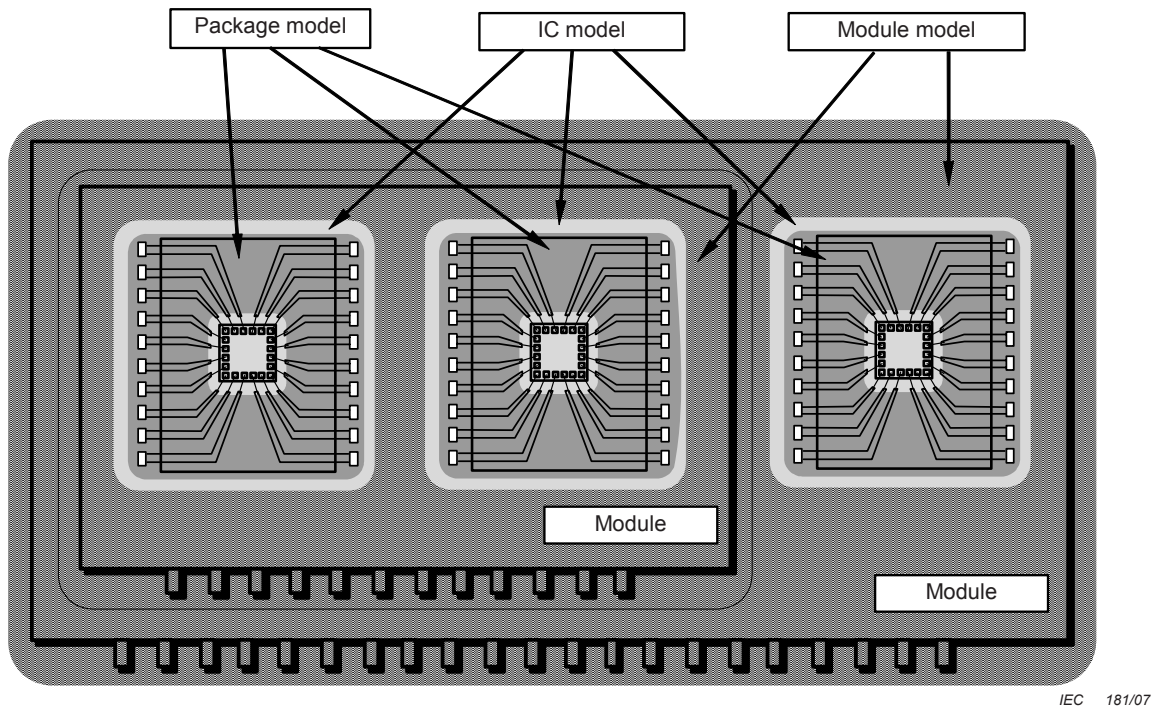


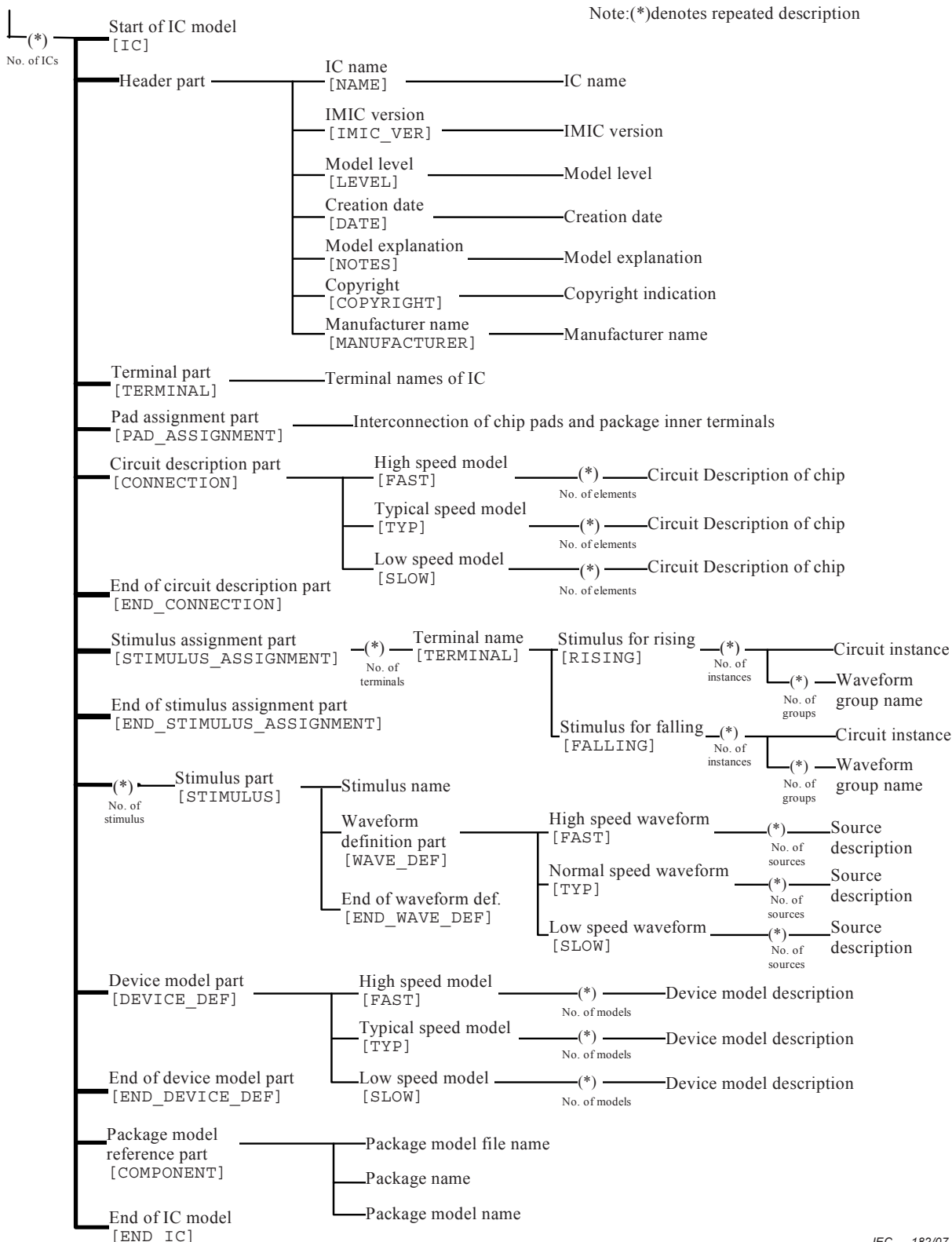
Figure 2 – Hierarchy of three models

IEC 181/07

Table 1 – Elements of model structures

File	Element	Description
IC model file	Header	IC type, model version, model level.
	External terminals	IC external terminals (package pins).
	Pad assignment	Connection between IC pads and package inner terminals.
	Circuit description	Internal circuits and their connections.
	Input stimulus assignment	Internal circuits and their stimuli to generate output waveforms.
	Input stimulus	Input waveforms.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	Package model reference	Name of the package model to be used.
Package model file	Header	Package name, model version, model level.
	Model name	List of models in package circuit model.
	Inner terminal	Cross-reference between internal terminals and package internal circuit model.
	Outer terminal	Cross-reference between external circuit and package internal circuit model.
	Circuit description	Internal circuits and their connections.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	Structure	Material, position, three-dimensional structures.
Module model file	Header	Module name, model version, model level.
	External terminals	External terminals (pins) of module.
	Circuit description	Internal circuits and their connections.
	Signal source	Internal circuits and their terminals to generate output waveforms at corresponding external terminals.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	IC/Module model reference	Names of IC/module model files and model names to be used.
	Structure	Material, position, three-dimensional structures.

IC model file
xxx . IMC

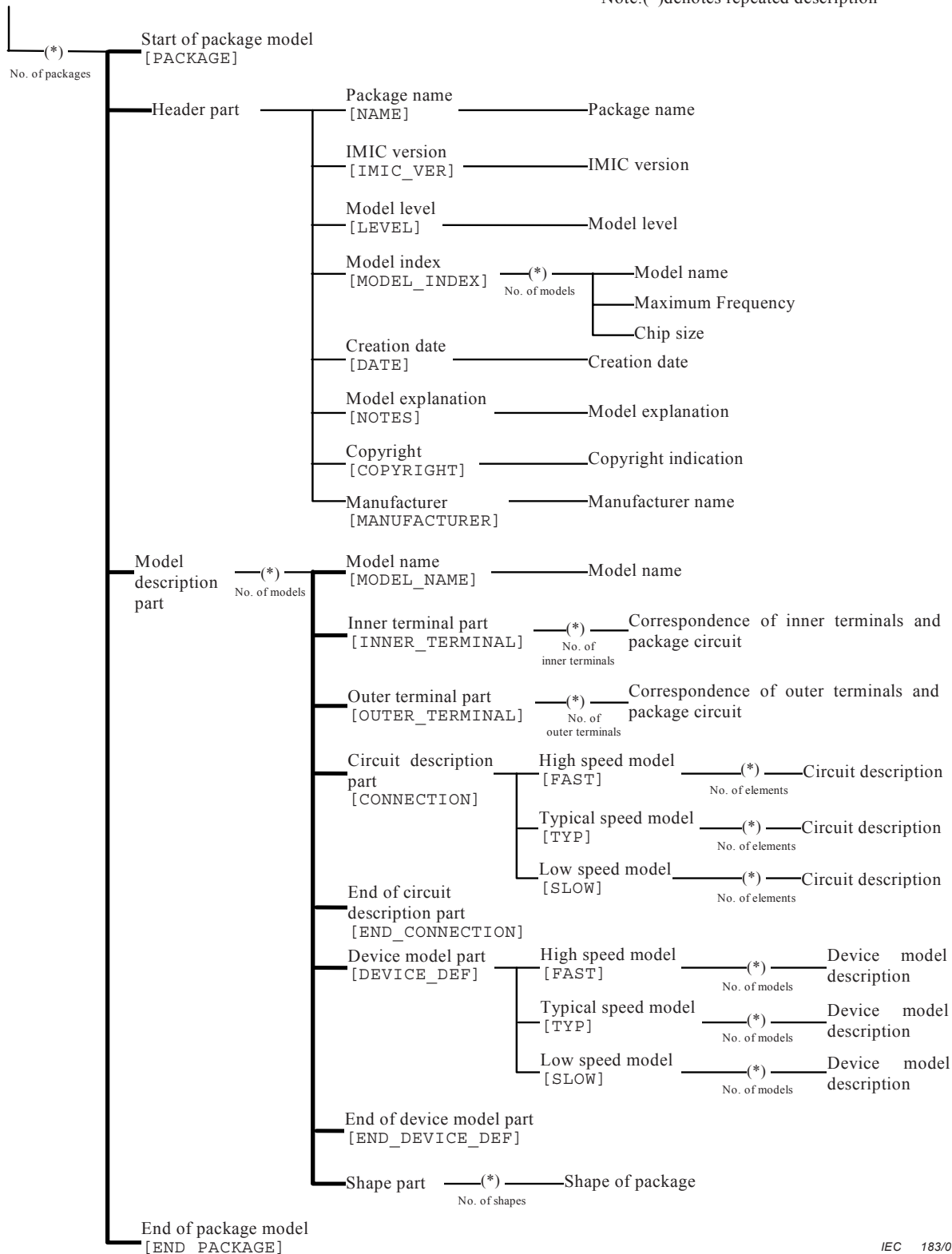


IEC 182/07

Figure 3 – Data structure of an IMIC model file for IC

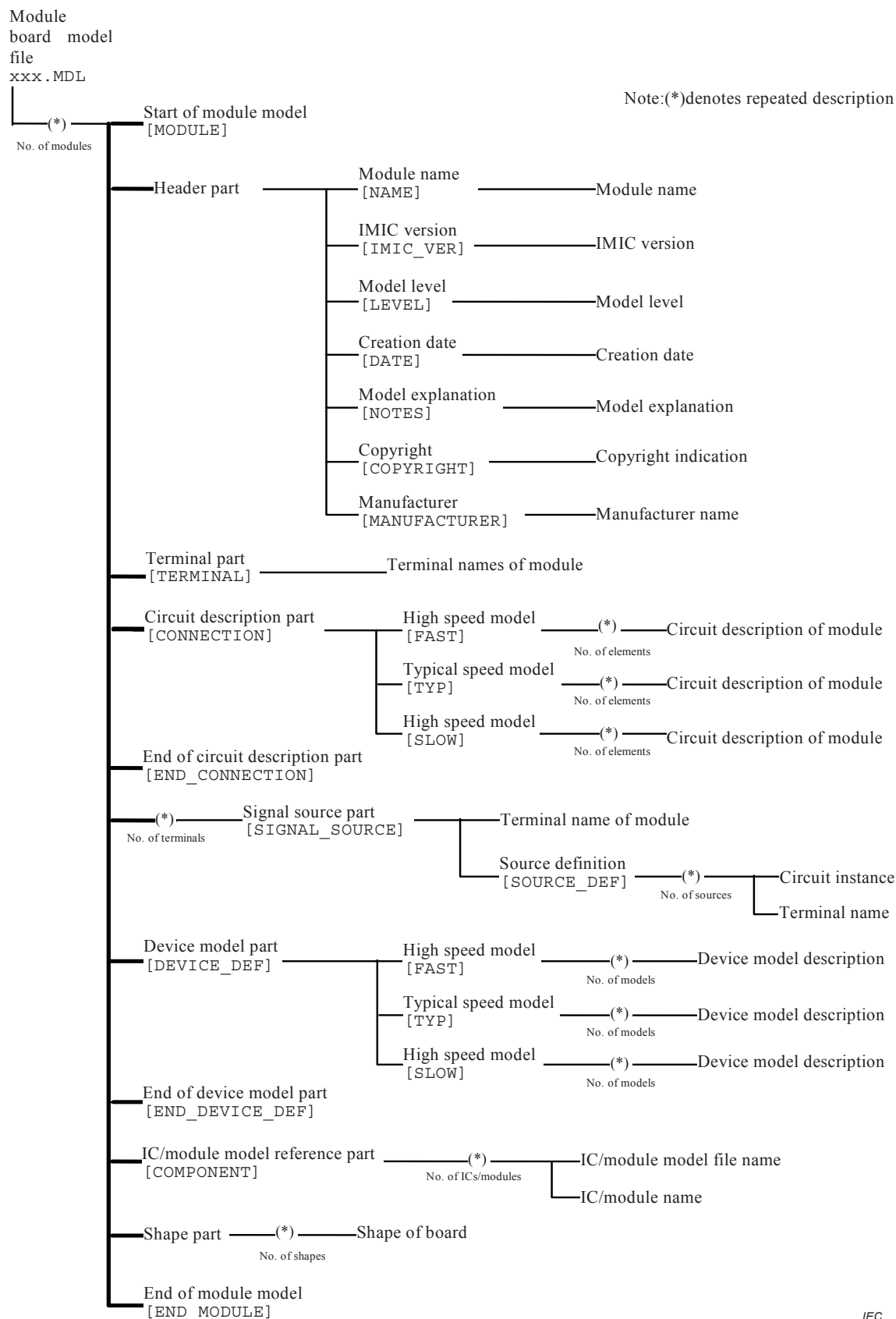
Package
model file
xxx . PKG

Note:(*)denotes repeated description



IEC 183/07

Figure 4 – Data structure of an IMIC model file for package



IEC 184/07

Figure 5 – Data structure of an IMIC model file for module

6 Detailed model description

6.1 Description rules

6.1.1 Characters

Recognition of characters in the model files is case insensitive. For instance, 'M' and 'm' are treated as the same character. It is recommended that all upper case or all lower case characters may be used.

6.1.2 Available characters

6.1.2.1 Available characters

A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, +, -, /, #, !, <, >, _ and %

6.1.2.2 Special characters

6.1.2.2.1 General

[]: Keywords

" ": Equations

. : File Extension

Space, TAB: Delimiter

6.1.2.2.2 Example of equations

'2.0*1+3'

"log(x)+2.3"

6.1.3 Keywords

6.1.3.1 General

Keywords shall be enclosed in square brackets, [], and shall be described from column 1 of the line. Tab or space cannot be used within []. The detailed description shall be described on the same line and/or the following lines as the keyword. There are three types of keyword format:

6.1.3.2 Type-1

The detailed descriptions shall be placed between [keyword] line and [END_keyword] line.

Example:

[IC]

....

[END_IC]

6.1.3.3 Type-2

The detailed descriptions shall be placed next to the [keyword] line. There is no [END_keyword] line.

Example:

[TERMINAL]

SUBCKT ALVCH16244 SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG

6.1.3.4 Type-3

[keyword] shall be followed by the detailed descriptions on the same line. There is no [END_keyword] line.

Example:

[NAME] ALVCH16244

6.1.4 Numbers and numerical values

6.1.4.1 General

The decimal sign shall be “.” (full-stop or period) on the line instead of “,” (comma), against 6.6.8.1 of ISO/IEC Directives, Part 2, 2004 ¹⁾ for the purpose of computer processing.

A scaling factor or scientific notation may be allowed. Either scaling factor or exponential expression may be used.

6.1.4.2 Scaling factor

T (tera) : 10^{12} G (giga) : 10^9 MEG, X (mega) : 10^6 K (kilo): 10^3

M (milli) : 10^{-3} U (micro): 10^{-6} N (nano): 10^{-9} P (pico): 10^{-12}

F (femto) : 10^{-15}

6.1.4.3 Scientific notation

Scientific notation shall use “E”.

6.1.4.4 Examples

1.3X=1.3E6=1300K=1300E3=1300000

0.5U=5E-7=500N=500E-9=0.0000005

6.1.5 Comment

When the first letter on the line is asterisk “*”, the rest of text on the line is deemed as a comment. When “\$” appears anywhere on the line, the rest of text on the line is deemed as a comment.

6.1.6 Continuous lines

Any statement beginning with “+” is considered to be a continuation of the previous statement.

¹⁾ ISO/IEC Directives, Part 2, 2004: *Rules for the structure and drafting of International Standards*

6.1.7 Reserved node names

The reserved node names for ideal reference ground are 0, GND, GND! and GROUND. Therefore, these node names cannot be used as signal names.

6.1.8 Order of descriptions

Descriptions in the file shall be ordered as shown in Figures 3, 4, and 5, where items at the top of a solid vertical line are to be described at the beginning, and items at the bottom are to be described at the end. Items along horizontal line may appear in any order with respect to each other.

6.2 IC model file

6.2.1 File name

6.2.1.1 General

The name of the model file starts with any alphabetical or numerical characters, with .IMC as an extension.

6.2.1.2 Example

ALVCH16244.IMC

NOTE The limitation of file name length (number of characters) depends on operating system.

6.2.2 Start and end of model description

6.2.2.1 General

The description of one model shall be represented as the single IC model.

6.2.2.2 Start of IC model description

6.2.2.2.1 Description

[IC]

6.2.2.2.2 Explanation

The contents of the model follow with this description.

6.2.2.3 End of IC model description

6.2.2.3.1 Description

[END_IC]

6.2.2.3.2 Explanation

The description of the IC model shall be terminated by this keyword.

6.2.3 Header

6.2.3.1 General

IC type, model level etc. shall be described as the beginning statement of IC model.

6.2.3.2 IC type

6.2.3.2.1 Description

[NAME] arbitrary text

6.2.3.2.2 Explanation

This indicates the IC type identifier, which includes Product Number and/or Name.

This is used by simulators to assign the correct model for an IC in a design.

6.2.3.2.3 Example

[NAME] ALVCH16244

6.2.3.3 Model version

6.2.3.3.1 Description

[IMIC_VER] arbitrary text

6.2.3.3.2 Explanation

The version number of the IMIC specification shall be described. Currently, only version 1.3 is available. Parsers shall follow the appropriate syntax rules for the entire IC model.

6.2.3.3.3 Example

[IMIC_VER] 1.3

6.2.3.4 Model level

6.2.3.4.1 Description

[LEVEL] Integer

6.2.3.4.2 Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise.

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise.

Level 3: EMI (Electromagnetic Interference) model for the analysis of conducted electromagnetic emission noise. This level is not available in this version.

Detailed specification is explained in Clause 7.

6.2.3.4.3 Example

[LEVEL] 2

6.2.3.5 Date

6.2.3.5.1 Description

[DATE] date

6.2.3.5.2 Explanation

The model release date is described using any of the following formats.

- Day / Month name / Year Example: 23MAR98
- Month name Day, Year Example: MARCH 23, 1998

6.2.3.5.3 Example

[DATE] 23MAR98

6.2.3.6 Explanation of model**6.2.3.6.1 Description**

[NOTES]

Arbitrary notes concerning the model shall be described if appropriate. This may be used for explanations of the origin, usage, and testing of the model, for example.

6.2.3.6.2 Explanation

Any comments can be described on the lines following [NOTES].

6.2.3.6.3 Example

[NOTES]

ELECTRICAL MODEL FOR ALVCH16244

6.2.3.7 Copyright**6.2.3.7.1 Description**

[COPYRIGHT] arbitrary text

6.2.3.7.2 Explanation

Copyright holder and related terms shall be stated.

6.2.3.7.3 Example

[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED

6.2.3.8 Manufacturer**6.2.3.8.1 Description**

[MANUFACTURER] arbitrary text

6.2.3.8.2 Explanation

Manufacturer is declared here.

6.2.3.8.3 Example

[MANUFACTURER] ZYX CORP.

6.2.4 Terminals

6.2.4.1 General

The external terminals of IC shall be defined. The external terminals are equivalent to the IC pins.

6.2.4.2 Description

[TERMINAL]

Arbitrary text

6.2.4.3 Explanation

The external terminals of the IC are defined.

The data begin on the line following [TERMINAL].

Signal names of external terminals at [PAD_ASSIGNMENT] shall be described.

The IC type name follows the string ".SUBCKT", and the names of terminals follow that.

6.2.4.4 Example

[TERMINAL]

.SUBCKT ALVCH16244 SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG

6.2.5 Pad assignment (see Figure 6)

6.2.5.1 General

The interconnections between chip pads and package inner terminals shall be described.

6.2.5.2 Description

[PAD_ASSIGNMENT]

Arbitrary text

6.2.5.3 Explanation

6.2.5.4 General

The interconnections between chip pads and package inner terminals are described.

The data begin on the line following [PAD_ASSIGNMENT].

Signal names of package inner terminals that are connected to chip pads shall be coincident with the signal names of the corresponding chip pads in ".SUBCKT" statement in [CONNECTION].

The data are given as subcircuit instance statements, starting with "X".

The subcircuit name of the top level ".SUBCKT" in [CONNECTION] shall appear after the terminal names at the end of this statement.

Following SPICE conventions, use of a particular node name (also known as a signal name) on both the chip instance and the package instance signifies a connection between these terminals.

NOTE If a chip pad is not connected to any package pad, the chip pad terminal shall be connected to signal "NO_CONNECTION". If a package inner terminal is not connected to any chip pad, the inner terminal shall be connected to signal "NO_CONNECTION".

6.2.5.5 Example

In the example below, the signal "SIG1I" is the first terminal of the CHIP connection to the first terminal of the PACKAGE.

[PAD_ASSIGNMENT]

```
XCHIP SIG1I SIG2I SIG3I SIG4I SIG5I SIG6I CHIP
XPACKAGE SIG1I SIG2I SIG3I SIG4I SIG5I SIG6I
+ SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG PACKAGE
```

[CONNECTION]

```
SUBCKT CHIP PAD1 PAD2 PAD3 PAD4 PAD5 PAD6
```

ENDS CHIP

<Package model file>

[CONNECTION]

```
SUBCKT PACKAGE L1I L2I L3I L4I L5I L6I
+ LEAD1 LEAD2 LEAD3 LEAD4 LEAD5 LEAD6 LEAD7 REFG
```

ENDS PACKAGE

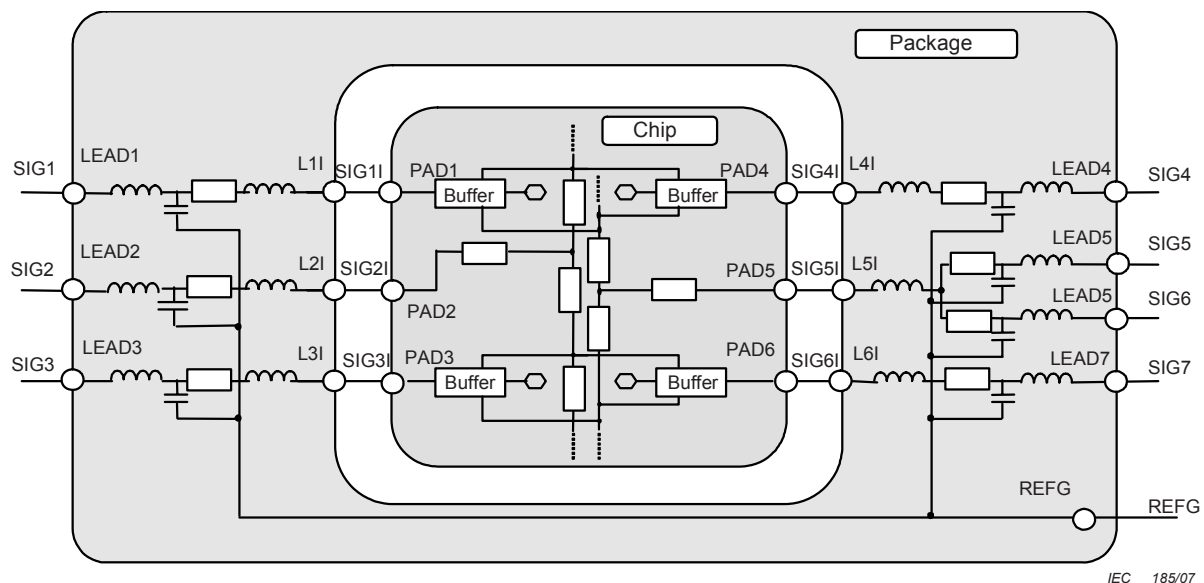


Figure 6 – Pad assignment

6.2.6 Circuit description (see example in Figure 7)

6.2.6.1 General

The elements of the internal circuit and their interconnections shall be described.

6.2.6.2 Description

[CONNECTION]

[FAST]

[TYP]

[SLOW]

[END_CONNECTION]

6.2.6.3 Explanation

6.2.6.3.1 General

The elements of internal circuit and their interconnections shall be described. The description is terminated with [END_CONNECTION].

Circuit descriptions with keywords are described after [CONNECTION].

These keywords are optional.

[FAST] Circuit description for the highest speed.

[TYP] Circuit description for typical speed.

[SLOW] Circuit description for the lowest speed.

The internal circuit of the chip contains the pad capacitance model statements.

The top level description of the internal circuit shall be described between “.SUBCKT” and “.ENDS”.

“.SUBCKT” shall be described together with subcircuit name of the top level circuit and pad signal names.

“.ENDS” shall be described together with subcircuit name of the top level circuit.

The general circuit description is as follows.

Element_Name <Node_Name> [Value] [Model_Name] <[Parameter = Parameter_Value]>

Where, < > indicates repeatable, and [] indicates optional.

Available elements include the following: resistor, capacitor, inductor, mutual inductor, diode, MOS transistor, bipolar transistor, voltage-controlled voltage source, current-controlled current source, voltage-controlled current source, current-controlled voltage source, lossless transmission line, independent voltage source, independent current source, subcircuit call, and subcircuit description. The first character of each element statement denotes the element type. The model name shall be defined in the device description.

Each element description is as follows.

6.2.6.3.2 Resistor

Rxxxxxxx node1 node2 *value* or model_name

Where unit of *value* is ohm.

6.2.6.3.3 Capacitor

Cxxxxxxx node1 node2 *value* or model_name

Where unit of *value* is (F) Farad.