

DIN EN 16602-60-02

ICS 49.140

**Raumfahrtproduktsicherung –
Entwicklung von ASIG und FPGA;
Englische Fassung EN 16602-60-02:2014**

Space product assurance –
ASIC and FPGA development;
English version EN 16602-60-02:2014

Assurance produit des projets spatiaux –
Développement des ASIC et FPGA;
Version anglaise EN 16602-60-02:2014

Gesamtumfang 67 Seiten

DIN-Normenausschuss Luft- und Raumfahrt (NL)

Nationales Vorwort

Dieses Dokument (EN 16602-60-02:2014) wurde vom Technischen Komitee CEN/CLC/TC 5 „Raumfahrt“ erarbeitet, dessen Sekretariat vom DIN (Deutschland) gehalten wird.

Das zuständige deutsche Normungsgremium ist der Arbeitsausschuss NA 131-10-01 AA „Interoperabilität von Informations-, Kommunikations- und Navigationssystemen“ im DIN-Normenausschuss Luft- und Raumfahrt (NL).

Dieses Dokument (EN 16602-60-02:2014) basiert auf ECSS-Q-ST-60-02C.

Dieses Dokument enthält unter Berücksichtigung des DIN-Präsidialbeschlusses 1/2004 nur die englische Originalfassung von EN 16602-60-02:2014.

Dieses Dokument wurde speziell zur Behandlung von Raumfahrtsystemen erarbeitet und hat daher Vorrang vor jeglicher Europäischer Norm, da es denselben Anwendungsbereich hat, jedoch über einen größeren Geltungsbereich (z. B. Luft- und Raumfahrt) verfügt.

Nationaler Anhang NA (informativ)

Begriffe und Abkürzungen

3 Begriffe und Abkürzungen

3.1 Begriffe aus anderen Normen

Für die Anwendung dieser Norm gelten die Begriffe nach ECSS-ST-00-01.

3.2 Für diese Norm spezifische Begriffe

3.2.1

anwendungsspezifischer integrierter Schaltkreis

(en: Application Specific Integrated Circuit, ASIC)

vollständig oder teilweise nach Kundenwünschen gestalteter monolithischer integrierter Schaltkreis, der über digitale, analoge oder gemischte Funktionen für einen bestimmten Anwender verfügen kann

3.2.2

ASIC-Technologie

Gesamtheit aller für den Entwurf und die Herstellung und Prüfung von ASIC-Bauteilen erforderlichen Elemente

ANMERKUNG Entwurfswerkzeuge und deren Beschreibung, Zellenbibliotheken, Verfahrensweisen, Entwurfsregeln, Verfahrenslinie und Prüfausrüstung.

3.2.3

anwendungsspezifische Standardprodukte

(en: application specific standard products, ASSP)

ASIC, die darauf ausgelegt sind, Standardprodukte zu bilden, die für eine größere Bandbreite an Anwendungen zur Verfügung gestellt werden

ANMERKUNG ASSP werden meistens mit einem VHDL-Modell versehen und mit einer Dokumentation ausgeliefert.

3.2.4

Blockschaltbild

abstrakte grafische Darstellung von miteinander verbundenen und mit Namen versehenen Rechtecken (Blöcken), die eine architektonische oder funktionsbezogene Zeichnung darstellen

3.2.5

Zelle

spezielle Schaltkreisfunktion einschließlich digitaler oder analoger Basisblöcke

3.2.6

Zellenbibliothek

Zusammenstellung von miteinander kompatiblen Zellen, die einer Reihe von allgemeinen Einschränkungen und genormten Schnittstellen entspricht, die für eine festgelegte Technologie ausgelegt und beschrieben sind

3.2.7

Datenblatt

detaillierte Beschreibung eines Bauteils in Bezug auf seine Funktionen, Betrieb und Parameter

ANMERKUNG Ein Datenblatt kann z.B. Blockschaltbilder, Wahrheitstabellen, Anschlussstift- und Signalbeschreibungen, umweltbezogene, elektrische und leistungsbezogene Parameter, zulässige Abweichungen, Terminierungsinformationen und Verpackungsbeschreibungen enthalten.

3.2.8

Entwurfsfluss

Auswahl und Abfolge der bei der Implementierung des Entwurfs anzuwendenden technischen Entwicklungsverfahren und -werkzeuge

3.2.9

Struktur für prüffreundliches Entwickeln

(en: design for test [DFT] structure)

Technik, die angewendet wird, um die Prüfung eines komplexen integrierten Schaltkreises (IC) zu ermöglichen

ANMERKUNG Dies kann jeden Wirkungsmechanismus einschließen, der darauf abzielt, zu besserer Beobachtbarkeit oder Beherrschbarkeit von internen Knoten des Chips zu gelangen, die für primäre Ein- und Ausgaben unzugänglich sind.

3.2.10

Entwurfswiederholungsschritt

Entwurfsänderungen, die innerhalb einer oder mehreren Phasen oder zwischen zwei aufeinander folgenden Phasen auftreten, wie im ASIC- und FPGA-Entwicklungsplan festgelegt, bevor der Entwurf für die Implementierung des Prototyps freigegeben wird

3.2.11

Bauartspezifikation

Beschaffungsspezifikation unter Einhaltung des ESCC-Formats, die z. B. Bemessungsgrenzwerte, Parameter einschränkungen, den mechanischen Grundriss, die Anschlussstiftbeschreibung und Klassierungsanforderungen festlegt

3.2.12

Entwicklungsschritt

wesentlicher Schritt des Entwicklungsflusses für die ASIC- und FPGA-Entwicklung

ANMERKUNG Festlegungsphase, architektonischer Entwurf, detaillierter Entwurf, Anordnung, Implementierung des oder der Prototypen und Entwurfsvalidierung.

3.2.13

Fehlzustandserkennungsgrad erkennbarer Fehleranteil

als Prozentsatz angegebenes Maß des Anteils der Fehlzustände eines digitalen Schaltkreises an dessen möglichen Fehlerzuständen, die im Falle eines gegebenen Satzes von Prüfmustern und in Bezug auf ein bestimmtes Fehlerzustandsmodell tatsächlich erkannt werden können

3.2.14

feldprogrammierbares Gatterfeld

(en: field programmable gate array, FPGA)

Standard-Halbleitergerät, das im Falle seiner Programmierung durch den Anwender mit Hilfe der FPGA-spezifischen Hard- und Softwaretools zu einem kundenspezifischen Gerät wird

3.2.15

Bauplan

abstrahierte, maßstäbliche Zeichnung der Schaltungsanordnung des Chips, die die Form, Größe und Position der wesentlichen Funktionsblöcke und die Kontaktflächen einschließlich der Stromleitungen und Grundlinien, Zeittaktverteiler und Verbindungskanäle zeigt

3.2.16

HDL-Modell

Textmodell, das auf einer Hardwarebeschreibungssprache (jedoch nicht einem Teil der eigentlichen Software) basiert und sich zur Beschreibung von Verhalten oder Struktur, zur Simulation und durch die Auswahl eines geeigneten Abstraktionsgrades zur automatischen Netzlistenerstellung eignet

3.2.17**schutz-/urheberrechtlich geschützter Kern**

(en: intellectual property [IP] core)

Entwurfselement, das eine eigenständige eigentumsrechtlich geschützte Funktion oder Funktionsgruppe implementiert

ANMERKUNG 1 Ein schutz-/urheberrechtlich geschützter Kern kann von einem Kunden gegen Zahlung eines angegebenen Preises und unter einer vom Eigentümer festgelegten Lizenzvereinbarung, in der die vom Kunden erworbenen Rechte festgelegt sind, erworben werden.

ANMERKUNG 2 Ein schutz-/urheberrechtlich geschützter Kern kann als HDL-Datei (z. B. synthesefähiger VHDL-Code oder Gatternetzliste) und mit der unerlässlichen Komplementärdokumentation geliefert werden, die es dem Kunden ermöglicht, diesen Kern erfolgreich in einem System zu implementieren und zu nutzen (z. B. Benutzerhandbuch und Verifizierungsdateien).

3.2.18**Makrozelle**

Modul, das komplexe Funktionen in einer Zellenbibliothek des Herstellers enthält, die aus festverdrahteten primitiven Zellen aufgebaut ist

3.2.19**Netzliste**

formatierte Liste von Zellen (Grundsaltungen) und ihren Verbindungen

3.2.20**Geräteprototyp**

gefertigter ASIC oder programmiertes FPGA, der bzw. das zur Validierung des neuen Entwurfs in Bezug auf dessen Funktionalität, Leistungsfähigkeit, Betriebsgrenzwerte und Kompatibilität mit dem betreffenden System verwendet wird

3.2.21**Neukonstruktion**

Entwurfsänderungen, die mehr als zwei aufeinander folgende Phasen der ASIC- und FPGA-Entwicklung betreffen, oder Entwurfsänderungen, die nach der Implementierung eines Prototyps implementiert wurden

3.2.22**Reize**

Eingangsdatensatz für Simulations- oder Prüfzwecke, um eine bestimmte Funktionalität oder Leistung eines Geräts nachzuweisen

3.2.23**Prüfmuster**

zum Nachweis des vorschriftsmäßigen Verhaltens eines Geräts verwendete Simulationsreize und die dafür erwarteten Reaktionen (unter Berücksichtigung der für die Einhaltung der Prüfeinrichtungsanforderungen geltenden speziellen Einschränkungen)

3.3 Abkürzungen

Für die Anwendung dieser Norm gelten die Abkürzungen nach ECSS-S-ST-00-01 und die folgenden Abkürzungen:

Abkürzung Bedeutung

ACP	ASIC- und FPGA-Steuerungsplan (en: ASIC and FPGA control plan)
ADP	ASIC- und FPGA-Entwicklungsplan (en: ASIC and FPGA development plan)
ARS	ASIC- und FPGA-Anforderungsspezifikation (en: ASIC and FPGA requirements specification)

Abkürzung Bedeutung

ASCII	American Standard Code for Information Interchange
ASIC	anwendungsspezifischer integrierter Schaltkreis (en: Application Specific Integrated Circuit)
ASSP	anwendungsspezifisches Standardprodukt (en: application specific standard product)
DD	Entwurfsdokumentation (en: design documentation)
DDR	ausführliches Design-Review (en: detailed design review)
DFT	prüffreundliches Entwickeln (en: design for test)
DRC	Prüfung der Designregeln (en: design rule check)
DVP	Entwurfsvalidierungsplan (en: design validation plan)
EDA	elektronische Entwurfsautomatisierung (en: electronic design automation)
EDIF	elektronisches Entwurfsaustauschformat (en: electronic design interchange format)
ERC	Prüfung der elektrischen Regeln (en: electrical rule check)
ESCC	European Space Component Coordination
FM	Flugmodulbauteil (en: flight module part)
FPGA	feldprogrammierbares Gatterfeld (en: field-programmable gate array)
FRA	Umsetzbarkeits- und Risikoanalysebericht (en: feasibility and risk analysis report)
GDS	Grafikdesignsystem (en: graphic design system) (Industriestandard-Grafikeingabewerkzeug)
HDL	Hardwarebeschreibungssprache (en: hardware description language)
	ANMERKUNG Dieser Begriff wird im Allgemeinen für die verschiedenen Hardwarebeschreibungssprachen verwendet, die für die Kodierung während der Entwurfsphase angewendet werden; z. B. VHDL und verilog.
IDMP	Eingangsdaten für Masken- oder Programmierungsdateierzeugung (en: input data for mask or programming file generation)
IEEE	Institute of Electrical and Electronics Engineers
IP	Schutz-/Urheberrecht (en: intellectual property)
MoM	Sitzungsprotokoll (en: minutes of meeting)
P&R	Ort und Route (en: place and route)
JTAG	Gemeinsame Prüfkaktionsgruppe (en: Joint Test Action Group)
LVS	Überprüfung Layout versus Schematic (en: layout vs. schematic check)
NCC	Netzlistenvergleichsüberprüfung (en: netlist comparison check)
QML	Liste der qualifizierten Hersteller (en: qualified manufacturer list)
RTL	Registertransferlogik (en: register transfer logic)
SEU	Einzelereignis-Upset
VHDL	VHSIC-Hardwarebeschreibungssprache (en: Very High Speed Integrated Circuit [VHSIC] Hardware Description Language)

English version

Space product assurance - ASIC and FPGA development

Assurance produit des projets spatiaux - développement
des ASIC et FPGA

Raumfahrtproduktsicherung - Entwicklung von ASIG und
FPGA

This European Standard was approved by CEN on 13 March 2014.

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This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CEN and CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

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Table of contents

Foreword	5
Introduction.....	6
1 Scope.....	7
2 Normative references	8
3 Terms, definitions and abbreviated terms.....	9
3.1 Terms from other standards.....	9
3.2 Terms specific to the present standard	9
3.3 Abbreviated terms.....	12
4 ASIC and FPGA programme management.....	14
4.1 General.....	14
4.1.1 Introduction	14
4.1.2 Organization.....	14
4.1.3 Planning.....	14
4.2 ASIC and FPGA control plan	14
4.3 Management planning tools	15
4.3.1 ASIC and FPGA development plan	15
4.3.2 Verification plan	15
4.3.3 Design validation plan	15
4.4 Experience summary report.....	15
5 ASIC and FPGA engineering	16
5.1 Introduction.....	16
5.2 General requirements	16
5.3 Definition phase.....	19
5.3.1 Introduction	19
5.3.2 General requirements	19
5.3.3 Feasibility and risk assessment.....	19
5.3.4 ASIC and FPGA development plan	20
5.3.5 System requirements review	20
5.4 Architectural design	22
5.4.1 General requirements	22
5.4.2 Architecture definition.....	22

5.4.3	Verification plan	23
5.4.4	Architecture verification and optimization	23
5.4.5	Preliminary data sheet	24
5.4.6	Preliminary design review	24
5.5	Detailed design	24
5.5.1	Introduction	24
5.5.2	General requirements	25
5.5.3	Design entry.....	25
5.5.4	Netlist generation	26
5.5.5	Netlist verification	27
5.5.6	Updated data sheet.....	28
5.5.7	Detailed design review	28
5.6	Layout.....	29
5.6.1	General requirements	29
5.6.2	Layout generation	29
5.6.3	Layout verification	30
5.6.4	Design validation plan	31
5.6.5	Updated data sheet.....	31
5.6.6	Draft detail specification	31
5.6.7	Critical design review	31
5.7	Prototype implementation	32
5.7.1	Introduction	32
5.7.2	Production and test	32
5.8	Design validation and release	33
5.8.1	Design validation.....	33
5.8.2	Radiation test performance	33
5.8.3	Design release and FM production preparation.....	34
5.8.4	Experience summary report	34
5.8.5	Final versions of application and procurement documents	34
5.8.6	Qualification and acceptance review	35
6	Quality assurance system	36
6.1	General.....	36
6.2	Review meetings	36
6.3	Risk assessment and risk management.....	38
7	Development documentation	39
7.1	General.....	39
7.2	Management documentation	39

7.3	Design documentation	40
7.3.1	General	40
7.3.2	Definition phase documentation	42
7.3.3	Architectural design documentation	42
7.3.4	Detailed design documentation	42
7.3.5	Layout documentation	43
7.3.6	Design validation documentation	43
7.4	Application and procurement documents	43
7.4.1	Data sheet	43
7.4.2	Application note	43
7.4.3	Detail specification	44
8	Deliverables	45
8.1	General	45
8.2	Deliverable items	45
	Annex A (normative) ASIC and FPGA control plan (ACP) – DRD	46
	Annex B (normative) ASIC and FPGA development plan (ADP) – DRD	48
	Annex C (normative) ASIC and FPGA requirements specification (ARS) – DRD	50
	Annex D (normative) Feasibility and risk assessment report (FRA) - DRD	52
	Annex E (normative) Verification plan (VP) – DRD	53
	Annex F (normative) Design validation plan (DVP) – DRD	54
	Annex G (normative) Data sheet – DRD	55
	Annex H (normative) Detail specification (DS) – DRD	57
	Annex I (normative) Experience summary report – DRD	59
	Annex J (informative) Document requirements list and configuration items to be delivered	60
	Bibliography	61
	Figures	
	Figure 5-1: Development flow (example)	17
	Figure 7-1: Design documentation	41
	Tables	
	Table J-1 : Deliverables of the ASIC and FPGA development	60

Foreword

This document (EN 16602-60-02:2014) has been prepared by Technical Committee CEN/CLC/TC 5 "Space", the secretariat of which is held by DIN.

This standard (EN 16602-60-02:2014) originates from ECSS-Q-ST-60-02C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by March 2015, and conflicting national standards shall be withdrawn at the latest by March 2015.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

Introduction

The added responsibilities of developing custom designed devices, as opposed to using off-the-shelf components, make certain management activities crucial to the success of the procurement programme. This was already considered by the applicable standard for "Space product assurance - EEE components", ECSS-Q-ST-60 that classifies custom designed devices, such as ASIC components, under "Specific components", for which particular requirements are applicable.

The supplier accepts requirements for the development of custom designed components within the boundaries of this standard based on the requirements of the system and its elements, and takes into consideration the operational and environmental requirements of the programme.

The supplier implements those requirements into a system which enables to control for instance the technology selection, design, synthesis and simulation, layout and design validation in a schedule compatible with his requirements, and in a cost-efficient way.

1

Scope

This Standard defines a comprehensive set of requirements for the user development of digital, analog and mixed analog-digital custom designed integrated circuits, such as application specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs). The user development includes all activities beginning with setting initial requirements and ending with the validation and release of prototype devices.

This Standard is aimed at ensuring that the custom designed components used in space projects meet their requirements in terms of functionality, quality, reliability, schedule and cost. The support of appropriate planning and risk management is essential to ensure that each stage of the development activity is consolidated before starting the subsequent one and to minimize or avoid additional iterations. For the development of standard devices, such as application specific standard products (ASSPs) and IP cores, and devices which implement safety related applications, additional requirements can be included which are not in the scope of this document.

The principal clauses of this Standard correspond to the main concurrent activities of a circuit development programme. These include:

- ASIC and FPGA programme management,
- ASIC and FPGA engineering,
- ASIC and FPGA quality assurance.

The provisions of this document apply to all actors involved in all levels in the realization of space segment hardware and its interfaces.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2

Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system – Glossary of terms
EN 16602-10	ECSS-Q-ST-10	Space product assurance – Product assurance management
EN 16602-20	ECSS-Q-ST-20	Space product assurance – Quality assurance
EN 16602-30	ECSS-Q-ST-30	Space product assurance – Dependability
EN 16602-60	ECSS-Q-ST-60	Space product assurance – Electrical, electronic and electromechanical (EEE) components
EN 16603-10	ECSS-E-ST-10	Space engineering – System engineering general requirements
EN 16601-10	ECSS-M-ST-10	Space project management – Project planning and implementation
EN 16601-10-01	ECSS-M-ST-10-01	Space project management – Organization and conduct of reviews
EN 16601-40	ECSS-M-ST-40	Space project management – Configuration and information management

Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 application specific integrated circuit (ASIC)

full custom or semi custom designed monolithic integrated circuit that can be digital, analog or a mixed function for one user

3.2.2 ASIC technology

totality of all elements required for the design, manufacture and test of ASIC components

NOTE Design tools and their description, cell libraries, procedures, design rules, process line and test equipment.

3.2.3 application specific standard products (ASSP)

ASICs designed to make standard products that are made available to a broader range of applications

NOTE ASSPs are most often are provided with a VHDL model and disseminated with documentation.

3.2.4 block diagram

abstract graphical presentation of interconnected named boxes (blocks) representing an architectural or functional drawing

3.2.5 cell

specific circuit function including digital or analog basic blocks

3.2.6 cell library

collection of all mutually compatible cells which conforms to a set of common constraints and standardized interfaces designed and characterized for a specified technology

3.2.7 data sheet

detailed functional, operational and parametric description of a component

NOTE A data sheet can include, for instance, a block diagram, truth table, pin and signal description, environmental, electrical and performance parameters, tolerances, timing information, and package description.

3.2.8 design flow

selection and sequence of engineering methods and tools to be applied during the implementation of the design

3.2.9 design for test (DFT) structure

technique used to allow a complex integrated circuit (IC) to be tested

NOTE This can include any mechanism aimed to provide better observability or commandability of internal nodes of the chip not accessible through primary inputs and outputs.

3.2.10 design iteration

design changes that occur in any single phase or between two consecutive phases as defined in the ASIC and FPGA development plan, before the design is released for prototype implementation

3.2.11 detail specification

procurement specification according to ESCC format that defines, for instance, the maximum ratings, parameter limitations, mechanical outline, pin description and screening requirements

3.2.12 development step

major step of the development flow for the ASIC and FPGA development

NOTE Definition phase, architectural design, detailed design, layout, prototype implementation and design validation.

3.2.13 fault coverage

measure expressed as a percentage of the proportion of actually detectable faults versus all possible faults in a digital circuit, for a given set of test patterns and with respect to a specific fault model

3.2.14 field programmable gate array (FPGA)

standard semiconductor device that becomes customized when programmed by the user with the FPGA specific software and hardware tools

3.2.15 floorplan

abstracted, scaled layout drawing of the die, outlining the form, size and position of the major functional blocks and the pads including power and ground lines, clock distribution and interconnect channels

3.2.16 HDL model

textual model based on a hardware description language (but not a piece of software in itself) suitable for the behavioural or structural description, simulation and by choosing a suitable level of abstraction for automatic netlist generation

3.2.17 intellectual property (IP) core

design element that implements a self-standing function or group of functions for which ownership rights exist

NOTE 1 IP core can be acquired by a customer, for a given price and under an owner-defined license agreement specifying the customer's acquired rights.

NOTE 2 IP core can be supplied as an HDL file (e.g. synthesizable VHDL code or gate-level netlist) and with the essential complementary documentation that allows the customer to successfully integrate and use it in a system (e.g. User's manual and verification files).

3.2.18 macrocell

module that contains complex functions in a manufacturer's cell library built up out of hard-wired primitive cells

3.2.19 netlist

formatted list of cells (basic circuits) and their interconnections

3.2.20 prototype device

fabricated ASIC or programmed FPGA used to validate the new design in respect to functionality, performance, operation limits and compatibility with its system

3.2.21 redesign

design changes which affect more than two consecutive phases of the ASIC and FPGA development or design changes that are implemented after prototype implementation

3.2.22 stimuli

input data set for simulation or test to show a specific functionality or performance of a device

3.2.23 test pattern

simulation stimuli and its expected responses (considering specific constraints to meet test equipment requirements) used to show correct behaviour of a device

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
ACP	ASIC and FPGA control plan
ADP	ASIC and FPGA development plan
ARS	ASIC and FPGA requirements specification
ASCII	American standard code for information interchange
ASIC	application specific integrated circuit
ASSP	application specific standard product
DD	design documentation
DDR	detailed design review
DFT	design for test
DRC	design rule check
DVP	design validation plan
EDA	electronic design automation
EDIF	electronic design interchange format
ERC	electrical rule check
ESCC	European Space Components Coordination
FM	flight module part
FPGA	field-programmable gate array
FRA	feasibility and risk analysis report
GDS	graphic design system (industry standard graphics entry tool)
HDL	hardware description language
Note: This term used in general for the various hardware description language which are applied for coding during design phase such as VHDL and verilog.	
IDMP	input data for mask or programming file generation
IEEE	Institute of Electrical and Electronics Engineers
IP	intellectual property
MoM	minutes of meeting
P&R	place and route
JTAG	joint test action group
LVS	layout vs. schematic check
NCC	netlist comparison check
QML	qualified manufacturer list
RTL	register transfer logic
SEU	single event upset
VHDL	VHSIC hardware description language

ASIC and FPGA programme management

4.1 General

4.1.1 Introduction

- a. The supplier shall establish and implement an ASIC and FPGA development, as part of the component programme (in conformance with ECSS-Q-ST-60), that ensures full conformance with the requirements of the project as defined by the customer in line with this standard.

4.1.2 Organization

- a. The supplier shall establish and maintain an organization for the management of the ASIC and FPGA programme.
- b. The organization shall comply with the requirements specified in ECSS-Q-ST-10.
- c. In case of major problems, the development team, as allocated in the development plan (see 4.3.1), shall directly report to the component advisory board as defined in ECSS-Q-ST-60.

4.1.3 Planning

- a. The supplier shall ensure that:
 - 1. the ASIC and FPGA developments that are necessary for the implementation of the ASIC and FPGA programme are planned, documented and implemented, and
 - 2. preventive or corrective actions are initiated whenever there is evidence of possible schedule or technical problems.

4.2 ASIC and FPGA control plan

- a. The supplier shall prepare an ASIC and FPGA control plan (ACP) in conformance with the DRD in Annex A.

4.3 Management planning tools

4.3.1 ASIC and FPGA development plan

- a. The supplier shall prepare a detailed ASIC and FPGA development plan (ADP) in conformance with the DRD in Annex B.
- b. The supplier shall maintain the ADP after the requirements are settled and the feasibility and risk for the ASIC and FPGA development is assessed.

4.3.2 Verification plan

- a. The supplier shall establish a verification plan in conformance with the DRD in Annex E.
- b. The verification plan shall define how the functionality and non-functional requirements stated in the definition phase documentation are demonstrated at all levels of modelling.

4.3.3 Design validation plan

- a. The supplier shall establish a design validation plan (DVP) in conformance with the DRD in Annex F.
- b. The DVP shall specify the measurements to be performed on the prototypes.

NOTE Those measurements allow verifying that the implemented devices contain the functionality and the characteristics they are designed for.

4.4 Experience summary report

- a. At the end of the ASIC and FPGA development cycle, the supplier should establish an experience summary report in conformance with the DRD in Annex I.

NOTE The experience summary report can be written in the frame of the supplier's continued quality improvement activities in order to establish economic and efficient development and test requirements for expected future projects.