

**DIN EN 16602-60-12**

ICS 49.140

**Raumfahrtproduktsicherung –  
Design, Auswahl, Beschaffung und Nutzung von MMIC;  
Englische Fassung EN 16602-60-12:2014**

Space product assurance –

Design, selection, procurement and use of die form monolithic microwave integrated circuits (MMICs);

English version EN 16602-60-12:2014

Assurance produit des projets spatiaux –

Conception, sélection, approvisionnement et utilisation de circuits intégrés monolithique hyperfréquence de forme die;

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## **Nationales Vorwort**

Dieses Dokument (EN 16602-60-12:2014) wurde vom Technischen Komitee CEN/CLC/TC 5 „Raumfahrt“ erarbeitet, dessen Sekretariat vom DIN (Deutschland) gehalten wird.

Das zuständige deutsche Normungsgremium ist der Arbeitsausschuss NA 131-10-01 AA „Interoperabilität von Informations-, Kommunikations- und Navigationssystemen“ im DIN-Normenausschuss Luft- und Raumfahrt (NL).

Dieses Dokument (EN 16602-60-12:2014) basiert auf ECSS-Q-ST-60-12C.

Dieses Dokument enthält unter Berücksichtigung des DIN-Präsidialbeschlusses 1/2004 nur die englische Originalfassung von EN 16602-60-12:2014.

Dieses Dokument wurde speziell zur Behandlung von Raumfahrtsystemen erarbeitet und hat daher Vorrang vor jeglicher Europäischer Norm, da es denselben Anwendungsbereich hat, jedoch über einen größeren Geltungsbereich (z. B. Luft- und Raumfahrt) verfügt.

## Nationaler Anhang NA (informativ)

### Begriffe und Abkürzungen

## 3 Begriffe und Abkürzungen

### 3.1 Begriffe aus anderen Normen

Für die Anwendung dieses Dokuments gelten die Begriffe und Definitionen nach ECSS-S-ST-00-01.

Für die Anwendung dieses Dokuments gilt der folgende Begriff nach ECSS-Q-ST-60-05:

#### **Prozessidentifikationsdokument**

### 3.2 Für diese Norm spezifische Begriffe

#### 3.2.1

##### **Chargenlos**

Wafer aus den gleichen Ausgangswerkstoffen, die im Fertigungsablauf (Diffusion, Metallisierung und Passivierung) in einem begrenzten und kontrollierten Zeitraum gemeinsam verarbeitet werden

**ANMERKUNG** Damit die Verarbeitungsschritte rückverfolgt werden können, werden ein Chargenlos und jeder Wafer mit einem eindeutigen Kennzeichen oder Code bezeichnet.

#### 3.2.2

##### **Prüfung der Designregeln**

Kontrollverfahren zur Überprüfung, ob die Designregeln erfüllt sind

**ANMERKUNG 1** Die Designregeln werden im Allgemeinen vom Zulieferer erstellt.

**ANMERKUNG 2** Die Überprüfung der Designregeln erfolgt mit Hilfe von Software.

#### 3.2.3

##### **Konstrukteur**

##### **Entwickler**

Organisation, die für das Design der MMICs verantwortlich ist

#### 3.2.4

##### **Die-Los**

##### **Dice-Los**

alle Dies, die aus einem einzigen Waferlos stammen

#### 3.2.5

##### **Prüfung der elektrischen Regeln**

Kontrollverfahren zur Überprüfung, ob die elektrischen Regeln erfüllt sind

**ANMERKUNG** Die elektrischen Regeln werden im Allgemeinen vom Hersteller erstellt.

#### 3.2.6

##### **evaluierter Prozess**

ausgereifte Technologie, die zum Nachweis der Leistungs- und Zuverlässigkeitsgrenzen einer Reihe von elektrischen Tests und Umweltprüfungen erfolgreich unterzogen wird

**ANMERKUNG 1** ECSS-Q-ST-60-01 enthält eine Liste der evaluierten Prozesse.

**ANMERKUNG 2** Die Spezifikation ESCC269010 definiert die Anforderungen an die Evaluierung.

### 3.2.7

#### **Hersteller**

Wafer-Fabrik, die für die Fertigung der MMICs verantwortlich ist

### 3.2.8

#### **Prozesskontrollmonitor**

Testgerät, das vom Zulieferer verwendet wird, um die Stabilität des Fertigungsprozesses mit Hilfe von Kontrollen, die während eines Zyklus der Waferherstellung durchgeführt werden, zu beurteilen

ANMERKUNG Der PCM wird bei jedem Waferlos mehrmals (je nach Hersteller) eingesetzt. Die mit dem PCM gewonnenen Messwerte werden verwendet, um den Wafer entsprechend den im Design-Handbuch festgelegten relevanten DC- und RF-Kriterien anzunehmen oder zu verwerfen.

### 3.2.9

#### **Fertigungslos**

Gerätetypen, die in der gleichen Fertigungsanlage aus den gleichen Rohstoffen gefertigt wurden und nach den gleichen Fertigungsverfahren und -kontrollen mit der gleichen Art von Geräten verarbeitet wurden

ANMERKUNG Ein Fertigungslos darf aus einem oder mehreren Chargenlosen bestehen.

### 3.2.10

#### **qualifizierter Prozess**

Prozess, der einem formellen Qualifikationstest erfolgreich unterzogen wurde

ANMERKUNG Die Spezifikation ESCC 20100 definiert die Anforderungen an die Qualifikation.

### 3.2.11

#### **Maske**

durch das Design auf Maskenebene definierter Bereich von Schaltkreis-Layouts (MMIC, TCV, DEC, PCM) zur Vervielfältigung über den gesamten Wafer während der MMIC-Fertigung

### 3.2.12

#### **statistische Prozesskontrolle**

Mittel zur Kontrolle der Qualität und der Stabilität des technologischen Prozesses

ANMERKUNG SPC wird bei verschiedenen Fertigungsschritten zur Messung und Analyse der Schlüsselparameter unter Verwendung geeigneter Verfahren implementiert.

### 3.2.13

#### **Kachelgrafik**

#### **Kachel**

siehe Maske

### 3.2.14

#### **Nutzer**

Person, die für die Integration der MMICs auf höherer Ebene verantwortlich ist

ANMERKUNG Beispiel: MMICs werden von Nutzern beispielsweise in Module, Hybride oder Geräte integriert.

### 3.2.15

#### **validiertes Design**

Design, das einem Annahmetest und einem LAT-Test des MMIC-Nutzers erfolgreich unterzogen wird

### 3.2.16

#### **validierter Prozess**

Prozess, der beurteilt oder qualifiziert wird

**3.2.17****Waferlos**

Wafer, die aus einem oder mehreren Losen gefertigt wurden

ANMERKUNG Je nach Prozessfortschritt wird ein Waferlos wie folgt definiert:

- Fall 1 (nicht beurteilter oder qualifizierter Prozess): ein Waferlos ist ein einzelner Wafer;
- Fall 2 (beurteilter oder qualifizierter Prozess und neues MMIC-Design): ein Waferlos ist ein Chargenlos;
- Fall 3 (ausgereifter Prozess und sich wiederholendes MMIC-Design): ein Waferlos wird als Fertigungslos aus 4 Chargen angesehen, die innerhalb von 3 Monaten gefertigt wurden.

**3.3 Abkürzungen**

Für die Anwendung dieser Norm gelten die Abkürzungen nach ECSS-S-ST-00-01 und die folgenden Abkürzungen.

| <b>Abkürzung</b> | <b>Bedeutung</b>                                       |                                               |
|------------------|--------------------------------------------------------|-----------------------------------------------|
| AQL              | annehmbare Qualitätsgrenzlage                          | (en: acceptance quality level)                |
| CTA              | Bauartzulassung des Schaltkreises                      | (en: circuit type approval)                   |
| DEC              | Dynamischer Auswertstromkreis                          | (en: dynamic evaluation circuit)              |
| DRC              | Prüfung der Designregeln                               | (en: design rules check)                      |
| ERC              | Prüfung der elektrischen Regeln                        | (en: electrical rule check)                   |
| HTRB             | Hochtemperatur-Sperrvorspannung                        | (en: high-temperature reverse bias)           |
| LAT              | Los-Abnahmetest                                        | (en: lot acceptance test)                     |
| LTRB             | Niedertemperatur-Sperrvorspannung                      | (en: low-temperature reverse bias)            |
| MMIC             | monolithische mikrowellenintegrierte Schaltung         | (en: monolithic microwave integrated circuit) |
| PAD              | Teilezulassungsdokument                                | (en: part approval document)                  |
| PCM              | Prozesskontrollmonitor                                 | (en: process control monitor)                 |
| PID              | Prozessidentifizierungs-Dokument                       | (en: process identification document)         |
| RGA              | Restgasanalyse                                         | (en: residual gas analysis)                   |
| SAM              | Akustische Mikroskopie<br>Rasterultraschallmikroskopie | (en: scanning acoustic microscopy)            |
| SEM              | Rasterelektronenmikroskop                              | (en: scanning electron microscope)            |
| SEU              | Einzelereignis-Upset                                   | (en: single event upset)                      |
| SPC              | Statistische Prozesslenkung                            | (en: statistical process control)             |
| TCV              | technologische Parameter-Teststruktur                  | (en: technological characterization vehicle)  |
| WAT              | Wafer-Abnahmetest                                      | (en: wafer acceptance testing)                |

— Leerseite —

English version

Space product assurance - Design, selection, procurement and  
use of die form monolithic microwave integrated circuits  
(MMICs)

Assurance produit des projets spatiaux - Conception,  
sélection, approvisionnement et utilisation de circuits  
intégrés monolithique hyperfréquence de forme die

Raumfahrtproduktsicherung - Design, Auswahl,  
Beschaffung und Nutzung von MMIC

This European Standard was approved by CEN on 13 March 2014.

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This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CEN and CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

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## Foreword

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This document (EN 16602-60-12:2014) has been prepared by Technical Committee CEN/CLC/TC 5 "Space", the secretariat of which is held by DIN.

This standard (EN 16602-60-12:2014) originates from ECSS-Q-ST-60-12C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by March 2015, and conflicting national standards shall be withdrawn at the latest by March 2015.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

## Introduction

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This Standard covers the design, selection, procurement and use of III-V monolithic microwave integrated circuits (MMICs) for space equipment.

It defines the design activity for the technical (methodology, phases to be followed) and quality (quality assurance, design review) aspects, and, the selection and procurement rules for these components taking into account whether or not the processes have been validated.

# 1

## Scope

---

This Standard applies to all types of MMIC (monolithic microwave integrated circuit) based on III-V compound materials for RF applications (i.e. frequency range  $\geq 1$  GHz). The requirements for the procurement of components in die form are defined.

It is not within the scope of this Standard to address packaged MMICs and discrete microwave components, these are dealt with in the relevant ESCC specification (ESCC 9010 and ESCC 5010).

This standard may be tailored for the specific characteristic and constraints of a space project in conformance with ECSS-S-ST-00.

## 2

# Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

| EN reference   | Reference in text | Title                                                                                   |
|----------------|-------------------|-----------------------------------------------------------------------------------------|
| EN 16601-00-01 | ECSS-S-ST-00-01   | ECSS system — Glossary of terms                                                         |
| EN 16602-30-11 | ECSS-Q-ST-30-11   | Space product assurance — Derating -- EEE components                                    |
| EN 16602-60    | ECSS-Q-ST-60      | Space product assurance - Electrical, electronic and electromechanical (EEE) components |
| EN 16602-60-05 | ECSS-Q-ST-60-05   | Space product assurance — Generic requirements for hybrids                              |
|                | MIL-STD-883       | Tests methods and procedures for microelectronics                                       |
|                | ESCC 20600        | Preservation, packaging and despatch of ESCC electronic components                      |
|                | ESCC 24600        | Minimum quality management system requirements                                          |
|                | ESCC 2049010      | Internal visual inspection of monolithic microwave devices                              |
|                | ESCC 2439010      | Requirements for capability approval of MMICs                                           |
|                | ESCC 9010         | Generic specification for MMICs                                                         |

## Terms, definitions and abbreviated terms

---

### 3.1 Terms from other standards

For the purpose of this document, the terms and definitions given in ECSS-S-ST-00-01 apply.

For the purpose of this document, the following term from ECSS-Q-ST-60-05 applies:

**process identification document**

### 3.2 Terms specific to the present document

#### 3.2.1 batch lot

wafers from the same basic raw materials processed as a single set in the manufacturing sequence (diffusion, metallization and passivation process) in a limited and controlled period of time

NOTE A unique identifier or code is assigned to a batch lot and to each wafer for processing traceability purposes.

#### 3.2.2 design rules check

control procedure for verifying that design rules have been satisfied

NOTE 1 Design rules checks are generally issued by the supplier.

NOTE 2 DRC is performed using software.

#### 3.2.3 designer

organization responsible for the design of the MMICs

#### 3.2.4 die lot

set of all dies coming from a single wafer lot

#### 3.2.5 electrical rule check

control procedure for verifying that the electrical rules have been satisfied

NOTE Electrical rules are generally issued by the manufacturer.

### 3.2.6 evaluated process

mature technology that has been successfully submitted to a set of electrical and environmental testing to demonstrate performance and reliability limits

NOTE 1 ECSS-Q-ST-60-01 contains a list of evaluated processes.

NOTE 2 The ESCC 2269010 specification defines the requirements for the evaluation.

### 3.2.7 manufacturer

foundry responsible for the manufacturing of the MMICs

### 3.2.8 process control monitor

test vehicle used by the supplier to assess the stability of the manufacturing process by means of controls conducted during a wafer production cycle

NOTE The PCM is repeated a number of times (depending on the manufacturers) on each wafer lot. The measurements taken during the PCM are used to accept or reject the wafer according to the relevant DC and RF criteria defined in the design manual.

### 3.2.9 production lot

device types manufactured from the same basic raw materials on the same production line, processed under the same manufacturing techniques and controls using the same type of equipment

NOTE A production lot may be composed of one or many batch lots.

### 3.2.10 qualified process

process that has been successfully submitted to a formal qualification testing

NOTE The ESCC 20100 specification defines the requirements for the qualification.

### 3.2.11 reticule

group of circuit layouts (MMIC, TCV, DEC, PCM) defined by design at the mask level, for duplication over the entire wafer during the MMIC manufacturing

### 3.2.12 statistical process control

tool to control the quality and the stability of the technological process

NOTE SPC is implemented by measuring key parameters during the different manufacturing steps and their analysis using appropriate methods.

### 3.2.13 tile

See **reticule**

#### 3.2.14 user

entity responsible for the integration of the MMICs at upper level

NOTE Example: MMICs are integrated by users into, for example, modules, hybrids, piece of equipment.

#### 3.2.15 validated design

design that is successfully submitted to application approval testing and an MMIC user LAT test

#### 3.2.16 validated process

process that is evaluated or qualified

#### 3.2.17 wafer lot

wafers manufactured from one or more batch lots

NOTE Depending on the maturity of the process a wafer lot is defined as follows:

- Case 1 (non-evaluated or qualified process): a wafer lot is a single wafer.
- Case 2 (evaluated or qualified process and new MMIC design): a wafer lot is one batch lot.
- Case 3 (mature process and recurrent MMIC design): a wafer lot is considered to be a production lot of 4 batches manufactured within a 3 month period.

### 3.3 Abbreviated terms

For the purpose of this standard, the abbreviated terms of ECSS-S-ST-00-01 and the following apply:

| Abbreviation | Meaning                                 |
|--------------|-----------------------------------------|
| AQL          | acceptance quality level                |
| CTA          | circuit type approval                   |
| DEC          | dynamic evaluation circuit              |
| DRC          | design rules check                      |
| ERC          | electrical rule check                   |
| HTRB         | high-temperature reverse bias           |
| LAT          | lot acceptance test                     |
| LTRB         | low-temperature reverse bias            |
| MMIC         | monolithic microwave integrated circuit |
| PAD          | part approval document                  |
| PCM          | process control monitor                 |
| PID          | process identification document         |