DIN EN 16602-70-60

ICS 31.180; 49.140

Entwurf

Einsprüche bis 2018-02-08
Vorgesehen als Ersatz für
DIN EN 16602-70-10:2015-05
und
DIN EN 16602-70-11:2015-05

Raumfahrtproduktsicherung – Qualifizierung und Beschaffung von Leiterplatten; Englische Fassung prEN 16602-70-60:2017

Space product assurance –
Qualification and Procurement of printed circuit boards;
English version prEN 16602-70-60:2017

Assurance produit des projets spatiaux –
Qualification et approvisionnement des circuits imprimés;
Version anglaise prEN 16602-70-60:2017

Anwendungswarnvermerk

Dieser Norm-Entwurf mit Erscheinungsdatum 2017-12-08 wird der Öffentlichkeit zur Prüfung und Stellungnahme vorgelegt.

Weil die beabsichtigte Norm von der vorliegenden Fassung abweichen kann, ist die Anwendung dieses Entwurfs besonders zu vereinbaren.

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Gesamtumfang 280 Seiten

DIN-Normenausschuss Luft- und Raumfahrt (NL)

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Nationales Vorwort

Dieses Dokument (prEN 16602-70-60:2017) wurde vom Technischen Komitee CEN/CLC/TC 5 „Raumfahrt“ erarbeitet, dessen Sekretariat von DIN (Deutschland) gehalten wird.

Das zuständige deutsche Normungsgremium ist der Arbeitsausschuss NA 131-06-02 AA „Interoperabilität von Informations-, Kommunikations- und Navigationssystemen“ im DIN-Normenausschuss Luft- und Raumfahrt (NL).

Dieses Dokument (prEN 16602-70-60:2017) basiert auf ECSS-Q-ST-70-60C DIR 1.

Dieses Dokument wird DIN EN 16602-70-10:2015-05 und DIN EN 16602-70-11:2015-05 ersetzen.

Dieses Dokument enthält unter Berücksichtigung des DIN-Präsidialbeschlusses 1/2004 nur die englische Originalfassung von prEN 16602-70-26:2017.

Dieses Dokument wurde speziell zur Behandlung von Raumfahrtsystemen erarbeitet und hat daher Vorrang vor jeglicher Europäischer Norm, die denselben Anwendungsbereich hat, jedoch über einen größeren Geltungsbereich (z. B. Luft- und Raumfahrt) verfügt.

Änderungen

Gegenüber DIN EN 16602-70-10:2015-05 und DIN EN 16602-70-11:2015-05 wurden folgende Änderungen vorgenommen:

a) Zusammenführung der Inhalte von DIN EN 16602-70-10 und DIN EN 16602-70-11 in ein gemeinsames Dokument;

b) Inhalt technisch überarbeitet.

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Nationaler Anhang NA
(informativ)

Begriffe und Abkürzungen

Die Benummerung der folgenden Begriffe und Abkürzungen ist identisch mit der Benummerung in der englischen Fassung.

3.1 Begriffe aus anderen Normen

a) Für die Anwendung dieser Norm gelten die Begriffe nach ECSS-S-ST-00-01, insbesondere die folgenden Begriffe:

1) Kunde

2) Lieferant

ANMERKUNG Hinsichtlich einer Beschreibung der Rollen von Kunden und Lieferanten siehe 4.2.

b) Für die Anwendung dieser Norm gelten die Begriffe nach ECSS-Q-ST-70-12, insbesondere die folgenden Begriffe:

1) Restring

2) Bauelement in Flächenarray-Bauweise

3) Aspektverhältnis

4) Basiskupfer

5) Blindkontaktloch, Sackloch

6) Bond-Ply

7) Lagenaufbau

8) verborgenes Kontaktloch

9) Leiter

10) FR4-Material

11) Bohrlochwand-Abhebung

12) Wärmesenke

13) Durchverbindung mit hoher Packungsdichte

14) Zwischenschicht

15) Intraschicht

16) Laminat

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17) Microvia

18) No-Flow-Prepreg

19) funktionsuntüchtiges Pad

20) nichtmetallisierte Bohrung

21) Normal Pitch

22) Panel

23) Durchkontaktierung

24) Prepreg

25) Leiterplatte

26) Harzmangel

27) Serialisierung

28) Abstand

29) Stack

30) Leiterbahn

31) Via, Kontaktloch

32) X-, Y-Richtung

33) Z-Richtung

3.2 Für diese Norm spezifische Begriffe

3.2.1
automatische optische Inspektion (AOI)
Inspektionsverfahren mit automatischer Vorrichtung zum Nachweis des Leiterbilds auf einer Ätzschicht

3.2.2
Backdrill-Loch
Art des Kontaktlochs, bei dem auf einer Seite ein Teil seiner Metallisierung mittels tiefengesteuerter mechanischer Bohrung mit einem Bohrer mit einem etwas größeren Durchmesser entfernt wird

3.2.3
Los
Gruppe von Leiterplatten und Probeblechen, die durch die gleiche Konformitätsbescheinigung und den gleichen Traveller abgedeckt sind

ANMERKUNG 1 Ein Los wird etwa zeitgleich hergestellt. Siehe 6.7a.

ANMERKUNG 2 Die Begriffe „Los“ und „Arbeitsauftrag“ sind synonym.

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3.2.4
Blase
Delaminierung in Form einer örtlich begrenzten Aufwölbung und Trennung zwischen jeglichen Schichten eines Basismaterials für die Laminierung oder zwischen dem Basismaterial und der leitfähigen Folie oder der Schutzbeschichtung

[IPC-T-50M]

3.2.5
Anheben der sekundären Kupferlage
Trennung zwischen dem Harz im Blindkontaktloch und der auf der Oberfläche befindlichen sekundären Kupferlage

ANMERKUNG Das Anheben der sekundären Kupferlage kann als Verdickung und als Trennung in Form einer dünnen Linie wie in Tabelle 10-18 dargestellt deutlich werden.

3.2.6
Verunreinigung
<KONTEXT: Qualifikation und Beschaffung von Leiterplatten>
in dielektrisches Material eingebettetes Fremdmaterial

ANMERKUNG 1 Synonyme sind: Schäden durch Fremdkörper, Einschluss, Fremdmaterial, Bruchstücke, Verschmutzung.

ANMERKUNG 2 Die Verunreinigung kann in Form von organischen Substanzen, Metallen, Partikeln oder Fasern vorliegen.

3.2.7
Probeblech
kleiner Teil einer Prüfschaltung, der zur Bewertung der Qualitätskonformität durch spezielle Prüfungen und Inspektionen angewendet wird

ANMERKUNG 1 Das Probeblech wird als Teil eines Panels hergestellt und während der letzten Herstellungsphase davon getrennt. Das Probeblech ist deshalb mit den Leiterplatten im Paneel verbunden, mit dem es gleichzeitig hergestellt wurde.

ANMERKUNG 2 Der Begriff „Probeblech“ bezieht sich auf ein typisches Leiterbild, während der Begriff „IST-Probeblech“ sich auf das spezifische IST-Leiterbild bezieht.

[übernommen aus IPC-T-50M]

3.2.8
Deckschicht
dünnes dielektrisches Material, dass zum Einkapseln der Schaltung verwendet wird, am häufigsten für flexible Schaltanwendungen

ANMERKUNG Die Begriffe „Decklage“ und „Überzugsmaterial“ sind synonym.

3.2.9
Maserung
Zustand im Inneren von verstärktem Basismaterial, bei dem sich Glasfaserbündel vom Harz ablösen; nicht auf Gewebekreuzungen beschränkt

ANMERKUNG 1 Dieser Zustand äußert sich in Form zusammenhängender weißer Punkte oder Kreuze unter der Oberfläche des Basismaterials. Er steht üblicherweise im Zusammenhang mit thermischen oder mechanischen Spannungen. Maserung ist ein schwerwiegenderer Fehler als Gewebetrennung. Delaminierung ist eine weitere Verschlechterung der Maserung.

ANMERKUNG 2 Siehe auch „Gewebetrennung“.

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3.2.10
Delaminierung
Trennung der Gewebelagen eines Basismaterials, zwischen dem Basismaterial und einer leitfähigen Folie oder jegliche sonstige planare Trennung in einer PCB

ANMERKUNG Siehe auch „Blase“, die eine örtliche Delaminierung darstellt.

[IPC-T-50M]

3.2.11
destruktive physische Analyse (DPA)
Analysenverfahren mithilfe von Probenahme, Vergießen, Schleifen, Polieren und Inspektion, wodurch das Versuchsfahrzeug zerstört wird

ANMERKUNG Der Begriff „Schlifferstellung“ ist in etwa synonym.

3.2.12
Entnetzung
Zustand, der auftritt, wenn geschmolzenes Lot eine Oberfläche bedeckt und sich dann zurückzieht und unregelmäßig geformte Lothügel zurücklässt, die durch Flächen mit dünner Lotschicht ohne freiliegendes Grundmetall getrennt sind

[IPC-T-50M]

3.2.13
Schlacke
Oxide und andere Verunreinigungen, die sich auf der Oberfläche von geschmolzenem Lot bilden

[IPC-T-50M]

3.2.14
Rückätzung
Abstand zwischen dem Harz der Bohrlochwand und der Innenfolie

3.2.15
Fine-Pitch
Abstand zwischen Leiterbahnen oder Lötflächen, der kleiner als bei einem normalen Pitch ist

ANMERKUNG Pitch wird in 7.4 der ECSS-Q-ST-70-12 festgelegt.

3.2.16
flexibel
Leiterplattentechnik, bei der nur flexible Schichten in deren Aufbau angewendet werden.

ANMERKUNG Der Begriff „biegsam“ ist synonym.

3.2.17
Glaskompression
verformte Prepreg-Glasfaserbündel, die aufgrund eines profilierten Kupferleitbilds das Fehlen von Harz zwischen Glas und Kupfer verursachen

ANMERKUNG Siehe auch „Harzmangel“.

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3.2.18
Hofbildung
mechanisch verursachte Rissbildung oder Delaminierung auf oder unter der Oberfläche eines Basismaterials, üblicherweise in Form von aufgehellten Bereichen um Löcher oder sonstige mechanisch bearbeitete Bereiche

[IPC-T-50M]

3.2.19
Einschluss
metallische oder nichtmetallische Fremdkörper, die in einem Isolierstoff, einer leitfähigen Schicht, einem Überzug, einem Basismaterial oder einer Lötverbindung eingeschlossen sein können

[IPC-T-50M]

3.2.20
Leiterbahndefekt (ICD)
Trennung an der Schnittstelle zwischen Innenlage und Durchkontaktierung

ANMERKUNG 1 Der Begriff „innere Schichttrennung“ ist synonym.

ANMERKUNG 2 Siehe „Verschmierung“ für zusätzliche Erklärung.

[IPC-6012D]

3.2.21
Interconnect Stress Test (IST)
Prüfverfahren, bei dem ein spezielles IST-Probeblech und eine spezielle IST-Ausrüstung angewendet werden

3.2.22
IST-Probeblech
spezielles Prüfblech für den IST

ANMERKUNG Der Begriff „Probeblech“ bezieht sich auf ein typisches Leiterbild, während der Begriff „IST-Probeblech“ sich auf das spezifische IST-Leiterbild bezieht.

3.2.23
Schlüsselpersonal
Personal, das über Fachwissen verfügt und für definierte Bereiche der Produktion oder Produktsicherung verantwortlich ist

3.2.24
Layout
Gestaltung des Leiterbilds auf einer Schicht

3.2.25
Gewebetrennung
Zustand im Inneren von verstärktem Basismaterial, bei dem sich Glasfaserbündel vom Harz ablösen; auf Gewebekreuzungen beschränkt

ANMERKUNG 1 Dieser Zustand äußert sich in Form einzelner weißer Punkte oder „Kreuze“ unter der Oberfläche des Basismaterials. Er steht üblicherweise im Zusammenhang mit thermischen Spannungen oder Luftfeuchte.

ANMERKUNG 2 Siehe auch „Maserung“, was eine weitere Verschlechterung von Gewebetrennung ist.

[IPC-T-50M]

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3.2.26
Metallkern
auf die Leiterplatte aufgebrachte oder lokal darin eingebrachte dicke Metallschicht, die üblicherweise als Wärmesenke, Erdungsschicht oder Begrenzung der thermischen Ausdehnung angewendet wird

3.2.27
Fräsen
mechanisches Verfahren, bei dem mithilfe eines Fräsers ein Teil des Materials entfernt wird, das für eine Leiterplatte bezeichnend ist

NOTE Siehe auch „Routing“.

3.2.28
Mehrfachschicht
Leiterplattentechnik, bei der eine Laminierung von verschiedenen Kupferschichten und Durchkontaktierungen für Verbindungen angewendet wird

ANMERKUNG Nicht mehrschichtige Leiterplatten sind doppelseitige oder einseitige Leiterplatten. Siehe auch „sequentiell“.

3.2.29
Durchkontaktierung
(en: plated hole)
Bohrung, die als Zwischenschichtverbindung angewendet wird

ANMERKUNG PTH und Vias sind Arten von Durchkontaktierungen.

3.2.30
Leiterplattenhersteller
Unternehmen, das die Leiterplatte herstellt

ANMERKUNG Der Leiterplattenhersteller ist Lieferant für die Beschaffungsbehörde.

3.2.31
Leiterplattentechnik
Kategorie von Herstellungsprozessen, Materialien und Design für Leiterplatten

ANMERKUNG Beispiele für Leiterplattentechnik sind:

- starr, sequentiell, Polyimid
- starrflexibel, sequentiell, Polyimid
- starr, sequentiell, Epoxid
- starrflexibel, nicht sequentiell, Epoxid
- HDI mit Microvias
- Hochfrequenz
- flexibel und Sculptured Flex

3.2.32
Beschaffungsbehörde
Unternehmen, das die Leiterplatte beschafft

ANMERKUNG 1 Die Beschaffungsbehörde ist Kunde des Leiterplattenherstellers.

ANMERKUNG 2 Die Beschaffungsbehörde kann Lieferant für den Hauptauftragnehmer sein.

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3.2.33
Qualifikationsbehörde
Unternehmen, das die Leiterplattentechnik und den Leiterplattenhersteller qualifiziert

3.2.34
Hochfrequenz
RF
(en: radio frequency)
elektronische Funktionalität, bei der spezielle konstruktive Maßnahmen bei dielektrischem Material und beim Kupferleiterbild erforderlich sind, um die zeitabhängige Signalintegrität beizubehalten

ANMERKUNG 1 Der Begriff „Hochgeschwindigkeit“ ist synonym.

ANMERKUNG 2 Der Begriff „RF PCB“ identifiziert die Leiterplattentechnik.

3.2.35
starr
Leiterplattentechnik, bei der nur starre Schichten in ihrem Aufbau angewendet wird

3.2.36
starrflexibel
Leiterplattentechnik, bei der eine Kombination von starren und flexiblen Schichten in ihrem Aufbau angewendet werden

3.2.37
Routing
Layout und Verbindung von Leitern zwischen Durchkontaktierungen und Pads

ANMERKUNG Der Begriff „Routing“ wird auch für „Fräsen“ angewendet. Diese zweite Bedeutung wird zur Vermeidung von Missverständnissen nicht in ECSS-Q-ST-70-60 angewendet.

3.2.38
Kratzer
schmale Furche oder Nut in einer Oberfläche

ANMERKUNG Er ist üblicherweise flach und wird durch das Markieren oder Schrammen der Oberfläche mit einem spitzen oder scharfen Gegenstand verursacht.

[IEC 60194 (1999-04)]

3.2.39
Sculptured Flex
flexible Leiterplattentechnik, die profilierte Kupferleiterbahnen anwendet

ANMERKUNG Aviflex ist eine kommerzielle Kennzeichnung von Sculptured Flex.

3.2.40
sequentiell
Leiterplattentechnik, bei der mehr als ein Laminierungs- oder Bohrschritt angewendet wird

ANMERKUNG Der Begriff „sequentiell“ bedeutet auch, dass die Leiterplatte vom Typ „Mehrfachschicht“ ist Das Gegenteil ist „nichtsequentiell“.

3.2.41
sequentielles Via
Art des Via, durch das Schichten mit der gleichen Beschichtungsabfolge miteinander verbunden werden

ANMERKUNG Beispiele für sequentielle Vias sind Blindkontaktlöcher und verborgene Kontaktlöcher

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3.2.42
Skip Plating
örtlich fehlende Abscheidung der Beschichtung

ANMERKUNG Skip Plating kann beim stromlosen Kupferbeschichten auf Glas in der Bohrlochwand auftreten. Skip Plating kann auch am Oberflächenfinish auftreten.

3.2.43
Verschmierung
Basismaterial Harz, das die Schnittfläche zwischen der freiliegenden Kante eines Innenpads und der Durchkontaktierung abdeckt

ANMERKUNG 1 Die Übertragung von Harz wird üblicherweise durch den Bohrvorgang verursacht und während des Reinigungsprozesses entfernt. Die Begriffe „Harzverschmierung“ oder „Verschmieren“ sind synonym.

ANMERKUNG 2 Eine Verschmierung kann mit einem Leiterbahndefekt oder vice versa verwechselt werden. Eine Verschmierung ist das Vorhandensein von Harz, während ein Leiterbahndefekt eine Trennung von Klebstoff von der Kupferschicht ist.

[übernommen aus IPC-T-50M]

3.2.44
Prüfleiterbild
Teil der PCB oder des Probeblechs, der zu speziellen Prüfzwecken mit dem Kupferleiterbild im Zusammenhang steht

[übernommen aus IPC-T-50M]

3.2.45
Traveller
Dokumentation, die während der Herstellungsprozesse beim Los aufbewahrt wird, auf der die Reihenfolge der speziellen Prozesse aufgezeichnet wird

3.2.46
durchgehendes Via
Art des Via, das durch die gesamte Dicke der Leiterplatte gebohrt wird

3.2.47
Via-in-Pad
Art des Via, das sich unmittelbar unterhalb eines SMT-Pads befindet

3.2.48
Antrag auf Sonderfreigabe
schriftliche Vereinbarung zwischen Leiterplattenhersteller und Beschaffungsbehörde zur Lieferung von Leiterplatten mit einer Nichtkonformität zu einer Anforderung einer Spezifikation

ANMERKUNG 1 Die folgenden Begriffe sind synonym: „Konzessionsgesuch“, „Freistellungsantrag“, „Sonderfreigabeantrag“, „Abweichungsantrag“.

ANMERKUNG 2 Bei Raumfahrtprojekten haben die Begriffe RFW und RFD eine spezielle Bedeutung, wie in ECSS-Q-ST-70 festgelegt. Diese spezielle Bedeutung ist im Kontext mit der Leiterplattenbeschaffung nicht strikt anzuwenden.

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3.2.49
Gewebefreilegung
Oberflächenzustand des Basismaterials, bei dem unversehrte Glasfasern nicht vollständig mit Harz bedeckt sind

ANMERKUNG Siehe auch „Gewebestruktur“.

[IPC-T-50M]

3.2.50
Gewebestruktur
Oberflächenzustand des Basismaterials, bei dem ein Gewebemuster durch die unversehrten Gewebefasern vollständig durch Harz abgedeckt sind

ANMERKUNG Siehe auch „Gewebefreilegung“.

[IPC-T-50M]

3.2.51
Dochteffekt
Eindringen der Kupferschicht in das Dielektrikum der Bohrlochwand

ANMERKUNG Die Begriffe „Kupferinfiltration“ und „Kupfereintritt“ sind synonym.

3.2.52
Arbeitsanweisung
Qualitätsdokument, das die technischen Einzelheiten zu Prozessen, dem Materialeinsatz, Prüf- und Annahmekriterien beschreibt

ANMERKUNG 1 Die Begriffe „Herstellungsverfahren“, „Kontrollverfahren“ oder „Steuerungsverfahren“ sind synonym.

ANMERKUNG 2 Die Arbeitsanweisung kann Prozessablaufpläne, Produktionsunterlagen (z. B. Herstellungspläne, Traveller, Router, Arbeitsaufträge, Arbeitsablaufkarten) und Prüfbescheinigungen enthalten.

3.3 Abkürzungen

Für die Anwendung dieser Norm gelten die Abkürzungen in ECSS-S-ST-00-01 und die folgenden Abkürzungen:

Abkürzung	Bedeutung	
AAD	Bauelement in Flächenarray-Bauweise	(en: area array device)
AC	Wechselstrom	(en: alternating current)
AOI	automatische optische Inspektion	(en: automated optical inspection)
AR	im Lieferzustand	(en: as received)
CDR	kritisches Design-Review	(en: critical design review)
CIC	Kupfer-Invar-Kupfer	(en: copper-invar-copper)
CoC	Konformitätsbescheinigung	(en: certificate of conformance)
CTE	Wärmeausdehnungskoeffizient	(en: coefficient of thermal expansion)
Cu	Kupfer (Element)	(en: copper (element))

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Abkürzung	Bedeutung	
CVCM	gesammelte flüchtige, kondensierbare Bestandteile	(en: collected volatile condensable material)
DC	Gleichstrom	(en: direct current)
DML	deklarierte Materialliste	(en: declared material list)
DPA	destruktive physische Analyse	(en: destructive physical analysis)
DR	Entwurfsprüfung	(en: design review)
DRB	Lieferungs-Untersuchungsausschuss	(en: delivery review board)
DRD	Dokumenten-Anforderungsdefinition	(en: document requirements definition)
DSC	dynamische Differenzkalorimetrie	(en: differential scanning calorimetry)
DWV	Spannungsfestigkeit	(en: dielectric withstanding voltage)
EBB	Steckplatine	(en: elegant breadboard)
ECM	elektrochemische Migration	(en: electrochemical migration)
EM	technisches Modell, Engineering-Modell	(en: engineering model)
EOL	Lebensdauerende	(en: end of life)
EQM	technisches Qualifizierungsmodell	(en: engineering qualification model)
FAI	Erstmusterprüfung	(en: first article inspection)
FCSI	Abnahmeprüfung durch den Endkunden	(en: final customer source inspection)
FM	Flugmodell	(en: flight model)
FOD	Fremdkörperablagerung	(en: foreign article debris)
FR4	FR4-Material (aus Harz für Leiterplatten)	(en: type of epoxy resin for PCBs)
FS	Flugersatzmodell	(en: flight spare)
HDI	Durchverbindung mit hoher Packungsdichte	(en: high density interconnect)
ICD	Leiterbahndefekt	(en: interconnect defect)
IMC	intermetallische Verbindung	(en: intermetallic compound)
IPA	Isopropanol	(en: isopropanol)
IPC	Association Connecting Electronic Industries	
IST	Interconnect Stress Test	
KPI	Leistungskennzahl	(en: key performance indicator)
max	Maximum	(en: maximum)
min	Minimum	(en: minimum)
MIP	Hauptprüfpunkt	(en: mandatory inspection point)
MPCB	Untersuchungsausschuss für Materialien und Prozesse	(en: material and processes control board)
MRR	Herstellungsbereitschafts-Review	(en: manufacturing readiness review)
n. a.	nicht zutreffend	(en: not applicable)
NCR	Nichtkonformitätsbericht	(en: nonconformance report)
NRB	Nichtkonformitäts-Untersuchungsausschuss	(en: nonconformance review board)

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Abkürzung	Bedeutung	
OTD	fristgemäße Lieferung	(en: on time delivery)
PCB	Leiterplatte	(en: printed circuit board)
PCN	Prozessänderungsankündigung	(en: process change note)
PDR	vorläufiges Design-Review	(en: preliminary design review)
PFM	Flug-Prototypmodell	(en: proto flight model)
PID	Prozessidentifizierungs-Dokument	(en: process identification document)
PTH	Durchkontaktierung	(en: plated-through hole)
PTFE	Polytetrafluorethylen	(en: polytetrafluoroethylene)
QA	Qualitätssicherung	(en: quality assurance)
QM	Qualifizierungsmodell	(en: qualification model)
QML	Liste qualifizierter Hersteller	(en: qualified manufacturers list)
QPL	Liste qualifizierter Produkte	(en: qualified product list)
r. m. s.	Effektivwert	(en: root-mean-square)
R&D	Forschung und Entwicklung	(en: research and development)
Ref	Verweisung (für Tabellen in Abschnitt 10)	(en: reference (for tables in clause 10))
RF	Hochfrequenz	(en: radio frequency)
RFA	Genehmigungsantrag	(en: request for approval)
RML	Restmassenverlust	(en: residual mass loss)
RW	Simulation der Nacharbeit	(en: rework simulation)
SB	Lötbadprüfung	(en: solder bath float)
SMT	Oberflächenmontagetechnik	(en: surface mount technology)
SPC	statistische Prozesslenkung	(en: statistical process control)
sq	Quadrat (in der Einheit Ω/sq)	(en: square (in unit Ω/sq))
TBD	festzulegen	(en: to be defined)
TDR	Zeitbereichsreflektometrie	(en: time domain reflectometry)
T288	Zeit bis zur Delaminierung bei 288 °C	(en: time to delamination at 288 °C)
Td	Zersetzungstemperatur	(en: temperature of decomposition)
Tg	Glasübergangstemperatur	(en: temperature of glass transition)
TGA	thermogravimetrische Analyse	(en: thermogravimetric analysis)
TMA	thermomechanische Analyse	(en: thermomechanical analysis)
wk	Woche	(en: week)

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EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

DRAFT
prEN 16602-70-60

September 2017

ICS 31.180; 49.140

Will supersede EN 16602-70-10:2015, EN 16602-70-11:2015

English version

Space product assurance - Qualification and Procurement of printed circuit boards

Assurance produit des projets spatiaux - Qualification et approvisionnement des circuits imprimés

Raumfahrtproduktsicherung - Qualifizierung und Beschaffung von Leiterplatten

This draft European Standard is submitted to CEN members for enquiry. It has been drawn up by the Technical Committee CEN/CLC/TC 5.

If this draft becomes a European Standard, CEN and CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

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European Foreword

This document (prEN 16602-70-60:2017) has been prepared by Technical Committee CEN/CLC/TC 5 “Space”, the secretariat of which is held by DIN (Germany).

This document (prEN 16602-70-60:2017) originates from ECSS-Q-ST-70-60C DIR 1.

This document is currently submitted to the CEN ENQUIRY.

This document will supersede EN16602-70-10:2015 and EN16602-70-11:2015.

This document has been developed to cover specifically space systems and will the-refore have precedence over any EN covering the same scope but with a wider do-main of applicability (e.g.: aerospace).

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Introduction

PCBs are used for the mounting of electronic components to produce PCB assemblies that perform electrical functions. The PCBs are subjected to thermo-mechanical stress during assembly such as soldering of components, rework and repair under normal terrestrial conditions. In addition, the assembled PCBs are exposed to the launch and space environment. The reliability of the circuit depends on the robustness of the manufacturing processes, for which this standard specifies requirements. PCB technology needs detailed inspections to verify its reliability, which is specified by at qualification and procurement phases of the PCB technology.

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1 Scope

This standard specifies the requirements for the PCB manufacturer, the procurement authority and the qualification authority for qualification and procurement of PCB technology.

ECSS-Q-ST-70-60 is applicable for all types of PCBs, including sequential, rigid and flexible PCBs, sculptured flex, HDI and RF PCBs.

This standard can be made applicable for other products combining mechanical and electrical functionality using additive or reductive manufacturing processes, as used in PCB manufacturing. Examples of such products are slip-rings, bus bars and flexible flat cables.

This standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

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2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system — Glossary of terms
EN 16602-10-09	ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
EN 16602-20	ECSS-Q-ST-20	Space product assurance — Quality assurance
EN 16602-70	ECSS-Q-ST-70	Space product assurance — Material, mechanical parts and processes
EN 16602-70-02	ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
EN 16602-70-08	ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high-reliability electrical connections
EN 16602-70-12	ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
EN 16602-70-21	ECSS-Q-ST-70-21	Space product assurance — Flammability testing for the screening of space materials
EN 16602-70-22	ECSS-Q-ST-70-22	Space product assurance — Control of limited shelf-life materials
EN 16602-70-29	ECSS-Q-ST-70-29	Space product assurance — Determination of offgassing products from materials and assembled articles to be used in a manned space vehicle crew compartment
	IEC 60326-2- am 1 (1992-06)	Printed boards. Part 2: Test methods
	IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions
	IPC-A-600J (2016)	Acceptability of Printed Boards

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EN reference	Reference in text	Title
	IPC-T-50M (2015)	Terms and definitions for interconnecting and packaging electronic circuits
	IPC-TM-650	Test methods manual
	IPC-1710A (2004)	OEM Standard for Printed Board Manufacturers' Qualification Profile
	IPC-4101E (2017)	Specification for base materials for rigid and multilayer printed boards
	IPC-4103A-WAM1 (2014)	Specification for Base Materials for High Speed/ High Frequency Applications
	IPC-4203A (2013)	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
	IPC-4204A-WAM1 (2014)	Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry
	IPC-6012D (2015)	Qualification and performance specification for rigid printed boards
	IPC-6012DS (2015)	Space and military avionics applications addendum to IPC-6012D
	IPC-6013C (2013)	Qualification and Performance Specification for Flexible Printed Boards
	IPC-6018C (2016)	Qualification and Performance Specification for High Frequency (Microwave) Printed Boards
	IPC-6018CS (2016)	Space and Military Avionics Applications Addendum to IPC-6018C

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3 Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, and in particular the following terms:

1. customer
2. supplier

NOTE See clause 4.2 for a description of roles of customer and supplier.

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-12 apply, and in particular the following terms:

1. annular ring
2. area array device (AAD)
3. aspect ratio
4. basic copper
5. blind via
6. bond ply
7. build-up
8. buried via
9. conductor
10. FR4
11. hole wall pull away
12. heat sink
13. high density interconnect (HDI)
14. interlayer
15. intralayer
16. laminate
17. microvia
18. no-flow prepreg
19. non-functional pad

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20. non-pated hole
21. normal pitch
22. panel
23. plated through-hole (PTH)
24. prepreg
25. printed circuit board (PCB)
26. resin starvation
27. serialization
28. spacing
29. stack
30. track
31. via
32. X,Y direction
33. Z direction

3.2 Terms specific to the present standard

3.2.1 automated optical inspection (AOI)

inspection method using an automated equipment to verify the pattern on an etched layer

3.2.2 back-drilled via

type of via with part of its metallisation removed on one side by depth controlled mechanical drilling with a larger diameter drill

3.2.3 batch

group of PCBs and coupons that are covered by the same CoC and the same traveller

NOTE 1 A batch is processed approximately at the same time. See 6.7a.

NOTE 2 The terms "lot" and "work order" are synonymous.

3.2.4 blister

delamination in the form of a localized swelling and separation between any of the layers of a laminated base material, or between base material and conductive foil or protective coating

[IPC-T-50M]

3.2.5 cap lift

separation between resin in blind via and copper cap plating on surface

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NOTE Cap lift can be shown as bulging and as thin line separation, as shown in Table 10-18.

3.2.6 contamination

<CONTEXT: Qualification and procurement of PCBs>

foreign material embedded in dielectric material

NOTE 1 Synonyms are: FOD, inclusion, foreign material, debris, pollution.

NOTE 2 Contamination can be organic, metallic, particulate or fibres.

3.2.7 coupon

small piece of test circuitry that is used for quality conformance evaluation by specific tests and inspection

NOTE 1 The coupon is manufactured as part of a panel and at the final manufacturing stage it is separated from it. The coupon is thus associated with the PCBs within the panel, with which it was simultaneously manufactured.

NOTE 2 The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

[adapted from IPC-T-50M]

3.2.8 coverlay

thin dielectric material used to encapsulate circuitry, most commonly for flexible circuit applications

NOTE The terms 'cover layer' and 'cover material' are synonymous.

3.2.9 crazing

condition that occurs in reinforced laminate base material whereby glass fibre bundles are separated from the resin not limited to the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to thermally or mechanically induced stress. Crazing is a more severe defect than measling. Delamination is a further worsening of crazing.

NOTE 2 See also "measling".

3.2.10 delamination

separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a PCB

NOTE See also 'blister', which is a local delamination.

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[IPC-T-50M]

3.2.11 destructive physical analysis (DPA)

analysis method using sampling, potting, grinding, polishing and inspection which, thus, destroys the test vehicle

NOTE The term 'microsectioning' is approximately synonymous.

3.2.12 dewetting

condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the base metal not exposed

[IPC-T-50M]

3.2.13 dross

oxide and other contaminants that form on the surface of molten solder

[IPC-T-50M]

3.2.14 etchback

distance from resin of hole wall to innerlayer foil

3.2.15 fine pitch

spacing of tracks or pads that is more dense than for normal pitch

NOTE Pitch is specified in clause 7.4 of ECSS-Q-ST-70-12.

3.2.16 flexible

PCB technology that uses only flexible layers in its build up

NOTE The term 'flex' is synonymous.

3.2.17 glass compression

deformed glass fibre bundles of prepreg causing absence of resin between glass and copper due to profiled copper pattern

NOTE See also 'resin starvation'.

3.2.18 haloing

mechanically-induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features

[IPC-T-50M]

3.2.19 inclusion

foreign particle, metallic or non-metallic, that can be entrapped in an insulating material, conductive layer, plating, base material or solder connection

[IPC-T-50M]

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3.2.20 interconnect defect (ICD)

separation at the interface between internal layer and through-hole plating

NOTE 1 The term 'innerlayer separation' is synonymous.

NOTE 2 See 'smear' for additional explanation.

[IPC-6012D]

3.2.21 interconnect stress test (IST)

test method using a specific IST coupon and a specific IST equipment

3.2.22 IST coupon

specific coupon for IST

NOTE The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

3.2.23 key personnel

personnel with specialist knowledge responsible for defined production or product assurance areas

3.2.24 lay-out

design of the conductive pattern on a layer

3.2.25 measling

condition that occurs in laminated base material whereby glass fibre bundles are separated from the resin limited to the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or "crosses" that are below the surface of the base material. It is usually related to thermally-induced stress or humidity.

NOTE 2 See also "crazing", which is a further worsening of measling.

[IPC-T-50M]

3.2.26 metal core

layer or local insert of thick metal embedded inside the PCB usually used as a heat sink, grounding layer or restriction of thermal expansion

3.2.27 milling

mechanical method that removes a portion of the material outlining a PCB using a cutting bit

NOTE See also 'routing'.

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3.2.28 multilayer

PCB technology that uses lamination of several copper layers and plated holes for interconnection

NOTE PCBs that are not multilayer, are double-sided or single-sided PCBs. See also "sequential".

3.2.29 plated hole

hole that is used as an interlayer connection

NOTE Types of plated holes are PTH and vias.

3.2.30 PCB manufacturer

entity that manufactures the PCB

NOTE The PCB manufacturer is supplier to the procurement authority.

3.2.31 PCB technology

category of manufacturing processes, materials and design for PCBs

NOTE Examples of PCB technology are:

- Polyimide sequential rigid
- Polyimide sequential rigid/flex
- Epoxy sequential rigid
- Epoxy non-sequential rigid/flex
- HDI with microvias
- RF
- Flexible and sculptured flex

3.2.32 procurement authority

entity that procures the PCB

NOTE 1 The procurement authority is customer of the PCB manufacturer.

NOTE 2 The procurement authority can be supplier to the prime contractor.

3.2.33 qualification authority

entity that qualifies the PCB technology and PCB manufacturer

3.2.34 radio frequency (RF)

electronic functionality that requires specific design precautions on dielectric materials and copper pattern to maintain time dependant signal integrity

NOTE 1 The term 'high speed' is synonymous.

NOTE 2 The term 'RF PCB' identifies the PCB technology.

3.2.35 rigid

PCB technology that uses only rigid layers in its build-up

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3.2.36 rigid/flex

PCB technology that uses a combination of rigid and flexible layers in its build-up

3.2.37 routing

the lay-out and connection of conductors between plated-holes and pads

NOTE The term 'routing' is also used for 'milling'. This second meaning is not used in ECSS-Q-ST-70-60 to avoid confusion.

3.2.38 scratch

narrow furrow or grove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.2.39 sculptured flex

flexible PCB technology that uses profiled copper tracks

NOTE Aviflex is a commercial identification of sculptured flex.

3.2.40 sequential

PCB technology that uses more than one lamination or drilling step

NOTE The term 'sequential' also implies that the PCB is of type 'multilayer'. The opposite is 'non-sequential'.

3.2.41 sequential via

via type that interconnects layers within the same plating sequence

NOTE Examples of sequential vias are blind vias and buried vias.

3.2.42 skip plating

local missing deposition of plating

NOTE Skip plating can occur on electroless copper plating on glass in the hole wall. Skip plating can also occur on surface finish.

3.2.43 smear

base material resin that covers the interface between the exposed edge of an innerlayer pad and through-hole plating

NOTE 1 The resin transfer is usually caused by the drilling operation and removed during the desmear process. The term 'resin smear' or 'smearing' are synonymous.

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NOTE 2 The aspect of smear can be mistaken for interconnect defect, or vice versa. Smear is the presence of resin, whereas interconnect defect is an adhesive separation of copper plating.

[adapted from IPC-T-50M]

3.2.44 test pattern

part of the PCB or coupon that refers to the copper pattern for a specific test

[adapted from IPC-T-50M]

3.2.45 traveller

documentation kept with the batch during the manufacturing processes in which the order of specific processes are recorded

3.2.46 through-going via

type of via that is drilled through the entire thickness of the PCB

3.2.47 via-in-pad

type of via directly underneath a SMT pad

3.2.48 waiver request

written agreement between PCB manufacturer and procurement authority to deliver PCBs with a non-conformance to a requirement from a specification

NOTE 1 The following terms are synonymous: “request for concession”, “demande de derogation”, “request for waiver”, “request for deviation”.

NOTE 2 In space projects the terms RFW and RFD have specific meaning as specified in ECSS-Q-ST-70. This specific meaning does not strictly apply in the context of PCB procurement.

3.2.49 weave exposure

a base material surface condition in which unbroken fibres of woven glass are not completely covered by resin

NOTE See also ‘weave texture’.

[IPC-T-50M]

3.2.50 weave texture

a surface condition of base material in which a weave pattern of cloth is apparent although the unbroken fibres of woven cloth are completely covered by resin.

NOTE See also ‘weave exposure’.

[IPC-T-50M]

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3.2.51 wicking

infiltration of copper plating into the dielectric of the hole wall

NOTE The terms "copper infiltration" and "copper ingress" are synonymous.

3.2.52 work instruction

quality document that describes the technical details about processes, material usage, inspection and acceptance criteria

NOTE 1 The terms 'manufacturing procedure' or 'control procedure' or 'process instruction' are synonymous.

NOTE 2 Work instructions can include process flow charts, production documents (e.g. manufacturing plans, travelers, routers, work orders, process cards) and inspection documents.

3.3 Abbreviated terms

For the purpose of , the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
AC	alternating current
AOI	automated optical inspection
AR	as received
CDR	critical design review
CIC	copper-invar-copper
CoC	certificate of conformance
CTE	coefficient of thermal expansion
Cu	copper (element)
CVCM	collected volatile condensable material
DC	direct current
DML	declared materials list
DPA	destructive physical analysis
DR	design review
DRB	delivery review board
DRD	document requirements definition
DSC	differential scanning calorimetry
DWV	dielectric withstanding voltage
EBB	elegant breadboard

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Abbreviation	Meaning
ECM	electrochemical migration
EM	engineering model
EOL	end of life
EQM	engineering qualification model
FAI	first article inspection
FCSI	final customer source inspection
FM	flight model
FOD	foreign article debris
FR4	type of epoxy resin for PCBs
FS	flight spare
HDI	high density interconnect
ICD	interconnect defect
IMC	intermetallic compound
IPA	isopropanol
IPC	association connecting electronic industries
IST	interconnect stress test
KPI	key performance indicator
max	maximum
min	minimum
MIP	mandatory inspection point?
MPCB	material and processes control board
MRR	manufacturing readiness review
n. a.	not applicable
NCR	nonconformance report
NRB	nonconformance review board
OTD	on time delivery
PCB	printed circuit board
PCN	process change notice
PDR	preliminary design review
PFM	proto flight model
PID	process identification document
PTH	plated-through hole
PTFE	polytetrafluoroethylene
QA	quality assurance
QM	qualification model
QML	qualified manufacturers list
QPL	qualified product list
r. m. s.	root-mean-square

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Abbreviation	Meaning
R&D	research and development
Ref	reference (for tables in clause 10)
RF	radio frequency
RFA	request for approval
RML	residual mass loss
RW	rework simulation
SB	solder bath float
SMT	surface mount technology
SPC	statistical process control
sq	square (in unit Ω/sq)
TBD	to be defined
TDR	time domain reflectometry
T288	time to delamination at 288°C
Td	temperature of decomposition
Tg	temperature of glass transition
TGA	thermogravimetric analysis
TMA	thermomechanical analysis
wk	week

3.4 Nomenclature

The following nomenclature applies throughout this document:

a. The word “shall” is used in this Standard to express requirements. All the requirements are expressed with the word “shall”.

b. The word “should” is used in this Standard to express recommendations. All the recommendations are expressed with the word “should”.

NOTE It is expected that, during tailoring, recommendations in this document are either converted into requirements or tailored out.

c. The words “may” and “need not” are used in this Standard to express positive and negative permissions, respectively. All the positive permissions are expressed with the word “may”. All the negative permissions are expressed with the words “need not”.

d. The word “can” is used in this Standard to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS “may” and “can” have completely different meanings: “may” is normative (permission), and “can” is descriptive.

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e. The present and past tenses are used in this Standard to express statements of fact, and therefore they imply descriptive text.

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4 Principles

4.1 General

This standard specifies requirements for the manufacture, qualification, procurement, test and inspection of PCBs.

4.2 Roles

In the context of ECSS-Q-ST-70-60 the roles “PCB manufacturer”, “procurement authority” and “qualification authority” were explicitly introduced and defined in clause 3.2 to allow proper allocation of requirements.

4.3 List of conditions

The formulation ”in case the following conditions are met” indicates that all of the listed conditions are met, except when it is stated that only one or some of the conditions can be met.

4.4 References to acceptance criteria

Clause 10 includes tables to specify acceptance criteria for certain technological features. The technological features can be further subdivided in each table. This is indicated with a reference letter in the first column and abbreviated as “Ref x”. This allows cross referencing to specific line items in the table, rather than to an entire table. An example of this is “internal annular ring on an inner layer at the end of a blind via” which is cross referenced as Ref b in Table 10-1.

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5
QA for qualification

5.1 Qualified PCBs

a. Qualified PCBs for space applications shall meet the following conditions:

1. the PCB is procured in conformance with clauses 6 and 8,
2. the PCB is procured from a PCB manufacturer that is qualified in conformance with clauses 5 and 7 and as specified in the PID,
3. the PCB design is in conformance with the requirements of ECSS-Q-ST-70-12.

NOTE Some specific PCB technologies can be used that are not covered by a valid PID or by a company qualification. Procurement can be done under RFA, including tests for (delta) qualification and tests for procurement but it can exclude the qualification of the company. Examples of specific PCB technology are complex HDI, complex RF and flex technology that are under development. This is described in clauses 5.2 and 7.7.

b. The qualification of PCBs in conformance with this standard shall cover for a maximum operational temperature of 85 °C.

NOTE 1 This is also described in clause 1 "Scope" of ECSS-Q-ST-70-08 and clause 1 "Scope" of ECSS-Q-ST-70-38.

NOTE 2 This is in conformance with current rating requirements from clause 13.6.2 of ECSS-Q-ST-70-12.

NOTE 3 PCBs are not qualified for a specific voltage as this is depending on PCB design in conformance with ECSS-Q-ST-70-12.

5.2 Special PCB technology

a. PCBs manufactured using conventional PCB processes and ceramic filled laminate shall be in conformance with ECSS-Q-ST-70-60.

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NOTE This is opposed to ceramic substrates using thick film or thin film processes that conform to ESCC-2566000.

b. Flexible flat cables manufactured using conventional PCB processes shall be in conformance with ECSS-Q-ST-70-60.

NOTE 1 This is opposed to heaters that conform to ESCC-4009 or cables that conform to ESCC-3901.

NOTE 2 This technology can also be called "flexprint" or "ribbon flex".

NOTE 3 Conventional PCB processes include etching of copper clad flexible laminate and lamination of coverlay, among others. Encapsulation of separate copper strings or wires to form a flexible ribbon is not a conventional PCB process.

5.3 Qualification process

a. The process for PCB qualification shall contain the following stages:

1. request for qualification and associated documentation in conformance with clause 5.4,
2. evaluation of a technology sample in conformance with clause 5.7,
3. audit of the manufacturing facility in conformance with clause 5.8,
4. qualification programme in conformance with clause 5.9.

b. The approval from the qualification authority of the completed qualification shall be in conformance with clause 5.11.

5.4 Request for qualification

a. The PCB manufacturer shall send a formal request for qualification to the qualification authority.

b. The PCB manufacturer shall provide the company profile including the following information:

1. description of the manufacturer capabilities,
2. business plan with basic financial figures for sales and R&D

NOTE The business plan demonstrates a healthy economical business and a strong commitment to quality assurance for space products.

c. The PCB manufacturer shall demonstrate the heritage on the PCB technologies for which qualification is requested, by providing the types of technology and quantity of PCBs produced for non-space customers, industrial space customers and space agencies.

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NOTE This is in particular important for the approved surface finishes, such as hot oil reflowed tin-lead.

d. The PCB manufacturer shall provide a letter of support from the main industrial space customers.

e. The PCB manufacturer shall provide a preliminary strategic planning, indicating the following:

1. the space projects for which qualified PCBs are foreseen to be provided,
2. which current customers can benefit from possible qualification,
3. which new customers or orders can be gained in case qualification is achieved,
4. what technologies are foreseen to qualify initially and in the medium and longer term,
5. the internal resource estimate for achieving qualification,
6. a target schedule for all activities related to achieving qualification.

f. The PCB manufacturer shall provide the completed survey for assessment of the PCB manufacturer's capabilities in conformance with IPC-1710.

g. The PCB manufacturer shall demonstrate that it meets the requirements for quality assurance in conformance with clause 5.5.

5.5 Quality standards

a. The quality assurance requirements specified in ECSS-Q-ST-20 shall apply.

b. The PCB manufacturer shall manage nonconformances in accordance with ECSS-Q-ST-10-09.

c. The PCB manufacturer shall hold certification for its quality management system in conformance with ISO-9001:2016 and EN9100:2017 or demonstrate that he has a quality management system in line with the above standards.

5.6 Description of qualification vehicle

a. The PCB manufacturer shall provide the PCB definition dossier, in conformance with the DRD in Annex A of ECSS-Q-ST-70-12, to the qualification authority for approval of the qualification vehicle.

b. The qualification vehicle shall be representative of the highest technological complexity for which qualification is requested.

c. The design of the qualification test vehicle shall accommodate the tests specified in clause 7.

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NOTE Examples of test patterns are shown in IPC-2221B.

d. The design of the qualification vehicle shall be in conformance with requirements from ECSS-Q-ST-70-12.

e. The coupons that are included in the qualification vehicle shall be in conformance with the clauses 8.2.2 and 8.2.3.

f. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2a shall be performed on at least 3 PCBs and the coupons in conformance with Figure 7-1.

g. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2a should include a spare PCBs and spare coupons in conformance with Figure 7-1.

h. Delta qualification and qualification renewal in conformance with requirement 7.2 shall be performed on at least 1 PCB and associated coupons.

5.7 Evaluation

a. The requirements of clause 5.6 shall apply to the evaluation samples.

b. The submission of evaluation samples shall include PCB, coupons, microsections and documentation in conformance with requirement 5.14a.

c. A first set of evaluation samples should be evaluated by a third-party.

NOTE It is beneficial to request a third-party evaluation by a company with knowledge on evaluation in conformance with ECSS-Q-ST-70-60.

d. The test flow for evaluation shall be in conformance with requirements from clause 7.5.

NOTE 1 This test flow includes DPA of PCB and coupons and IST.

NOTE 2 The evaluation phase is intended as a relatively fast assessment of the quality to gain confidence in the product before initiating the full qualification programme.

e. The qualification authority shall perform the evaluation and issue the test report.

f. The qualification authority shall provide to the PCB manufacturer the authorization to proceed with the qualification in case the following conditions are met:

1. Evaluation is acceptable.

2. Assessment of the request for qualification, in conformance with the clause 5.4, is acceptable.

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NOTE It is the intention to perform a PCB evaluation only once. In case the first attempt fails, a second final opportunity for passing the evaluation successfully can be offered. The qualification process can be discontinued in case the evaluation fails or in case the schedule as agreed in the strategic planning is exceeded.

5.8 Audit

a. The qualification authority shall audit the manufacturing line.

b. The audit shall occur when PCB production is in progress.

c. Before the audit, the PCB manufacturer shall make the following documents available to the qualification authority for review and approval:

   1. PID in conformance with the DRD in Annex D;

   2. Qualification test plan in conformance with clause 7.1 including test description, test vehicle and schedule.

d. The qualification authority shall submit to the PCB manufacturer an audit checklist that verifies the requirements from ECSS-Q-ST-70-60 and its normative references one month prior to the date of the audit.

e. The PCB manufacturer shall provide the response to the audit checklist to the qualification authority at least one week prior to the date of the audit.

f. The response from the PCB manufacturer in the audit checklist shall include the following:

   1. compliance level as follows:

      (a) “compliant” or

      (b) “non-compliant” or

      (c) "partial compliant” or

      (d) “not applicable”,

   2. a comment explaining any non-compliance, partial compliance or non-applicability,

   3. references to work instructions that specify the verified requirement.

g. During the audit, the PCB manufacturer shall make the following documents available to the qualification authority:

   1. Documented information in conformance with EN9100:2017 clause 4.2.2

   2. Business process procedures, in conformance with EN9100

   3. Work instructions, in conformance with EN9100.

      NOTE 1 Quality manual is one possible type of Documented information from 5.8g.1.

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NOTE 2 See definition of work instructions in clause3.2.52.

h. In case of an audit for qualification renewal, the PCB manufacturer shall provide the following:

1. A collection of the QA reports in conformance with clause 5.13.
2. Lists of PCBs per PID supplied in conformance with ECSS-Q-ST-70-60 since the previous audit.

i. The qualification authority shall issue the audit report and any findings, in conformance with clause 5.8j.

NOTE The minutes of meeting can be the audit report.

j. Findings from the audit shall be categorised by the qualification authority as follows:

1. "Major non-conformance" is a non-conformance against ECSS-Q-ST-70-60 that is evaluated by the qualification authority as mandatory to disposition by a corrective action for successful audit closure.
2. "Minor non-conformance" is a non-conformance against ECSS-Q-ST-70-60 that is a longer term action for continuous improvement and therefore not preventing successful audit closure according to the qualification authority.
3. "Observation" is a recommendation or observation that does not prevent successful audit closure and that is not a non-conformance against ECSS-Q-ST-70-60.

k. The audit report and any findings shall be approved and signed by the PCB manufacturer and qualification authority.

l. Corrective actions from findings shall be added to the updated audit report or minutes of meeting of a delta audit.

m. The final conclusion of the audit process shall be provided in the final audit report or minutes of meeting.

5.9 Qualification test programme

a. The requirements of clause 5.6 shall apply to the qualification vehicle.

b. The PCB manufacturer shall perform the qualification tests as specified in the qualification test plan in conformance with requirement 7.2a and approved by the qualification authority in conformance with requirements 5.8c and 5.8k.

NOTE The PCB manufacturer can use labs from a third-party or from the customer to perform tests.

c. The PCB manufacturer shall issue the qualification test report in conformance with the DRD in Annex C.

d. The PCB manufacturer shall provide the qualification test report to the qualification authority for review and approval.

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e. The qualification authority may request to the PCB manufacturer an additional test vehicle or microsections for evaluation.

5.10 PID

a. The PCB manufacturer shall issue the PID in conformance with the DRD of Annex D.

b. The specific parts of the PID shall be issued, in conformance with D.2.1.2, for the following PCB technologies in separate documents:

1. Polyimide rigid
2. Polyimide rigid/flex
3. Epoxy rigid
4. Epoxy rigid/flex
5. HDI
6. RF
7. Flexible
8. Sculptured flex

5.11 Qualification approval

a. Upon successful qualification, the qualification authority shall issue a qualification letter in conformance with the DRD in Annex A.

b. The qualification authority shall publish the qualification status.

c. The reason for a change or updated qualification status shall be published as a comment to the qualification status.

NOTE The term "qualified" can be used to indicate a valid qualification status. The term "not qualified" can be used to indicate an invalid qualification status, for instance as a result of nonconformances during qualification renewal or as a result of an expired qualification period. The status is not definite and can be updated when new results are available. A comment is included to clarify the reason for the qualification status. A definite disqualification or discontinuation of PCB technology or PCB manufacturer can be indicated by deletion from the published list or by the terms "disqualified" or "discontinued".

d. The qualification authority shall grant qualification approval to the PCB manufacturer based on the acceptance of the evaluation in conformance with clause 5.7, the audit in conformance with clause 5.8 and the qualification programme in conformance with clause 5.9.

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e. The qualification approval shall be valid for a period of maximum two years.

f. In case nonconformances have been encountered, the qualification authority may grant a period of validity for the qualification that is shorter than two years.

NOTE One year is a commonly used qualification period to ensure a more frequent verification of the process control for a critical technology.

5.12 Process change

a. Process changes shall include process parameters, chemistry, material, equipment, process flow and inspections.

b. Process changes shall be categorised by the PCB manufacturer as “major” or “minor” in the PID.

c. Requests for major process changes shall be submitted to the qualification authority for approval.

d. The implementation of a major change shall be submitted to the qualification authority for approval.

e. Minor process changes may be implemented by the PCB manufacturer without prior approval of the qualification authority.

NOTE The PCN for a minor change includes the acceptable evaluation of the affected acceptance criteria in conformance with E.2.1b1.

f. For major and minor process changes, the PCB manufacturer shall issue a process change notice in conformance with the DRD in Annex E to the qualification authority.

g. All process change notices should be submitted to the procurement authority for information.

h. Major process change notices should be submitted to the procurement authority for approval.

5.13 QA report

a. The PCB manufacturer shall issue a QA report to the qualification authority in conformance with the DRD in Annex F.

b. The QA report shall be issued quarterly.

5.14 Qualification renewal

a. The PCB manufacturer shall submit to the qualification authority the following items for qualification renewal at least two months prior to expiration of the qualification:

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