



ANSI/EIA-5670000-1991
APPROVED: October 7, 1991

EIA SPECIFICATION

EIA Commercial Component Model Specification

EIA-5670000

OCTOBER 1991

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT



Approved For Use In
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(From Standards Proposal No. 2229 and 2229-A formulated under the cognizance of the VHDL Modelling Standards Committee)

Published by

ELECTRONIC INDUSTRIES ASSOCIATION
Engineering Department
2001 Pennsylvania Avenue N.W.
Washington, D.C. 20006

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EIA COMMERCIAL COMPONENT MODEL SPECIFICATION

1.0 SCOPE: The purpose of this specification is to define the contents and acceptance criteria of VHDL behavioral models for commercial electronic components. Full function VHDL models are addressed herein. Any subset models (i.e. those which do not incorporate all of the functions that the underlying component is capable of performing in accordance with its data sheet) are excluded.

2.0 APPLICABLE DOCUMENTS:

2.1 Professional, Industrial

- 2.1.1 Institute of Electrical and Electronic Engineers, Inc. Standard 1076-1987: VHDL Language Reference Manual (VHDL LRM).
- 2.1.2 JEDEC Standard Number 3-A, Standard Data Transfer Format Between Data Preparation System and Programmable Logic Device Programmer, May 1986
- 2.1.3 ANSI/IEEE Standard 91-1984, Graphic Symbols for Logic Functions, adopted 10 May 1984.
- 2.1.4 JEDEC Standard Number 99, Glossary of Microelectronic Terms, Definitions, and Symbols, June 1985.
- 2.1.5 JEDEC Standard Number 100, Terms, Definitions, and Letter Symbols for Microcomputer and Memory Integrated Circuits, October 1982.
- 2.1.6 JEDEC Standard Number 12-4, Method of Specification of Performance Parameters for CMOS Semicustom Integrated Circuits, April, 1987.
- 2.1.7 EIA Timing and Environmental Data Specification (PN-XXXX).
- 2.1.8 EIA Blank Detail Specification for Commercial Component Models, PN-2773.

2.2 Government

- 2.2.1 Data Item Description entitled Electronic Hardware Description of the VHSIC Hardware Description Language (VHDL), Identification Number DI-EGDS-80811.
- 2.2.2 MIL-STD-454 Standard General Requirements for Electronic Equipment, Revision L or later versions when issued.

3.0 REQUIREMENTS: The following paragraphs define the contents of the models and associated files together with application requirements:

3.1 VHDL VERSION: Models shall be written using the latest version of VHDL. The IEEE Standard 1076-1987 VHDL Language Reference Manual (per section 2.1.1 above) provides this definition. Areas of ambiguity are to be resolved by the IEEE VHDL Analysis and Standardization

Group, which is responsible for maintaining the VHDL 1076 standard.

3.2 MODEL TYPES: Full function behavioral (Procedural or Data Flow) models at the architectural level are required. Since this model type incorporates a VHDL entity declaration and a behavioral VHDL body (both of which must be readable by the user), it is also defined as a leaf level module in accordance with Section 10.2.1.1 of the VHDL DID. In acknowledgement of the fact that most simulations in the past have used structural models rather than behavioral, such models rewritten in VHDL are acceptable if they are authorized for release by the semiconductor company who originated the component design and as an objective they do not incur major simulator run time penalties. Moreover, mixtures of structural and behavioral models are acceptable for the same reasons, and such mixtures are especially applicable to Program Logic Devices, per Section 3.4.11, which contain fixed structural elements normally disclosed on data sheets.

3.3 MODEL CONTENTS: The component's functionality shall be accurately represented. The capabilities of the component and associated data incorporated in each model shall conform to the current version of referenced Government specifications for design and documentation purposes. It shall additionally incorporate model features needed by engineers for simulation convenience as identified in the following paragraphs:

3.3.1 ENTITY DECLARATION: Information appearing in the Entity Declaration shall include but not be limited to the following (in accordance with Section 10.2.2.1 of the referenced DID): Items 1. through 4. are declarations within the VHDL language, which are analyzable by software programs. Items 5. through 13. are required comments that may also be used by software programs and represent additional information needed by the user and the government. They shall either be included in the model itself or in a package to facilitate applicability to families of components for efficient model development and maintenance:

1. **Component name.** To avoid conflicts with simulators that have a limitation on the length of names accepted, the component name shall uniquely identify the component in the first 24 characters used (per Section 10.2.2.4 of the referenced DID). In fact, names might be longer than 24 characters, but the simulator will in such cases recognize only the first 24.
2. **Interface Declaration.** All input and output ports shall be listed as individual logic signal names (non-vector) and correlated with package pin numbers (in accordance with Section 10.2.2 of the referenced DID). This information may be in the form of port mapping statements (or port attributes for unique declarations). Both signal names and pin numbers can be accommodated in an external table per Reference 2.1.7. and interfaced with the model via a VHDL package. See Note 6.4. Linkage mode ports declarations shall not be used.
3. **Timing and Electrical Requirements.** Timing parameter names, unit and types shall be identified as generics (in accordance with section 10.2.2.2 of the DID), as well as applicable boundary conditions (e.g. setup and hold times or power supply voltage extremes). The actual timing values shall be in a separate data file per section 3.4.1 of this document. The names shall be those of the component manufacturer unless an illegal name has been assigned which would violate rules associated with certified (or validated) VHDL simulators or which would interfere with back annotation. Where more than one manufacturer produces exactly the same part, then the timing parameter names, units, values and types shall be those of one selected manufacturer, which shall be identified in the entity declaration along with the names of the other manufacturers who make that same part. Any exceptions should be flagged. The operating conditions corresponding to worst case times shall also be included, such as voltage level, temperature, load, etc.
4. **Operating Conditions.** Pertinent component data shall be recorded, such as electrical I/O specifications, maximum power dissipation, RAD effects, signal excursions allowable, logic voltage level definitions, temperature range, etc. (in accordance with

Section 10.2.2.3 of the referenced DID). VHDL package declarations should be used whenever characteristics are common across a class of similar components.

5. Revision Designator for error corrections in models. Hardware changes require a different model if behavior is altered. The cumulative revision history of the model itself, once released, and reasons for change shall be recorded. The revision history shall include changes that affect the model interface as well as changes that affect performance. While not a part of the Entity Declaration, changes to architectural bodies shall also incorporate version designators and revision histories. Such information shall be readable by the user.
6. Component manufacturer. The model shall be written for the primary manufacturer's product identified. If multiple sources exist, they shall be referenced.
7. Component description (including timing version or versions for certain temperature ranges, such as commercial versus military, and physical package type).
8. Data book, data sheet or military specification reference (unless or until the model replaces such paper references).
9. Names of all associated files, i.e. the model code file, the timing value file and test suite files.
10. Point of contact (name, address, telephone number). Name can be either for an individual or for an organization.
11. Dates of model design completion, final tests by the model builder and completion of validations by an independent body.
12. Type of model (e.g. behavioral (or procedural), structural, data flow full functional model).
13. Annotations. In accordance with Section 10.2.7 of the referenced DID other user information shall be shown where it is necessary to augment the formal VHDL text in order to make the intent of the model clear (including instantiation procedures, error message philosophy, assumptions followed in the writing of the model, qualifications, exceptions, etc.). Items that must be identified are: a. Discrepancies between the submitted description and applicable requirements. b. Any factors restricting the general use of the model description to represent the subject hardware. c. General approaches taken and decisions regarding modeling fidelity. d. Any information which the originating activity considers vital to subsequent users.

3.3.2 BEHAVIORAL BODY: The behavioral body (per section 10.2.3 of the referenced DID) is an abstract, high-level VHDL description of the functions performed by hardware. It shall be written in two parts as identified in 3.4.1 below. User accessible built-in test or maintenance functions that are incorporated in the hardware, or those that affect functionality whether accessible or not, shall also be encoded as part of the behavioral body.

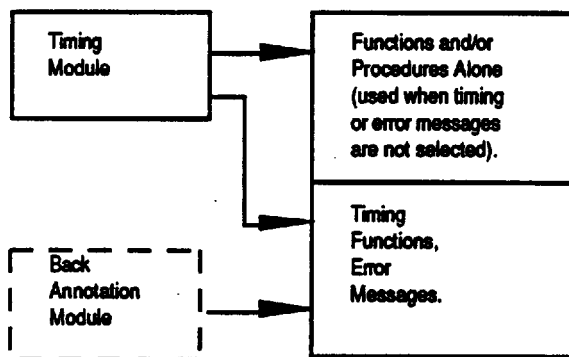
3.4 MODEL FEATURES: Models shall be written in such a way as to contain all of the following capabilities and characteristics and to avoid the pitfalls identified:

3.4.1 CONTROL OF TIMING: Timing data must be user-controlled, user-selectable and user-modifiable without losing original values which are under configuration management. Moreover, the models shall be written in such a way that minimum cost logic simulations can be performed without timing-related error messages. Therefore, VHDL models shall be capable of having throughput times applied when the model is simulated (in accordance with Section 10.2.3.2

of the referenced DID). Such times shall be inserted without reanalysis via an external timing module, as indicated in the figure below. The external timing module shall provide the capability to select nominal, minimum, maximum or generic times and to derate all times in accordance with system design requirements via the scaling factor. The scaling factor shall be the main mechanism by which the user can alter timing values, although it shall be possible for the user to override an existing value as warranted by his simulation requirements. Variable names (identified in the manufacturer's data book or selected in accordance with EIA JEDEC Council recommendations) shall be used in place of scalars in the model code itself. These variable names should have timing values assigned to them in the external timing module as shown in the manufacturer's data book. Also, by means of scaling factors, it should be possible for the user to derate any of the selected set of times prior to simulation runs. The default timing values shall be the minimum time unit (1 femtosecond).

In order to minimize the necessity to vary timing data in accordance with system characteristics (and to improve productivity), known voltage and temperature dependencies shall be incorporated in the timing section of the model where feasible. Such capabilities shall be identified in the Entity Declaration.

Throughput times, including unsymmetrical rise and fall times, are required in order to provide a good approximation of hardware performance. However, VHDL logic simulators are not timing analyzers, and analog-type timing information (i.e. voltage levels versus times) is specifically not required. Detection of "glitches" or race conditions may result from this level of timing definition, but such detections are not overriding objectives, especially for behavioral simulations. Timing accuracies shall be in accordance with the manufacturer's data book, but adjustments to timing values for voltage and temperature variations in the timing module will improve accuracy.



Behavioral Model. The model is conceptually divided into two sections. The first section represents the pure logic functions, and is to be used for simulations without timing or error messages. The second section adds throughput timing capability together with error messages which report input/output timing violations. The Timing Module is to be included with the model. Provisions are to be made for varying input port times (and if necessary output port times) for an external Back Annotation Module that is not included with the model.

3.4.2 LOGIC STATES: Pure behavioral models of commercial components can be written exclusively with logic states identified in the table below. The enumeration type in VHDL shall be used to declare logic states in a separate declaration called LOGIC_MV. States are defined in such a way as to convey a maximum amount of hardware design information while minimizing the amount of coding required.

A superset of logic states, strengths and levels has been identified in the combination of tables shown below and in the Appendix. Models shall be written such that all interfaces achieve interoperability by using the EIA BASICDEFS package provided with the Blank Detail Specification. If additional types are used for internal modeling, a package defining these types will be included with the model. To enhance portability, practices shown in the EIA VHDL Modeling Guidelines (under development) should be followed. The standard subset of logical states and strengths for each semiconductor process currently used to produce commercial components is identified in this section, in 3.4.3 below and in the Blank Detail Specification. A VHDL package shall map the actual states and strengths used to a given VHDL simulator. See Note 6.5.