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EIA STANDARD

TP-112

Contact Resistance and Current Rating of Parallel Circuits Test Procedure for Electrical Connectors, Contacts and Sockets

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January 2010



Electronic Components Industry Association

EIA-364-112

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(From Standards Proposal No. 5179 and reaffirmed by Standards Proposal No. 5361.07, formulated under the cognizance of the EIA CE-2.0 Committee on National Connector and Socket Standards).

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TEST PROCEDURE No. 112

CONTACT RESISTANCE AND CURRENT RATING OF PARALLEL CIRCUITS
TEST PROCEDURE FOR ELECTRICAL CONNECTORS AND SOCKETS

(From EIA Standards Proposal No. 5179, formulated under the cognizance of EIA CE-2.0 Committee on National Connector Standards)

1 Introduction

1.1 Scope

This procedure applies to connectors and sockets when multiple circuits are electrically connected in a parallel configuration and there is a need to determine the expected parallel resistance and or current rating.

1.2 Object

1.2.1 This standard establishes a procedure for determining the predicted parallel contact resistance of a connector or socket when multiple circuits are connected in parallel. A statistical approach is employed to determine the parallel or effective contact resistance using empirical data from EIA connector test sequences such as EIA-364-1000.

1.2.2 The procedure for determining current rating of a connector or socket when multiple circuits are connected in parallel will be added in the near future to this document.

1.3 Background

Traditional methods for determining low level contact resistance limits for parallel circuits such as a worst case parallel resistance calculation employ extremely conservative calculations that produce limits unlikely to be seen in actual application. This procedure outlines a more realistic method that is based on sound statistical principles and determines the parallel resistance limit with a percentile derived from calculations made using easily-obtained data. The limit calculated by this standard may be used by system designers to plan their voltage drop budget. Unrealistically high limits calculated with the previous method result in inefficient use of power resources in an application. Method A applies the Central Limit Theorem to parallel resistance distributions for low power level applications. Method B applies to current rating of parallel circuits using distribution fitting and Monte Carlo simulation.