



ANSI/EIA-469-E-2017
Approved: April 25, 2017

EIA-469-E

EIA STANDARD

Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolithic Capacitors

EIA-469-E
(Revision of EIA-469-D)

April 2017



Electronic Components Industry Association

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(From Standards Proposal No. 5217, formulated under the cognizance of the P-2.1 Committee on EIA National Ceramic and Dielectric Capacitors Standards).

Published by

©Electronic Components Industry Association 2017
EIA Standards & Technology Department
2214 Rock Hill Road, Suite 265
Herndon, VA 20170

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Foreword

This Standard was prepared under the cognizance of the P-2.1 Engineering Subcommittee on Ceramic Dielectric Capacitors of the Electronic Components Industry Association.

1 Scope

This document provides terminology, suggested methods, and criteria for characterizing the internal structural features of monolithic, ceramic dielectric capacitors. Its major objective is the accurate evaluation of the internal physical quality of the chip capacitor element as it relates to the functional reliability of the finished capacitor. This Standard also provides needed and useful information pertaining to activities associated with destructive physical analysis (DPA), such as visual inspection and DPA reporting. In addition, it provides tutorial help for problems inherent in DPA sample processing.

2 Purpose

This specification is primarily applicable to multilayer ceramic chip capacitors. It also contains criteria for radial and axially leaded multilayer ceramic capacitors but is not intended to define lead attachment criteria for other styles of leaded ceramic capacitors such as stacked, leaded capacitors with DIP (dual inline package) lead frames.

DPA is only one test contributing to the complete evaluation of a product lot regarding its fitness for use and its conformance to design and performance specifications. Information from other tests, such as initial electrical testing, voltage conditioning and other electrical and environmental testing that may be imposed, should be considered as well as DPA results. DPA should not be used in place of electrical testing for determining lot quality.

2.1 Representative DPA sampling

A DPA sample shall represent no more than one chip lot, since the probability of internal structural anomalies in chip elements often is associated with a chip lot because of some process variation or material variation, explained or unexplained, which may have affected only the lot in question.

The DPA sample shall be a group of parts that is randomly drawn from a lot that is ready for acceptance testing in accordance with the procurement document.

2.2 Sampling plan

A sampling plan purposely has been omitted from this Standard. The number of sample specimens to be subjected to DPA shall be the responsibility of the procurement agency and shall be specified in a document of that agency, in the purchase order, or in a contract with a supplier. If the purchase order does not specify a sampling plan when invoking this Standard, the plan given in Table XIV in 4.6.2 of MIL-PRF-123, *General Specification for High Reliability, Fixed, Ceramic Dielectric Capacitors (Temperature Stable and General Purpose)*, may be used, or the supplier may specify an appropriate sampling plan.

3 Ceramic capacitor DPA terminology

The terms and definitions included in this section are intended to aid in the complete understanding of this Standard and other DPA or procurement specifications. These are generally accepted and used throughout the ceramic capacitor industry.

Active area: The region within the chip element that consists of the overlapping portion of all of the opposed electrodes and the dielectric between them.

Artifact: Any anomaly, which is induced by DPA processes and which was not present in the sample specimen(s) prior to DPA processing. Examples are stress relief cracking, pull-out, surface fracturing, and dislodged leads that may occur during the decapsulation process.

Barrier layer: Generally, a layer of copper or nickel, which is deposited onto the primary end metallization to protect that layer during periods of exposure to molten solder.

Casting material: A plastic in liquid, unpolymerized form used for casting sample specimens for sectioning.

Chip-out: The physical, visual evidence remaining on the capacitor body, indicative of material loss from corners or edges (ceramic, encapsulation, or ceramic plus metallization) due to mechanical damage, lack of material integrity, or both. Generally, a chip-out has sharp corners and may be associated with a crack or cracks.

Cold solder: A condition of a solder joint characterized by a dull, grainy, and excessively porous surface with indications of incomplete reflow or poor lead or chip wetting. Internally, cold solder is excessively porous and may entrap small pockets of flux.

Common electrodes: All of the electrodes in a chip element designed to contact a single end termination.

Cover plate: The outer ceramic envelope on the top and bottom of the capacitor. See **Figure A.2**.

Crack: A fissure or break without a separation of the material. Cracks may be seen in the ceramic material, encapsulation material, or in the solder joint. A crack may be the result of inadequate manufacturing processes or materials or it may be an induced artifact of DPA processing or environmental stresses.

Delamination: A separation between two layers of ceramic or at a ceramic-to-electrode interface, or rarely, a separation within a single layer of ceramic which is roughly parallel to the electrode plane. A delamination differs from a void in that there is no material missing, only a separation of layers.

Dielectric: The ceramic between electrically opposed electrodes.

Dielectric thickness: The distance between opposed electrodes measured on a line perpendicular to the electrode plane.

NOTE—Assessment of this dimension should be based upon a technique which measures several thickness samples (5 to 10) and averages the value for one layer, accounting for electrode thickness.

Encapsulant: The body insulation material used to physically and electrically protect the capacitor element.

Encapsulation: The physically configured encapsulant that forms the capacitor case.

End margin: The portion of the ceramic envelope, extending from the outer edge of the chip element to the opposed electrodes, through which the common electrodes pass to the termination. See **Figure A.2**.

End margin delamination: Specifically, a delamination in an interface of a terminating electrode and one or both of the adjacent ceramic layers, but in general the term used for indicating any delamination which occurs in an end margin, including a knitline delamination.

End metallization: The system of metallization used to cover both ends of the capacitor. It may be the only metallization or found under a barrier and solderable layer.

Inspection lot: A group of capacitors or other devices offered for acceptance testing at one time, generally associated with a military specification; it may include many production lots, depending on the control document.

Interface: The junction of two layers in a layered device; for example, the junction of electrode to dielectric layers or between two ceramic sheet layers.

Intermetallic: A solution of two metallic elements formed during reflow or due to certain other conditions involving temperature and time; for example, the copper/tin intermetallic formed between a copper surface and a tin/lead solder when the solder is reflowed against the copper surface.

Knitline: Generally, the bonding interface between two layers of bondable materials; these may be the same, similar, or different materials. Specifically, in ceramic multilayer capacitors, the interface of bonding between two ceramic sheets or a ceramic sheet and metal electrode layer.

Margin: The ceramic portion of a chip element which envelopes the active area.

Microcrack: A very fine narrow crack in the ceramic that is visible only at relatively high magnifications (generally above 150X) with the aid of indirect or dark field or polarized lighting. See **Annex D, Figure D.2**.

Mounting: The process, during DPA, consisting of setting the sample specimens up on an adhesive surface and surrounding them with a retainer ring, ready for pouring of the mounting resin.

Overlap view: The longitudinal sectional view of the capacitor, showing the overlapped electrode edges, end margins, end metallizations, and chip to lead solder joint (if applicable). This is commonly called the side view. See **Figure A.2**.

Pinhole: By definition, an open cavity in the ceramic cover plate, generally circular in shape and usually having appreciable depth.

Production lot: A quantity of capacitors of the same design, having a common raw material origin and formulation, which was processed through the chip manufacturing sequence as a single group.

NOTE —More than one production lot may come from one chip lot, and procurement specifications for capacitors may require traceability all the way back to raw material lots.

Pull-out: The undesirable shattering, crumbling, and removal of materials from the specimen surface during abrasive sectioning or polishing. This is a problem particularly around voids, delaminations or other unsupported edges.

Side margin: The portion of the ceramic which extends from the side of the electrodes to the outside edge of the chip element. See **Figure A.2**.

Side margin view: The sectional view of a sample unit, showing the side margins, cover plates and electrode edges. See **Figure A.2**.

Solder fill: The bulk of solder metal which occupies the space between a capacitor lead wire and the capacitor element, which constitutes the solder joint between lead and capacitor element.

Solder fillet: The externally visible portion of the solder metal which attaches the lead wire to the capacitor element and is characterized by a smooth and tapering convergence of solder metal with lead wire and capacitor element, the surface of the solder often being somewhat concave.

Solder wetting: The coating of a surface to be soldered with a smooth adherent film of molten solder.

Stress relief cracking: Cracks generally seen in the overlap view, but also in the side margin view, associated usually with the cover plates and the outer two or three electrodes. These are artifacts of the sectioning process due to grinding samples without decapsulation before mounting or due to inadequate edge support. They are not defects and must not be assessed as such.

Surface fracturing: Shallow, oblique cracking of ceramic between electrodes and in cover plates due to grinding stresses or chatter of the potted sample on the moving surface of the abrasive grit where the sample may alternately grab and slide. This artifact may be induced also during hand polishing operations.

Surface relief: The difference in the level or height of the ground or polished specimens between the relatively hard and softer materials. The metal portions erode faster during grinding and polishing than do the harder ceramic surfaces. Hand polishing produces considerable surface relief.

Void: An absence of material, typically in the dielectric layer. A void differs from a delamination in that material is missing and therefore there is a cavity in the dielectric layer or other material.

4 Recommended procedures and methods

It is important that the DPA process be repeatable and reproducible. The guidelines given here provide minimal but crucial information necessary to achieve that outcome. However, it is the responsibility of the laboratory performing the DPA to develop test methods that ensure the repeatable and reproducible results. As the part size and dielectric thickness decrease, marginal procedures in sample preparation can falsely enlarge the true size of internal defects. Use of automated grinding and polishing equipment, although not required by this specification, is recommended due to the more consistent results obtained when using automation.

There are several steps involved in the DPA process; cleaning (and decapsulation if necessary), mounting parts in a block of cold mounting resin, then grinding and polishing the mounted specimen.

4.1 Visual appearance of DPA sample units

Since the primary purpose of DPA is determination of internal physical quality, capacitors with rejectable visual defects should not be used for DPA. However, sometimes it is expedient to use visual rejects for DPA. If visual rejects are included in the DPA, then appropriate records of the type and number of external defects must be kept to avoid confusing the internal examination performed during DPA.

4.2 Cleaning prior to mounting

In order to ensure good adhesion of the mounting resin to the capacitor, it is necessary to clean and dry the capacitors prior to mounting. Isopropyl alcohol is a good cleaning solvent. Place cleaned capacitors on an absorbent tissue and allow to air dry until all residual moisture is evaporated.

4.3 Mounting and casting

Parts should be fixtured on a double-sided adhesive surface inside a mold ring. See **Figure C.3**. Mold rings may be disposable or reusable. If they are reusable, a fixture that applies an even force across the resin block should be used for removing the block from the mold ring to ensure no induced failures in the capacitor samples during removal.

One half of the capacitors should be fixtured so that grinding and polishing will reveal the side view and the other half the end view. If there are an uneven number of capacitors, the larger quantity should be fixtured to reveal the side view. See **Figure A.2**.

The capacitors shall be mounted so that there is adequate space between parts and adequate space between the edges of the parts and the mold ring. Adequate space means that sufficient space is allowed so that mounting resin can flow between the parts and also flow between the parts and the mold ring. The capacitors should also be mounted so that they are flat within 5 degrees of the sectional plane. Mold rings should be as small as is practical. Generally, 1.25 inch mold rings are large enough for all but the largest capacitors.

A suitable cold mounting resin should be mixed according to the manufacturer's recommendation and poured into the mold. The cold mounting resin should cure at room temperature and have an exotherm of less than 65°C. The resin should have low shrinkage and after curing should still support the edges of the capacitor. Finally, the resin should be sufficiently hard to resist edge relief during polishing.

It is advisable to remove any trapped air prior to curing the resin.

4.4 Grinding and polishing

Grinding is used to cut into the mounted parts and expose the region of interest. Successively finer grades of silicon carbide paper are used with a continuous stream of water for cooling and cleaning the wheel. Mounts should be cleaned with a mild detergent, or similar solution at each change of silicon carbide paper.

It is suggested that automated grinding and polishing equipment be used for sectioning. Automated equipment applies a constant, known pressure during grinding and polishing. This minimizes the introduction of defects during the grinding and polishing steps. See **Clause 5**.

Due to the high probability of introducing cracks into the capacitor, cutting or sawing of the parts is not permitted. For the same reason, it is suggested that silicon carbide paper coarser than 320 (P400) grit not be used.

Polishing should be accomplished in several steps. Steps should be kept to a minimum in order to avoid corner rounding of the capacitors which could conceal defects. The first step is a rough polish and the second step is a very fine grit polish. The preferred polishing media are diamond compounds, although alumina powder may be used, where aluminum contamination is not an issue. Alumina powder, when used incorrectly, is known for causing corner rounding.

5 Sample preparation problems

The process of mounting, grinding and polishing parts remains more of an art than a science. Poor preparation techniques can induce problems that are not present in the sample prior to mounting and sectioning. These anomalies are called artifacts. As ceramic capacitors can break under relatively low mechanical force or due to thermal stresses, it is important to follow established procedures and to automate the process if possible. As the part size and dielectric thickness decrease, marginal procedures in sample preparation can falsely enlarge the true size of internal defects.

Problems induced by poor sample preparation may include the following:

Excessive pull-out: Pull-out increases the size of voids or delaminations in the capacitor. It occurs during the grinding step if excessively coarse silicon carbide paper and/or high contact pressure is used. It may also occur during grinding or polishing when using finer grit papers or abrasives if the mount is grabbing and then releasing against the silicon carbide paper or polishing abrasive.

Because of the possibility of pull-out, the best method for determining the microstructure of ceramic capacitors is not DPA. Fracturing the capacitor with angle cutters and examining the fractured surface using a microscope with a large depth of field, such as a scanning electron microscope, yields a much truer picture of the ceramic microstructure.

Inclined component mounting: Samples that are mounted at an incline to the desired sectional plane may show wide wavy appearing electrodes. These samples should not be used for analysis.

Cover plate cracking: Cracks in the cover plate frequently occur as a result of unsupported cover layers due to improper sample cleaning or improperly cured mounting resin. Mounting resin is usually a two-part system. The quantity of each part and the mixing technique used are very important. Cover plate cracking can also occur due to excessive pressure during grinding and polishing.

Grinding scratches: If the silicon carbide grit used for grinding is not chosen properly or samples and paper surface are contaminated by larger grit, scratches may remain even after the polishing step. The scratches can also cause pull-outs. Both the scratches and the pull-outs may be misinterpreted as defects.

Corner Rounding: Excessive pressure or excessive time during polishing can cause the sample edges and corners to round. Rounding makes accurately measuring terminations, barrier layers and solderable surfaces impossible. It also may hide cracks radiating back from the terminations.