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EIA-540B0AE

EIA SPECIFICATION

Detail Specification for Production Land Grid Array (LGA) Socket for Use in Electronic Equipment

EIA-540B0AE

JUNE 2000



Electronic Components, Assemblies & Materials Association

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This Specification does not purport to address all safety problems associated with its use or all applicable regulatory requirements. It is the responsibility of the user of this Specification to establish appropriate safety and health practices and to determine the applicability of regulatory limitations before its use.

(From Standards Proposal No. 3935-A, formulated under the cognizance of the CE-3.0 Committee on Sockets.)

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Systems Standard Organization ELECTRONIC INDUSTRIES ALLIANCE	DETAIL SPECIFICATION NUMBER EIA-540B0AE
GENERIC SPECIFICATION NUMBER EIA-5400000-A	SECTIONAL SPECIFICATION NUMBER EIA-540B000
	BLANK DETAIL SPECIFICATION NUMBER None
Socket Outline Drawing See figures 1 and 2 for dimensional information. Tolerances: ± 0.13 mm (± 0.005 in) on all figures except where noted.	Product Description This specification is for use with LGA devices described by JEDEC.
	Product Requirements The complete requirements for the interconnect system shall consist of this Detail Specification and where applicable the latest issue of EIA-540B000.
	TYPICAL CONSTRUCTION Contact Material : Copper alloy Outermost Contact Finish: Gold Termination Finish : Tin-lead Insulator Material : High temperature thermoplastic
	APPLICATION/ASSESSMENT LEVEL For use in commercial, computer, and communications equipment.

1 Scope and purpose

This specification covers interconnect systems typically used for production land grid array (LGA) devices.

1.2 Purpose

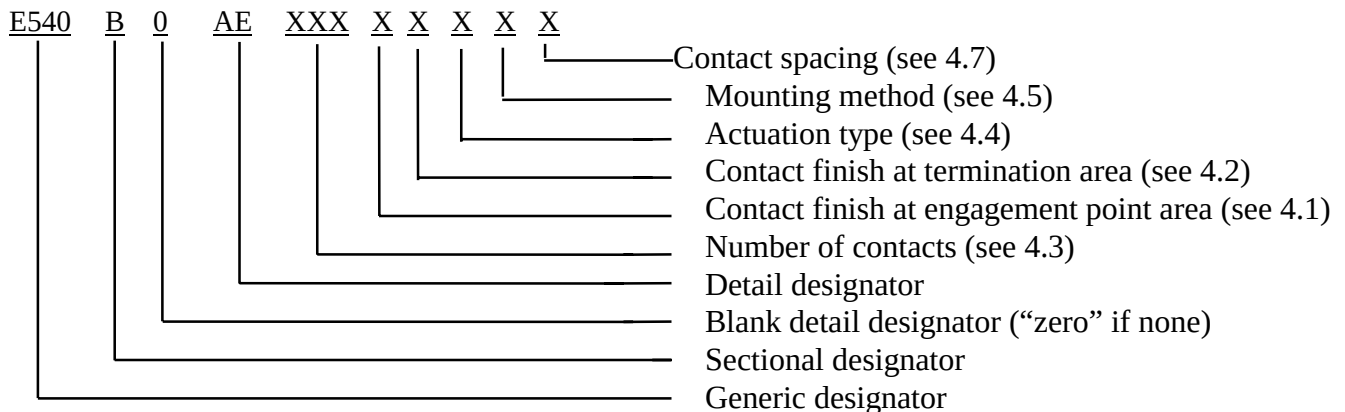
The purpose of this detail specification is to provide all information required for the identification and assessment of the LGA socket described herein. The information, contained herein or by reference, is complete and sufficient for inspection purposes.

2 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

- a) EIA-364-C, Electrical Connector Test Procedures Including Environmental Classifications (December, 1994).
- b) EIA-5400000-A , Generic Specification (August, 1996).
- c) EIA-540B000, Sectional Specification (November, 1997).

3 EIA part number (example)



4 Socket details

4.1 Contact plating

The outermost plating of the contact area shall be gold or tin-lead and shall satisfy the requirements specified in the qualification test sequence. The contact plating systems utilized shall be compatible to the systems they are mated to, such as:

- a) Gold (designation “A”)
- b) Tin-lead (designation “B”)

NOTE: Gold-plated contact surfaces mated to tin-lead plated contact surfaces are not an acceptable plating combination.

4.2 Contact finish at termination area

Contact finish at the termination area shall be designated by a letter indicated in Table 1.

Table 1 Contact finish at termination area

Identification number	Contact finish
P	Gold
Z	Other

4.3 Number of contacts and footprint pattern

Three characters shall designate the number of terminals of the socket and the footprint pattern. The first two characters shall be numerical designating the grid size of the socket. For example “16” designates a 16 x 16 grid, “25” designates a 25 x 25 grid, etc. The third character shall be the numeral “0” if the socket contains the maximum number of contacts obtainable, or a letter (A through Z) for a partially filled array. Annex F delineates the three character designations for all known arrays. See figure 2 for the recommended LGA board pattern.

NOTE- If all letters of the alphabet have been used for the third character of a particular grid size, then the first character shall be replaced with the numeral “9”, allowing another complete use of the alphabet as the third character. For example “90R” would depict a specific 10 x 10 array, whereas “91R” would depict a specific 11 x 11 array. If additional designations are needed, the process shall continue by utilizing an “8”, “7”, etc. as the first character.

4.4 Actuation method

The actuation of the socket shall be designated by one number indicated in table 2.

Table 2 Actuation type

Identification Number	Actuation method
1	ZIF with Lever Actuation
2	ZIF with Slot Actuation
3	Other

4.5 Mounting Method

The mounting of the socket shall be designated by one letter indicated in table 3.

Table 3 Mounting method

Identification letter	Mounting method
A	Surface Mount
B	Through Hole
C	Other

4.6 Socket dimensions

The configuration of the LGA socket is optional within the limits of the dimensions within figure 1 and the mounting dimensions within figure 2.

4.7 Contact spacing

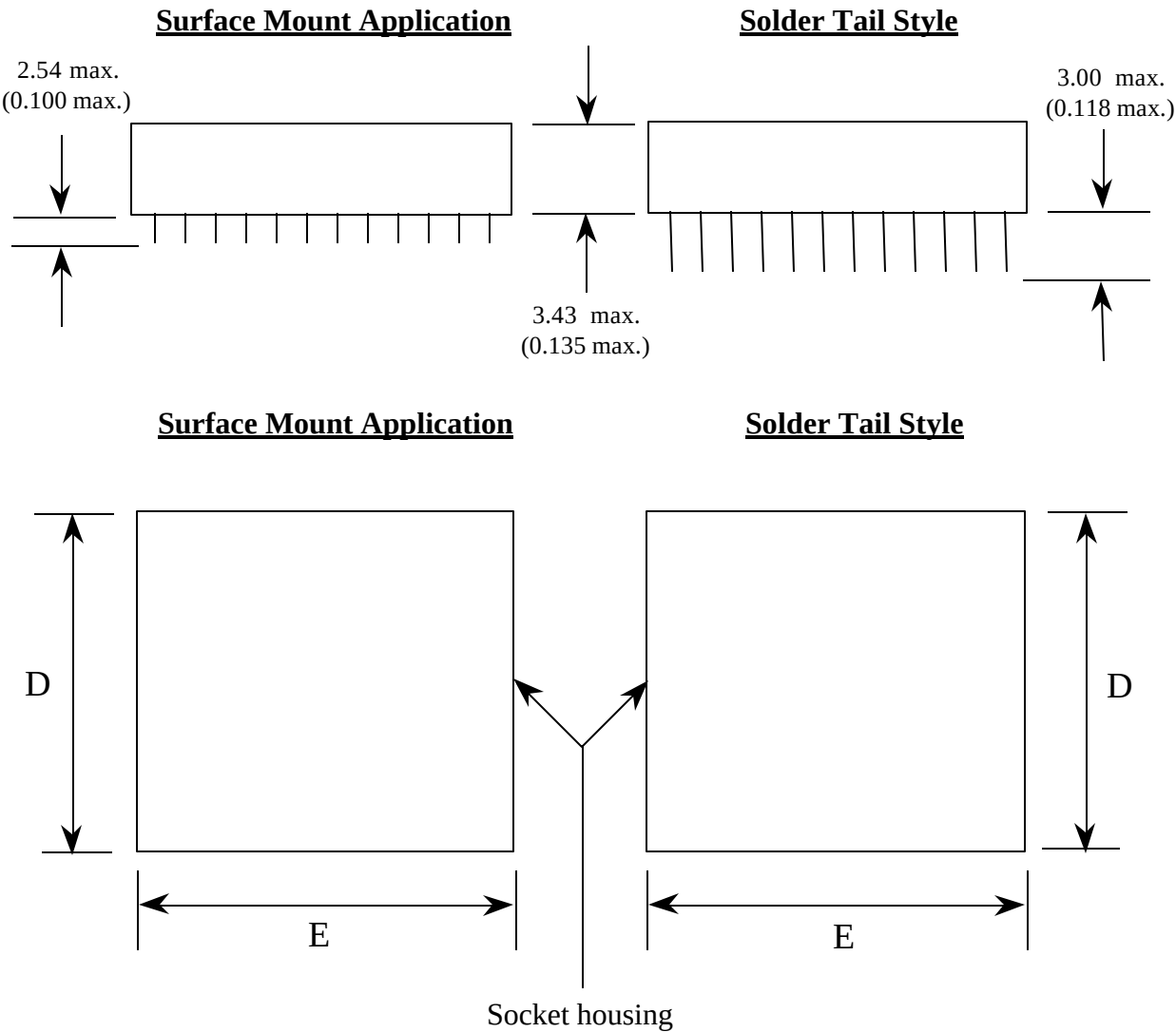
The contact spacing shall be designated by one letter indicated in table 4.

Table 4 Contact spacing

Identification letter	Contact spacing
A	1.27 (0.050)
B	1.00 (0.039)
C	0.80 (0.030)
D	0.50 (0.020)
E	Other

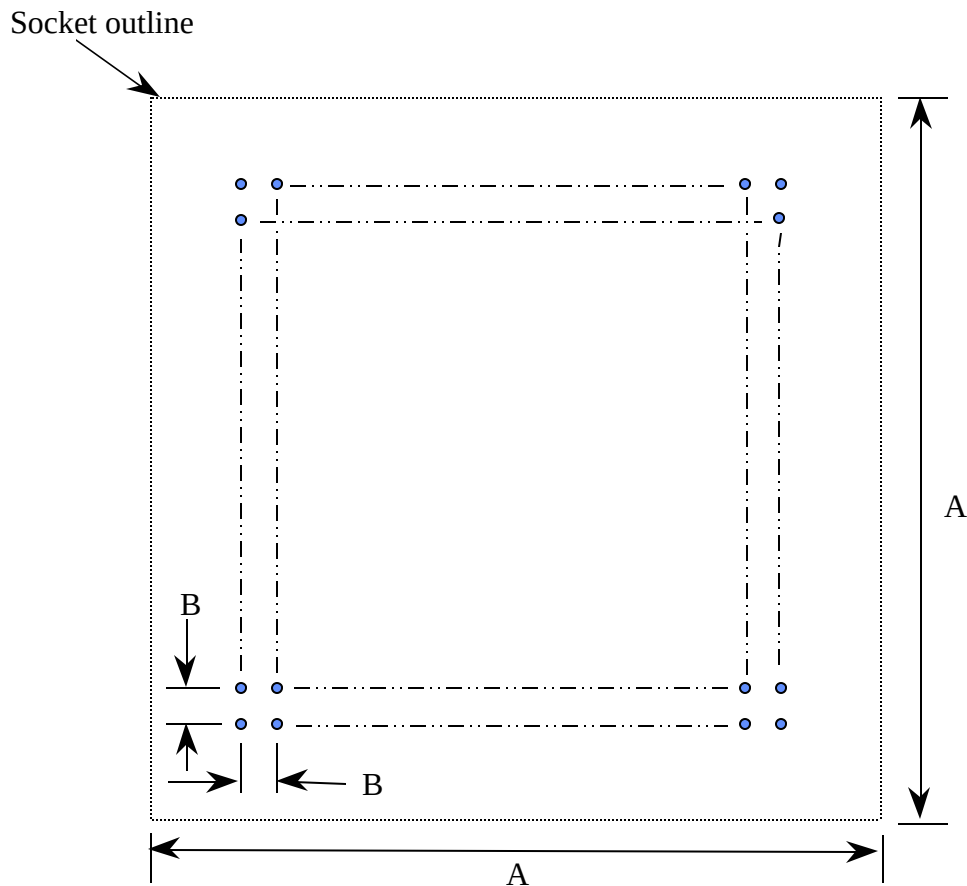
5 Mating devices

Mating devices shall be in accordance with JEDEC specifications. Said devices shall be internally wired in order to perform the appropriate electrical measurements such as low-level circuit resistance (LLCR).



Socket housing	D (minimum)	E (minimum)
16 x 16	30.40 (1.197)	30.40 (1.197)
25 x 25	40.64 (1.600)	40.64 (1.600)
33 x 33	50.80 (2.000)	50.80 (2.000)

Figure 1 Housing dimensions



A	B
30.40	See table 4 for spacing
40.64	See table 4 for spacing
50.80	See table 4 for spacing

Notes (Surface mount application):

- a) SMT pad size : 0.86 mm +/- 0.05 mm diameter
(0.034 in +/- 0.002 in diameter)
- b) SMT pad plating : Tin-Lead

Notes (Plated through hole application):

- a) Finished PTH size : 0.86 mm +/- 0.05 mm diameter
(0.034 in +/- 0.002 in diameter)
- b) PTH plating : Tin-Lead

Figure 2 - Recommended board pattern



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6 Atmospheric conditions for testing

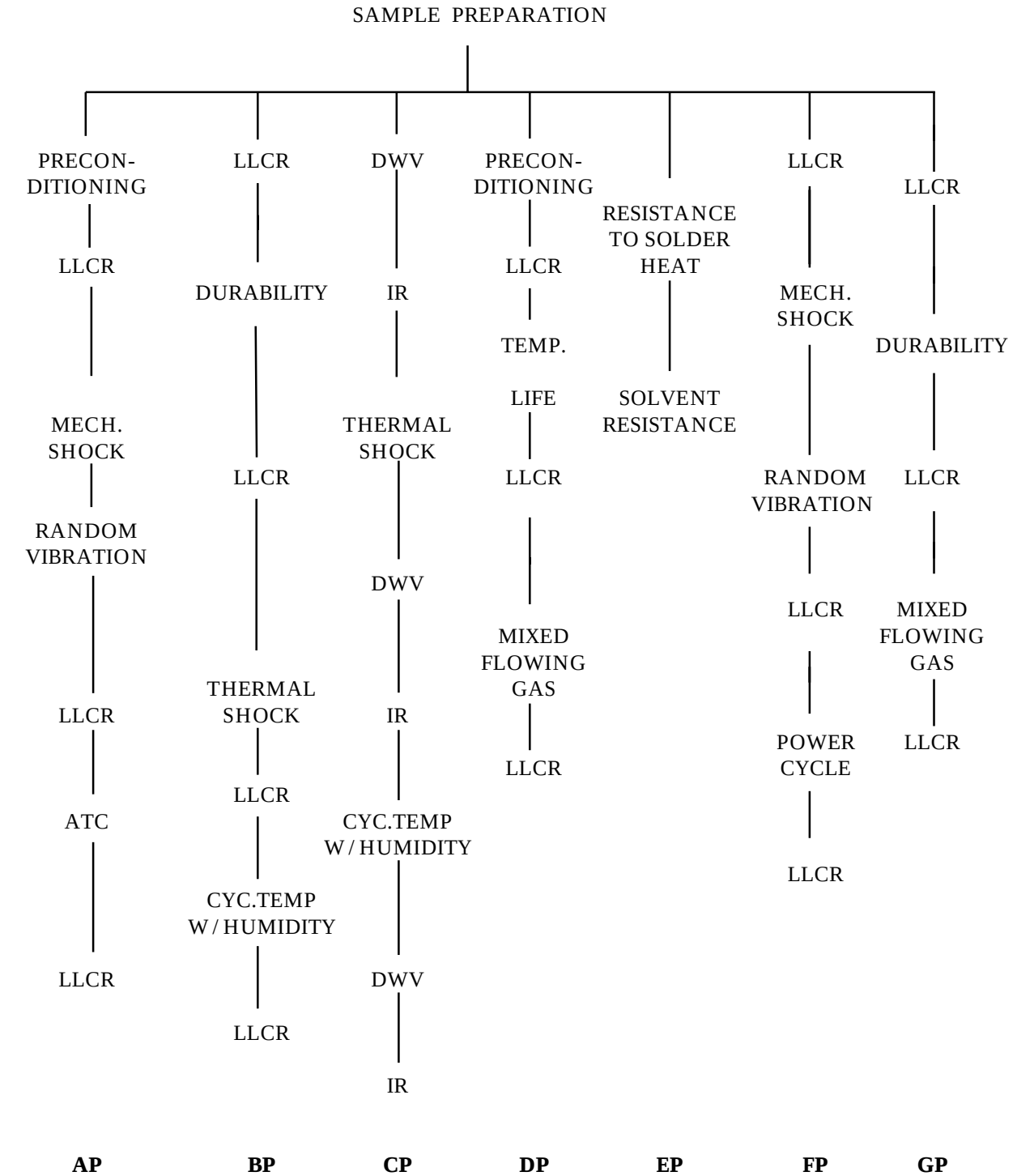
The interconnect system shall be tested at the atmospheric conditions as specified in table 5, general controlled.

Table 5 Atmospheric conditions for testing

Atmospheric conditions	Temperature	Air pressure	Relative humidity
General controlled	15 °C to 35 °C (59 °F to 95 °F)	87 kPa to 107 kPa (650 mmHg to 800 mmHg)	80% or less

7 Test sequence

This test sequence shows all tests and the order in which they shall be carried out as well as the requirements to be met. The baseline test sequence (figure 3) illustrates the order of tests by group. In the following test sequence tables, where an EIA test is specified without a letter suffix, the latest approved version of that test shall be used.



LLCR : Low level circuit resistance
 ATC : Accelerated thermal cycling
 DWV : Dielectric withstanding voltage
 IR : Insulation resistance

Figure 3 - Baseline test sequence