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Specification for QSFP+ 10 Gb/s Pluggable Transceiver

EIA-964

(Was SFF-8436, Rev 4.8, dated October 31, 2013)

December 2016



Electronic Components Industry Association

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CONTENTS

Clause		Page
Foreword		vii
Background		viii
1	Introduction	1
1.1	Scope	1
1.2	Description of clauses	1
2	Applicable documents	2
2.1	Industry documents	2
2.2	SFF Specifications	2
2.3	Sources	2
2.4	Conventions	3
3	Content	3
4	Electrical specification	7
4.1	Electrical connector	7
4.1.1	Low speed electrical hardware pins	12
4.1.1.1	ModSell	12
4.1.1.2	ResetL	12
4.1.1.3	LPMODE	12
4.1.1.4	ModPrsL	13
4.1.1.5	IntL	14
4.1.2	Low speed electrical specification	14
4.1.3	High speed electrical specification	15
4.1.3.1	Rx(n)(p/n)	15
4.1.3.2	Tx(n)(p/n)	15
4.2	Power requirements	16
4.2.1	Host board power supply filtering	17
4.3	ESD	19
5	Mechanical and board definition	19
5.1	Introduction	19
5.2	QSFP+ datums and component alignment	20
5.3	QSFP+ module mechanical package dimensions	22
5.3.1	Mating of QSFP+ module PCB to QSFP+ electrical connector	25

CONTENTS (continued)

Clause		Page
5.4	Host PCB layout	26
5.4.1	Insertion, extraction and retention forces for QSFP+ modules	27
5.5	Color coding and labeling of QSFP+ modules	28
5.6	Bezel for systems using QSFP+ modules	29
5.6.1	Bezel for the thru bezel cage assembly version	29
5.6.2	Bezel for the behind the bezel cage assembly version	31
5.7	QSFP+ electrical connector mechanical	32
5.8	Individual QSFP+ cage assembly versions	34
5.8.1	QSFP+ heat sink clip dimensions	36
5.8.2	QSFP+ heat sink dimensions	37
5.8.3	Light pipes	38
5.9	Dust / EMI cover	38
5.10	Optical interface	39
6	Environmental and thermal	41
6.1	Thermal requirements	41
7	Management interface	41
7.1	Introduction	41
7.2	Timing specification	41
7.2.1	Introduction	41
7.2.2	Management interface timing specification	42
7.2.3	Serial interface protocol	43
7.2.3.1	Management timing parameters	43
7.3	Memory interaction specifications	44
7.3.1	Timing for soft control and status functions	45
7.4	Device addressing and operation	47
7.5	Read/write functionality	49
7.5.1	QSFP+ memory address counter (Read AND Write operations)	49
7.5.2	Read operations	50
7.5.2.1	Current address read	50
7.5.2.2	Random read	51
7.5.2.3	Sequential read	52
7.5.2.4	Sequential read from random start address	53
7.5.3	Write operations	54
7.5.3.1	BYTE write	54
7.5.3.2	Sequential write	55
7.5.3.3	Acknowledge polling	56

CONTENTS (continued)

Clause	Page
7.6 QSFP+ memory map	56
7.6.1 Lower memory map	58
7.6.1.1 Status indicator bits	59
7.6.1.2 Interrupt flags	60
7.6.1.3 Module monitors	65
7.6.1.4 Channel monitoring	67
7.6.1.5 Control bytes	69
7.6.1.6 Module and channel masks	71
7.6.1.7 Rate select (Byte 87-88)	73
7.6.1.8 Password entry and change	74
7.6.2 Upper memory map Page 00h	75
7.6.2.1 Identifier (Address 128)	78
7.6.2.2 Extended Identifier (Address 129)	79
7.6.2.3 Connector (Address 130)	80
7.6.2.4 Specification compliance (Address 131-138)	80
7.6.2.5 Encoding (Address 139)	82
7.6.2.6 BR, nominal (Address 140)	82
7.6.2.7 Extended RateSelect compliance (Address 141)	83
7.6.2.8 Length (Standard SM Fiber)-km (Address 142)	83
7.6.2.9 Length (OM3) (Address 143)	83
7.6.2.10 Length (OM2) (Address 144)	83
7.6.2.11 Length (OM1) (Address 145)	84
7.6.2.12 Cable assembly length (copper or active cable) (Address 146)	84
7.6.2.13 Device tech (Address 147)	84
7.6.2.14 Vendor name (Address 148-163)	85
7.6.2.15 Extended module codes (Address 164)	85
7.6.2.16 Vendor OUI (Address 165-167)	86
7.6.2.17 Vendor PN (Address 168-183)	86
7.6.2.18 Vendor Rev (Address 184-185)	86
7.6.2.19 Wavelength (Address 186-187)	86
7.6.2.20 Wavelength tolerance (Address 188-189)	87
7.6.2.21 Max case temp (Address 190)	87
7.6.2.22 CC_BASE (Address 191)	87
7.6.2.23 Options (Address 192-195)	87
7.6.2.24 Vendor SN (Address 196-211)	89
7.6.2.25 Date Code (Address 212-219)	89
7.6.2.26 Diagnostic monitoring type (Address 220)	90
7.6.2.27 Enhanced options (Address 221)	91
7.6.2.28 CC_EXT (Address 223)	91
7.6.2.29 Vendor specific (Address 224-255)	91

CONTENTS (continued)

Clause	Page
7.6.3 Upper memory map (Page 01h)	92
7.6.4 User writable and vendor specific memory	92
7.6.5 Upper memory (Page 03h)	93
7.6.5.1 Module and channel thresholds	93
7.6.5.2 Optional channel controls	95
7.6.5.3 Channel monitor masks	96

Figure	Page
1 Application reference model	6
2 QSFP+ module pad layout	7
3a Example QSFP+ host board schematic for optical modules	10
3b Example QSFP+ host board schematic for passive copper cables	11
4 Recommended host board power supply filtering	17
5 Instantaneous and sustained peak currents for Vcc1, Vcc Tx or Vcc Rx	18
6 QSFP+ pluggable and direct attach module rendering	20
7 QSFP+ datum alignment, depth	22
8 Drawing of QSFP+ module	23
9 QSFP+ module tab drawings	24
10 Pattern layout for QSFP+ printed circuit board	25
11 QSFP+ host PCB mechanical layout	26
12 QSFP+ host PCB mechanical layout, detail Z	27
13a Recommended bezel design for cages that extend into or thru bezel	30
13b Recommended bezel design for cages that extend up against the inside surface of the bezel	31
14 QSFP+ module electrical connector illustration	32
15 QSFP+ electrical connector specification	33
16 Thru bezel (left side) and behind the bezel (right side) cage and optional heat sink designs (exploded view)	34
17 1-by-1 thru bezel cage design	35
18 QSFP+ heat sink clip	36
19 QSFP+ heat sink	37
20 Dust / EMI cover	38
21a QSFP+ Optical receptacle and channel orientation for MPO connector	39
21b QSFP+ Optical receptacle and channel orientation for dual LC connector	39
21c QSFP+ MPO optical patchcord	40
21d QSFP+ dual LC optical patchcord	40
22 QSFP+ timing diagram	42
23 QSFP+ device address	49

CONTENTS (continued)

Figure		Page
24	QSFP+ current address read operation	50
25	QSFP+ random read	51
26	Sequential address read starting at QSFP+ current address	52
27	Sequential address read starting with random QSFP+ read	53
28	QSFP+ write byte operation	54
29	QSFP+ sequential write operation	55
30	QSFP+ memory map	57

Table		Page
1	Multimode fiber applications	5
2	Single mode fiber applications	5
3	Pin function definition (see Figure 10 for pad dimensions)	8
4	Power mode truth table	13
5	Low speed control and sense signals	14
6	Power supply specification	18
7	Power budget classification	19
8	Definition of datums	21
9	Insertion, extraction and retention forces	28
10	Temperature range class of operation	41
11	Management interface timing parameters	43
12	QSFP+ memory specification	44
13	Single byte writable memory block	44
14	Multiple byte writable memory block	44
15	Timing for QSFP+ soft control and status functions	45
16	I/O Timing for squelch & disable	47
17	Lower memory map (A0h)	58
18	Status indicators (Page A0)	59
19	Channel status interrupt flags (Page A0)	61
20	Module monitor interrupt flags (Page A0)	62
21	Channel monitor interrupt flags (Page A0)	63
22	Module monitoring values (Page A0)	66
23	Channel monitoring values (Page A0)	68
24	Control bytes (Page A0)	69
25	IntL masking bits for module and channel status interrupts (Page A0)	71
26	Functionality of byte 87 and 88: xN rate select with extended rate selection (Page A0)	73
27	Definition of application select (Bytes 89 to 92 and Bytes 94 to 97) (Page A0)	74

CONTENTS (continued)

Table	Page
28 Detailed description of control mode (Page A0)	74
29 Serial ID data fields (Page 00)	75
30 Identifier values (Address 128) (Page 00)	78
31 Extended identifier values (Address 129) (Page 00)	79
32 Connector values (Address 130) (Page 00)	80
33 Specification compliance (Address 131-138) (Page 00)	80
34 Encoding values (Address 139) (Page 00)	82
35 Extended RateSelect compliance tag assignment (Address 141) (Page 00)	83
36 Description of device technology (Address 147) (Page 00)	84
37 Transmitter technology (Address 147 bits 7-4) (Page 00)	85
38 Extended module code values (Address 164) (Page 00)	85
39 Option values (Address 192-195) (Page 00)	88
40 Date codes (Address 212-219) (Page 00)	89
41 Diagnostic monitoring type (Address 220) (Page 00)	90
42 Enhanced options (byte 221) (Page 00)	91
43 Application select table (Page 01)	92
44 Application code structure	92
45 Upper memory map (Page 03h)	93
46 Module and channel thresholds (Page 03)	94
47 Vendor specific and optional channel controls (Page 03)	95
48 Output amplitude control (address 238-239) (Page 03)	96
49 Channel monitor masks (Page 03)	96

Foreword

(This foreword is informative only and is not part of this specification.)

This Specification is from EIA Standards Proposal No. 5331, formulated under the cognizance of EIA CE-2.0, Committee on Connector and Socket Standards. This project was conducted in liaison with the SFF Committee as representing the disk drive industry. Utilization of this Standard is intended to eliminate misunderstandings or confusion between a manufacturer and user with respect to product performance and testing requirements for this as well as other possible applications.

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

Background

Abstract: This specification defines the electrical (copper), the optical and the mechanical characteristics of the pluggable Quad SFP+ Module/direct attach cable plug and connector.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of drives.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Specification for QSFP+ 10 Gb/s Pluggable Transceiver

(From EIA Standards Proposal No. 5331, formulated under the cognizance of the EIA CE-2.0 Committee on National Connector and Socket Standards, and previously published by the SFF Committee as SFF-8436.)

1. Introduction

1.1 Scope

In an effort to broaden the applications for storage devices, an ad hoc industry group of companies representing system integrators, peripheral suppliers, and component suppliers decided to address the issues involved.

1.2 Description of clauses

Clause 1 contains the Scope and Purpose

Clause 2 contains Referenced and Related Standards and SFF Specifications

Clause 3 begins the specification

Clause 4 contains electrical specifications

Clause 5 contains mechanical specifications and printed circuit board recommendations

Clause 6 contains environmental and thermal considerations

Clause 7 is a description of the management interface and management register contents.

2 Applicable documents

The following documents form a part of this specification to the extent indicated herein. In the event of conflict between this specification and the referenced documents, this specification shall take precedence.

2.1 Industry documents

The following interface standards and specifications are relevant to this Specification.

- GR-253-CORE
- IEEE Std 802.3
- IEEE Std 802.3ba
- InfiniBand Architecture Specifications
- INCITS 404 FC-PI-2 (Fibre Channel Physical Interface -2)
- INCITS 460 FC-PI-3 (Fibre Channel Physical Interface -3)
- INCITS 450 FC-PI-4 Fibre Channel Physical Interface -4)
- INCITS 457 SAS - 2 (Serial Attached SCSI - 2)
- INCITS 478 SAS - 2.1 (Serial Attached SCSI - 2.1)
- INF - 8438 QSFP 4X 4 Gb/s Transceiver (Quad SFP)
- SFF - 8636 Management Interface for Cabled Environments
- SFF - 8431 has been superseded by:
- SFF - 8418 SFP+ 10 Gb/s Electrical Interface
- SFF - 8419 SFP+ Power and Low Speed Interface
- SFF - 8472 Management Interface for SFP+

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at <ftp://ftp.seagate.com/sff/SFF-8000.TXT>

2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (<http://www.sffcommittee.com/ie/join.html>).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards

Copies of SFF, ASC T10 (SCSI), T11 (Fibre Channel) and T13 (ATA/SATA) standards and standards still in development are available on the HPE version of CD_Access

2.4 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,426.9	1 323 426,9	1 323 462.9

3 Content

3.1 This Specification covers the following items:

- a) electrical interfaces (including pinouts for data control, status, configuration and test signals) and the electrical connector and recommended host PCB layout requirements.
- b) management interfaces encompassing features from the current SFP MSA and includes specific multi-data rate and multi-protocol implementations.
- c) optical interfaces (including the optical connector receptacle and mating fiber optic connector plug and recommended breakout cable assembly.) The optical specifications are left to the applicable standards for each protocol.
- d) mechanical including package outline with latching detail and optical connector receptacle detail, electrical connector mechanical details for both the module and host PCB halves, front panel cut-out recommended dimensions and a blocking key solution to prevent damage from XFP modules.
- e) thermal requirements (case temperatures)
- f) electromagnetic interference (EMI) recommendations (including necessary shielding features to seal the OEM chassis front panel output with and without the QSFP+ module installed in the cage.)
- g) electrostatic discharge (ESD) requirements solely to the extent disclosed in the Specification where the sole purpose of such disclosure is to enable products to operate, connect or communicate as defined within the Specifications.

3.2 The overall package dimension shall conform to the indicated dimensions and tolerances indicated in clause 5. The mounting features shall be located such that the products are mechanically interchangeable with the cage and connector system. In addition, the overall dimensions and mounting requirements for the cage and connector system on a circuit board shall be configured such that the products are mechanically and electrically interchangeable and the overall dimensions and insertion requirements for the optical connector and corresponding fiber optic cable plug shall be such that the products are mechanically and optically interchangeable.

3.3 The electrical and optical specifications may be compatible with those enumerated in the ITU-T Recommendation G.957 (STM-1, STM-4 and STM-16), Telcordia Technologies GR-253-CORE (OC-3, OC-12, OC-48 and OC-192), Ethernet IEEE 802.3 (Gigabit, 10Gigabit and 40Gigabit Ethernet), InfiniBand Architecture Specifications (SDR, DDR and QDR), SFF-8431, or Fibre Channel-PI-3/4 (2GFC, 4GFC, 8GFC) and 10GFC. Electrical and optical specifications may be compatible with standards under development.

3.4 The Specifications will provide a common solution for combined four-channel ports that support SONET/SDH and/or Ethernet and/or InfiniBand and/or Fibre Channel specifications. This specification encompasses design(s) capable of supporting multimode, single mode Modules, passive copper, active copper and active optical cables.

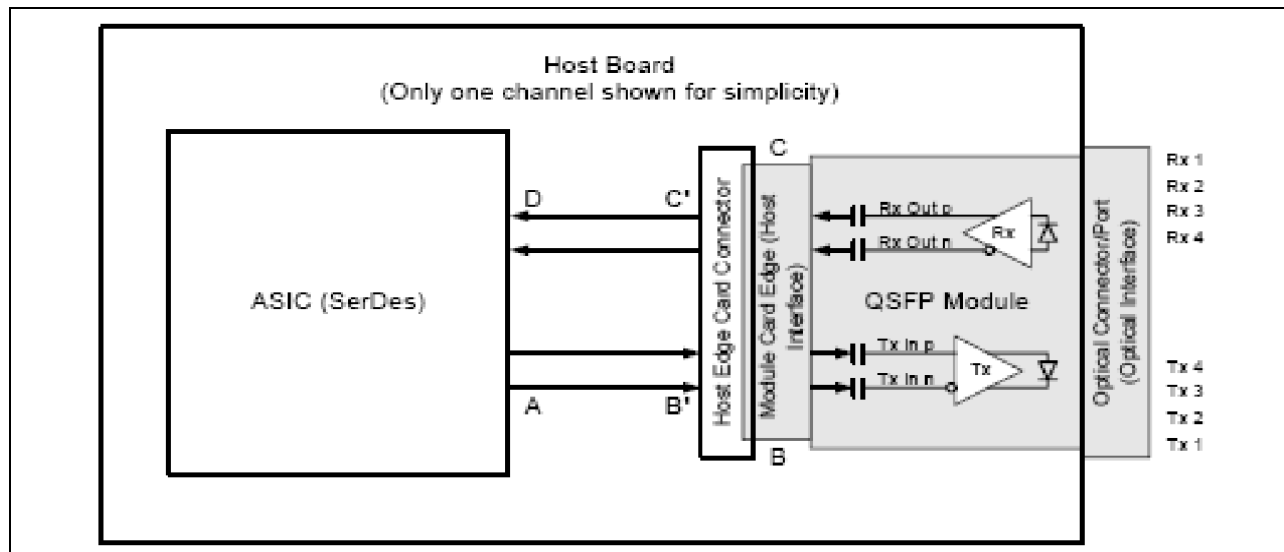
Table 1 - Multimode fiber applications

Distance	Fiber Type Core Diameter MHZ*km	IEE 802.3			Fibre Channel- FC-PI-2/3/4				InfiniBand		
		1G E	10 GE	40 GE	2 GFC	4 GFC	8 GFC	10 GFC	SDR	DDR	QDR
275m	62.5/200	X									
220m	62.5/160	X									
26m	62.5/160		X					X			
33m	62.5/200		X					X			
150m	62.5/200				X						
75m	62.5/200								X		
70m	62.5/200					X					
50m	62.5/200									X	
21m	62.5/200						X				
550m	50/500	X									
500m	50/400	X									
66m	50/400		X					X			
82m	50/500		X					X			
300m	50/2000		X					X			
300m	50/500				X						
150m	50/500					X					
125m	50/500								X		
75m	50/500									X	
50m	50/500						X				
200m	50/2000				X				X		
380m	50/2000					X					
150m	50/2000						X			X	
100m	50/2000			X							X
150m	50/4700			X							

Table 2 - Single mode fiber applications

Distance	Fiber type	IEEE 802.3			Fibre Channel FC-PI-2/3/4				InfiniBand		
		1 GE	10 GE	40 GE	2 GFC	4 GFC	8 GFC	10 GFC	SDR	DDR	QDR
1.4km	SM						X				
2km	SM										
4km						X					
10km	SM	X	X	X	X	X	X	X	X	X	X
30km	SM		X					X			
40km	SM		X					X			

An application reference Model, See Figure 1, shows the high-speed data interface between an ASIC (SerDes) and the QSFP+ module. Only one data channel of the interface is shown for simplicity. Either parallel MPO or duplex LC fiber connectors can be used for the optical interface.



Notes:

QSFP+ reference points for 6 Gb/s and lower speeds are as follows:

A: Host ASIC transmitter output at ASIC package pin on a DUT board

B: Host ASIC transmitter output across the Host Board and Host Edge Card connector at the Module Card Edge interface

B': Host ASIC transmitter output across the Host Board at Host Edge Card Connector

C: QSFP+ receiver output at the Module Card Edge interface

C': QSFP+ receiver output at Host Edge Card Connector

D: QSFP+ receiver output at Host ASIC package receiver input pin on a DUT board

For speeds above 6Gb/s the compliance board methodology of IEEE802.3ba, FC-P14 and SFF8431 should be used. Measurements taken with QSFP+ compliance boards should be corrected for any difference between the loss of these compliance boards and the loss of the compliance boards specified in the standard.

Figure 1 – Application reference model

4 Electrical specification

This clause contains pin definition data for the QSFP+ Module. The pin definition data is generic for gigabit -per-second datacom applications such as Fibre Channel and Gigabit Ethernet and SONET/ATM applications. Compliance Points for high-speed signal electrical measurements are defined in Figure 1. Compliance Points for all other electrical signals are at comparable points at the host edge card connector.

4.1 Electrical connector

Figure 2 shows the signal symbols and contact numbering for the QSFP+ Module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 38 contacts intended for high speed, low speed signals, power and ground connections. Table 3 provides more information about each of the 38 contacts.

For EMI protection the signals to the connector should be shut off when the QSFP+ Module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the QSFP+ module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

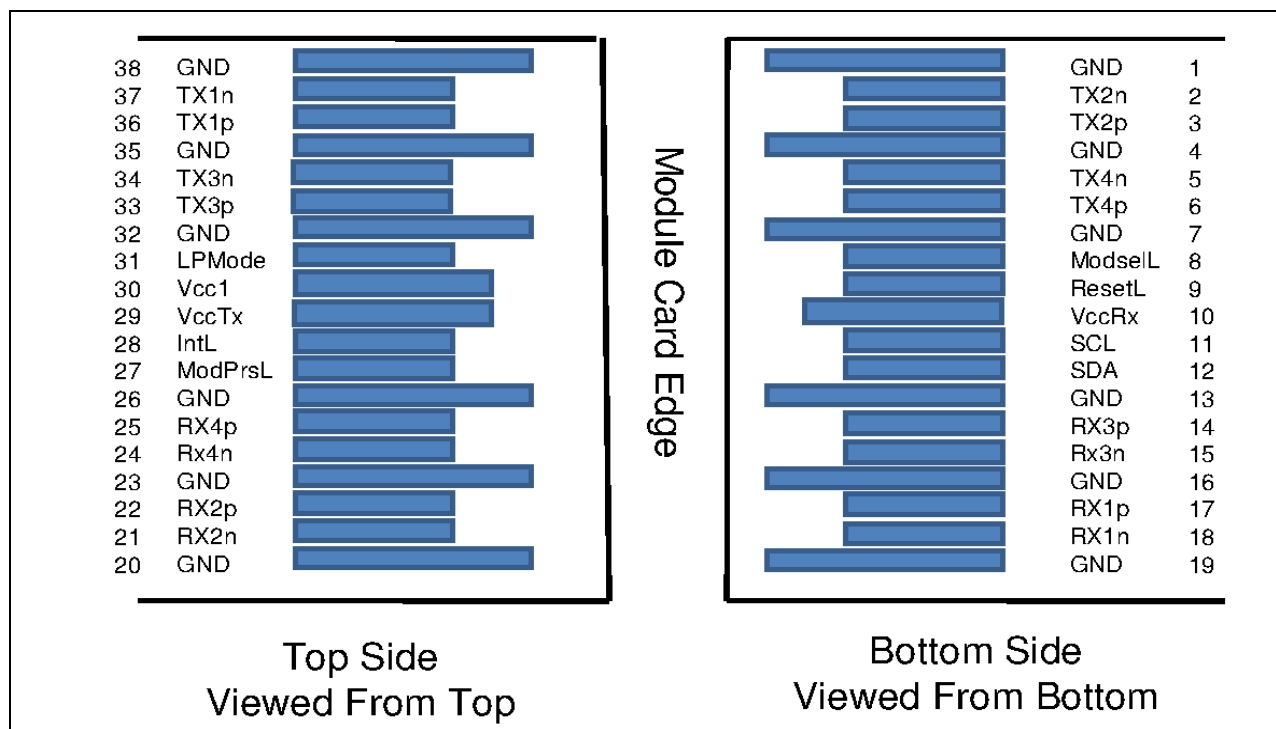


Figure 2 - QSFP+ module pad layout

Table 3 - Pin function definition (see Figure 10 for pad dimensions)

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1

Table 3 - Pin function definition (see Figure 10 for pad dimensions) (continued)

Pin	Logic	Symbol	Description	Plug Sequence	Notes
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

NOTES –

1 GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2 Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Figure 1: Typical QSPF+ module block diagram.

The diagram illustrates the internal architecture and external connections of a QSPF+ module. Key components and their connections include:

- Host System:** Provides $V_{cc\ Host} = +3.3V$ and ground. It connects to the PLD/PAL, Protocol IC, and Micro Controller.
- PLD/PAL:** Manages signals: $ModPrsL$, SCL , SDA , $ModSelL$, $ResetL$, $IntL$, and $LPMODE$.
- Protocol IC:** Handles signals: $TXDisable$, $TXFault$, $RXLOS$, $RXRate$, and $RXRate$.
- Micro Controller:** Connected to SCL and SDA .
- Quad SERDES IC:** Features 100 ohm termination resistors on $RX1p/n$, $RX2p/n$, $RX3p/n$, and $RX4p/n$. It is connected to the Protocol IC via $Tx\ Data\ Bus$ and $Rx\ Data\ Bus$. It also has $TX1p/n$, $TX2p/n$, $TX3p/n$, and $TX4p/n$ outputs.
- Quad TIA & Limiting Amplifier:** Connected to the RX inputs of the Quad SERDES IC.
- Quad Laser Driver:** Connected to the TX outputs of the Quad SERDES IC.
- Power and Ground:** Includes V_{ccRx} , V_{ccTx} , and V_{cc1} , each with 22 uF decoupling capacitors and 0.1 uF bypass capacitors. Inductors of 1 uH are used for the TX and RX lines.

Note: Decoupling capacitor values are informative and vary depending on applications.

Note: V_{cc1} connection may be connected to $V_{cc\ Tx}$ or V_{ccRx} provided the applicable derating of the maximum current limit is used.

Figure 3a - Example QSFP+ host board schematic for optical modules

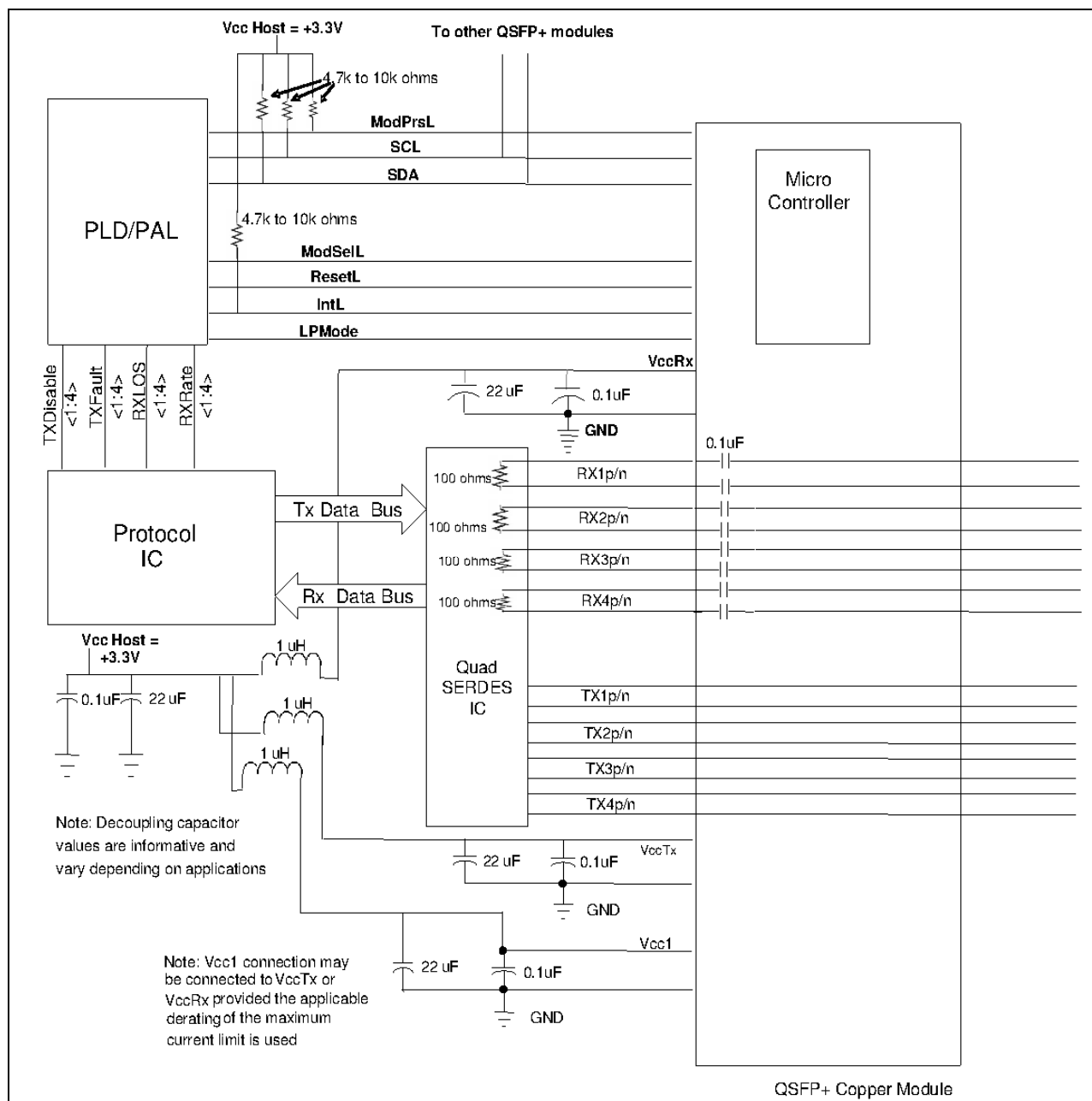


Figure 3b - Example QSFP+ host board schematic for passive copper cables

4.1.1 Low speed electrical hardware pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModSelL
- ResetL
- LPMode
- ModPrsL
- IntL

4.1.1.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.1.1.2 ResetL

The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length ($t_{\text{Reset_init}}$) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting “low” an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

4.1.1.3 LPMode

The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).

The module has two modes a low power mode and a high power mode. The high power mode operates in one of the four power classes.

When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

The modules 2-wire serial interface and all laser safety functions must be fully operational in this low power mode. The module shall still support the completion of reset interrupt in this low power mode.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate a power consumption greater than 1.5W and the module is in low power mode it must reduce its power consumption to less than 1.5W while still maintaining the functionality above. The exact method of accomplishing low power is not specified, however it is likely that either the Tx or Rx or both will not be operational in this state.

If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that its power consumption is less than 1.5W then the module shall be fully functional independent of whether it is in low power or high power mode.

The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_override bit is in the high state and the Power set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power override bit is high and the Power set bit is low. Note that the default state for the Power override bit is low.

A truth table for the relevant configurations of the LPMode and the Power over-ride and Power set are shown in Table 4.

Table 4 - Power mode truth table

LPMode	Power override Bit	Power set Bit	Module power allowed
1	0	X	Low Power
0	0	X	High Power
X	1	1	Low Power
X	1	0	High Power

At Power up, the Power override and Power set bits shall be set to 0.

4.1.1.4 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

4.1.1.5 IntL

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is deasserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’ and the flag field is read (see 7.6.1.2).

4.1.2 Low speed electrical specification

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Note 1 - Timing diagrams for SCL and SDA are included in clause 7.2.2.

The QSFP+ low speed electrical specifications are given in Table 5. This specification ensures compatibility between host bus masters and the 2-wire interface.

Table 5 - Low speed control and sense signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc+0.3	V	
	VIH	Vcc-0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms Pullup resistor, max
			200	pF	1.6 k Ohms Pullup resistor max
LPMode, Reset and Mod Sell	VIL	-0.3	0.8	V	IinI ≤125 μA for 0V<Vin, Vcc
	VIH	2	VCC+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	

4.1.3 High speed electrical specification

4.1.3.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP+ module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP+ module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 1600 mVpp or the relevant standard, whichever is less.

Note - Due to the possibility of insertion of QSFP modules into a host designed for QSFP+, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to clause 7.6.5.2.

4.1.3.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP+ module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP+ module. The AC coupling is inside the QSFP+ module and not required on the Host board. For operation at 6 Gb/s and below the inputs will accept single-ended voltage swings between 250 mV to 800 mV and differential voltage swings between 500 mVpp to 1600 mVpp. For best EMI results, single-ended swings between 250 mV and 600 mV and differential voltage swings between 500 mVpp to 1200 mVpp are recommended. For operation above 6 Gb/s see the appropriate specification, e.g. 802.3ba Annex 86A, FC-PI-4, FC-PI-5 or the InfiniBand specification. For 10G Ethernet reference SFF-8431.

Due to the possibility of insertion of QSFP+ modules into a host designed for QSFP interface per INF-8438i the damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set.

Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to clause 7.6.5.2.

4.2 Power requirements

The power supply has three designated pins, Vcc Tx, Vcc1, and Vcc Rx, in the connector. Vcc1 is used to supplement Vcc Tx or Vcc Rx at the discretion of the module vendor. Power is applied concurrently to these pins.

Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host, through the management interface, identify the power consumption class of the module before allowing the module to go into high power mode.

A host board together with the QSFP+ module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.2.1 Host board power supply filtering

The host board should use the power supply filtering equivalent to that shown in Figure 4.

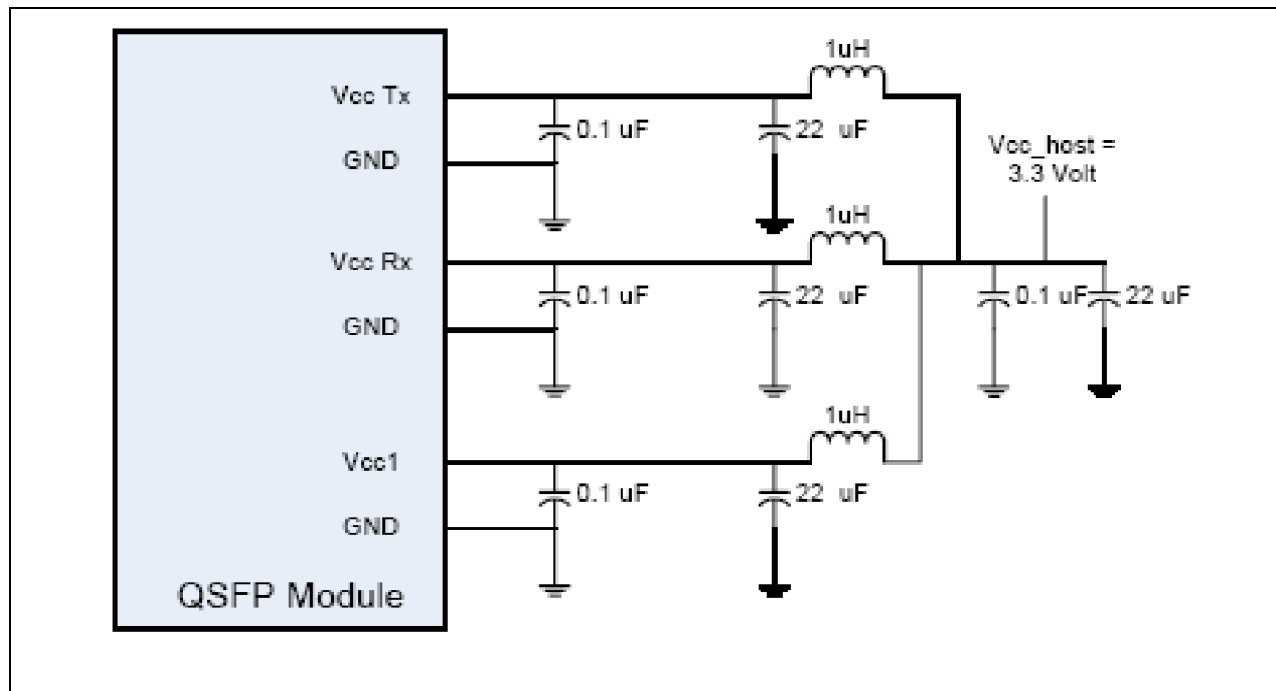


Figure 4 - Recommended host board power supply filtering

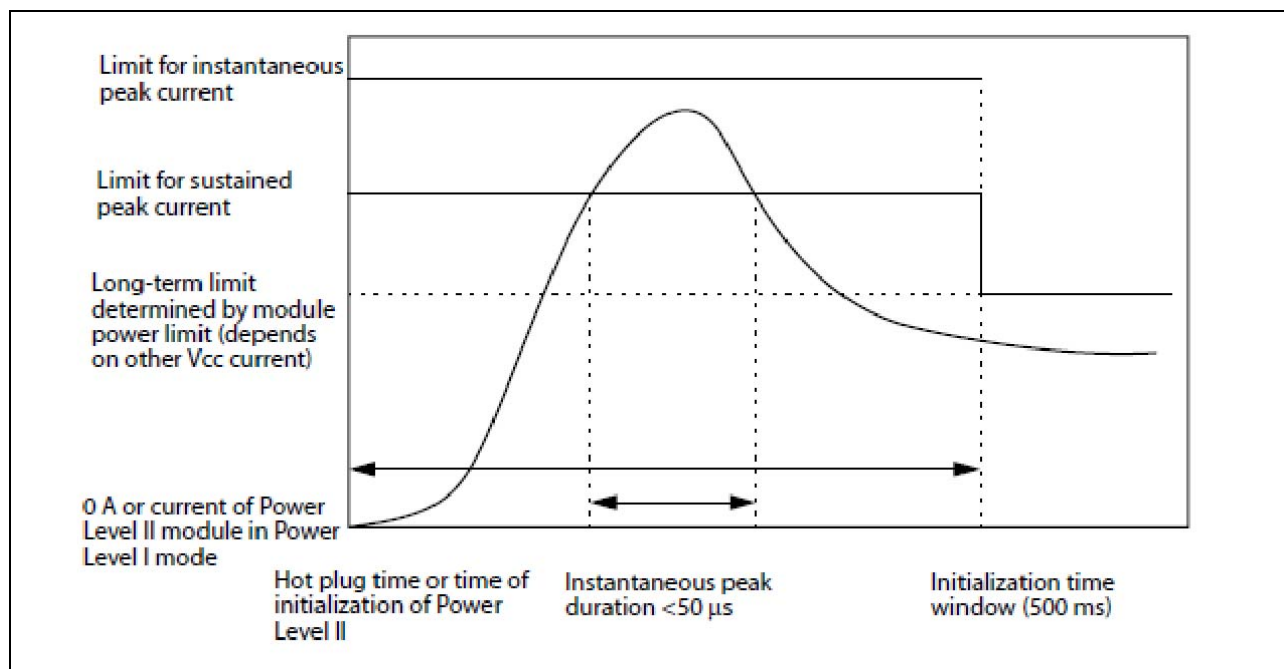
Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. It is recommended that the 22 μ F capacitors each have an equivalent series resistance of 0.22 ohm.

The specification for the power supply is shown in Table 6.

Table 6 - Power supply specification

Parameter	Min	Nominal	Max	Unit	Condition
Vcc		3.3		V	Measured at Vcc Tx, Vcc Rx and Vcc1.
Vcc set point accuracy	-5		5	%	Measured at Vcc Tx, Vcc Rx and Vcc1.
Power Supply Noise including ripple			50	mV	1kHz to frequency of operation measured at Vcc host.
Sustained peak current at hot plug with LPMODE Pin asserted			495	mA	See Figure 5
Maximum instantaneous current with LPMODE asserted			600	mA	See Figure 5
Module sustained peak current with LPMODE Pin deasserted			750	mA	
Maximum instantaneous current with LPMODE deasserted			900	mA	

These limits separately apply to the current that flows through each inductor in the power supply filter.

**Figure 5 - Instantaneous and sustained peak currents for Vcc1, Vcc Tx or Vcc Rx**

Power levels associated with classifications of modules are shown in Table 7.

Table 7 - Power budget classification

Power Level	Max Power (W)
1	1.5
2	2
3	2.5
4	3.5

In general, the higher power classification level is associated with higher data rates and longer reach. The system designer is responsible for ensuring that the maximum temperature does not exceed the case temperature requirements.

4.3 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the QSFP+ module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. The QSFP+ module and host high speed signal contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The QSFP+ module and all host contacts with exception of the module and host high speed signal contacts shall withstand 2 kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

5 Mechanical and board definition

5.1 Introduction

The overall module defined in this clause is illustrated in Figure 6. All Pluggable modules and direct attach cable plugs must mate to the connector and cage design defined in this specification. The QSFP+ optical interface shall meet the dimensional specifications of IEC 61754-7 interface 7-3, the MPO adapter interface, and shall optically mate with the plug on the optical fiber cabling. Several cage to bezel options are defined. Both metal spring finger and elastomeric EMI solutions are permitted but must pass customer defined requirements. Heat sink/clip thermal designs are application specific and not specifically defined by this specification, however a general design is given as an example.

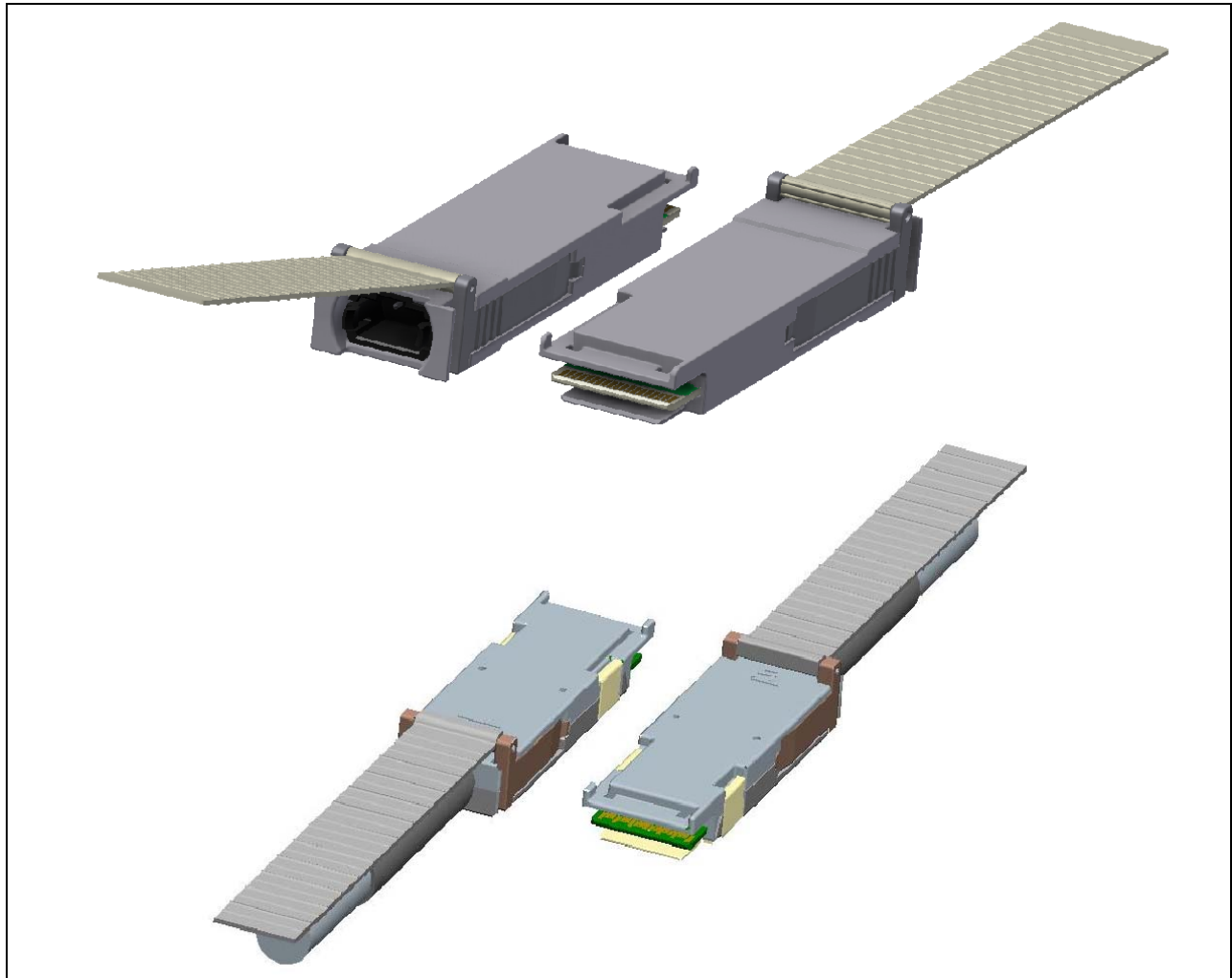


Figure 6 - QSFP+ pluggable and direct attach module rendering

5.2 QSFP+ datums and component alignment

A listing of the datums for the various components is contained in Table 8. The alignments of some of the datums are noted. The relationship of the Module, Cage, and Connector relative to the Host Board and Bezel is illustrated in Figure 7 by the location of the key datums of each of the components. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified.

Table 8 - Definition of datums

Datum	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	**Distance between Connector terminal thru holes on host board
D	*Hard stop on Module
E	**Width of Module
F	Height of Module housing
G	**Width of Module pc board
H	Leading edge of signal contact pads on Module pc board
J	Top surface of Module pc board
K	*Host board thru hole #1 to accept connector guide post
L	*Host board thru hole #2 to accept connector guide post
M	**Width of bezel cut out
N	*Connector alignment pin
P	**Width of inside of cage at EMI gasket (when fully compressed)
R	Height of inside of cage at EMI gasket (when fully compressed)
S	Seating plane of cage on host board
T	*Hard stop on cage
V	Length of heat sink clip
W	Seating surface of the heat sink on the cage
X & Y	Host board horizontal and depth datums
Z	**Width of heat sink surface that fits into clip
AA	**Connector slot width
BB	Seating plane of cage on host board
CC	Length of boss on heat sink that fits inside of the cage
DD	Top surface of connector backshell
NOTES *Datums D, K, L, N and T are aligned when assembled (see Figure 7) **Centerlines of datums AA, C, E, G, M, P and Z are aligned on the same vertical axis	

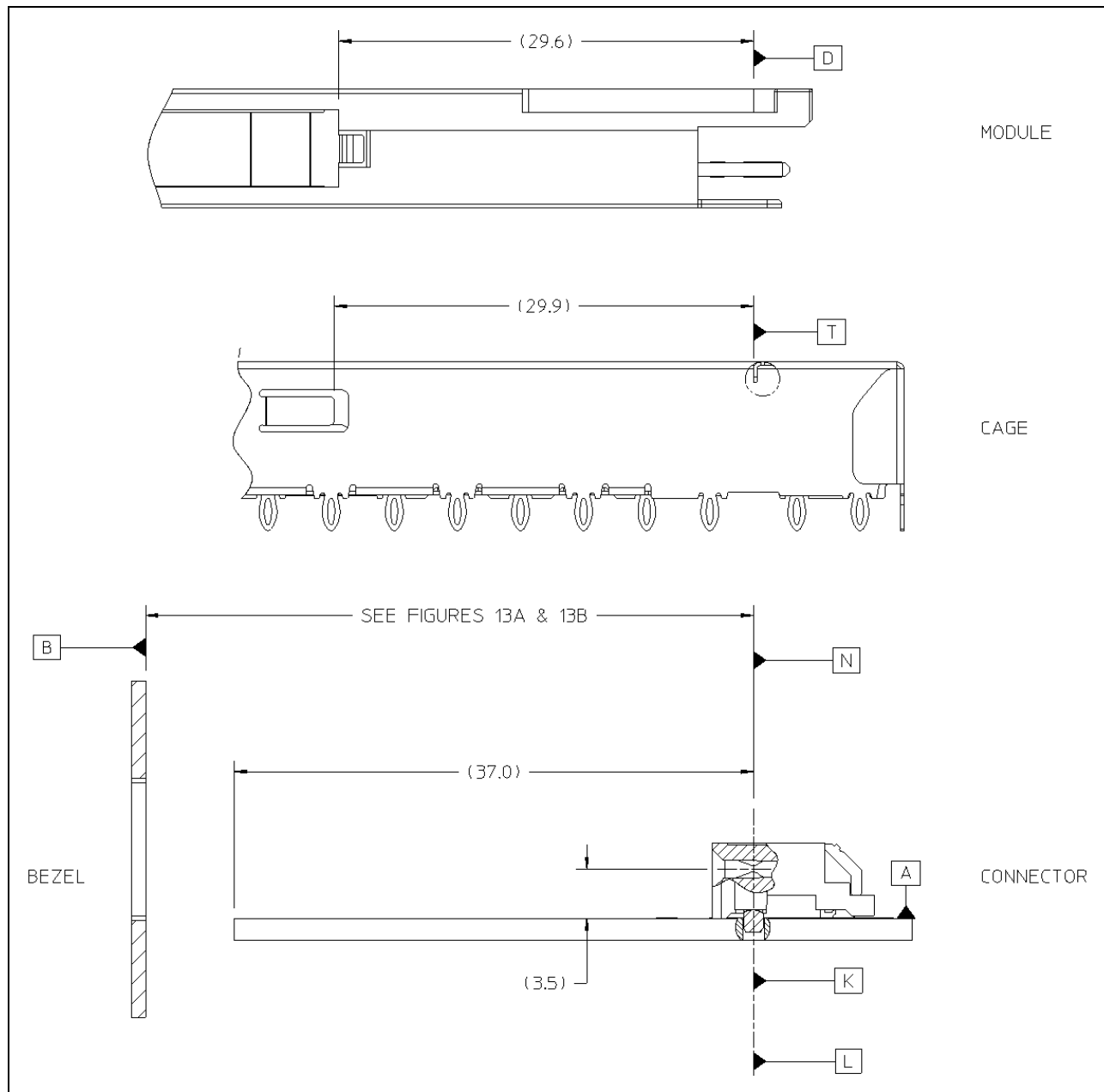


Figure 7 - QSFP+ datum alignment, depth

5.3 QSFP+ module mechanical package dimensions

A common mechanical outline is used for all QSFP+ Modules and direct attach cables. The preferred method of removing the module from the cage assembly is by a bail type actuation method. The module shall provide a means to self-lock with the cage upon insertion. The package dimensions for the QSFP+ Module are defined in Figure 8 and Figure 9. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 1 and Note 6 in Figure 8. Note: All dimensions are in millimeters.

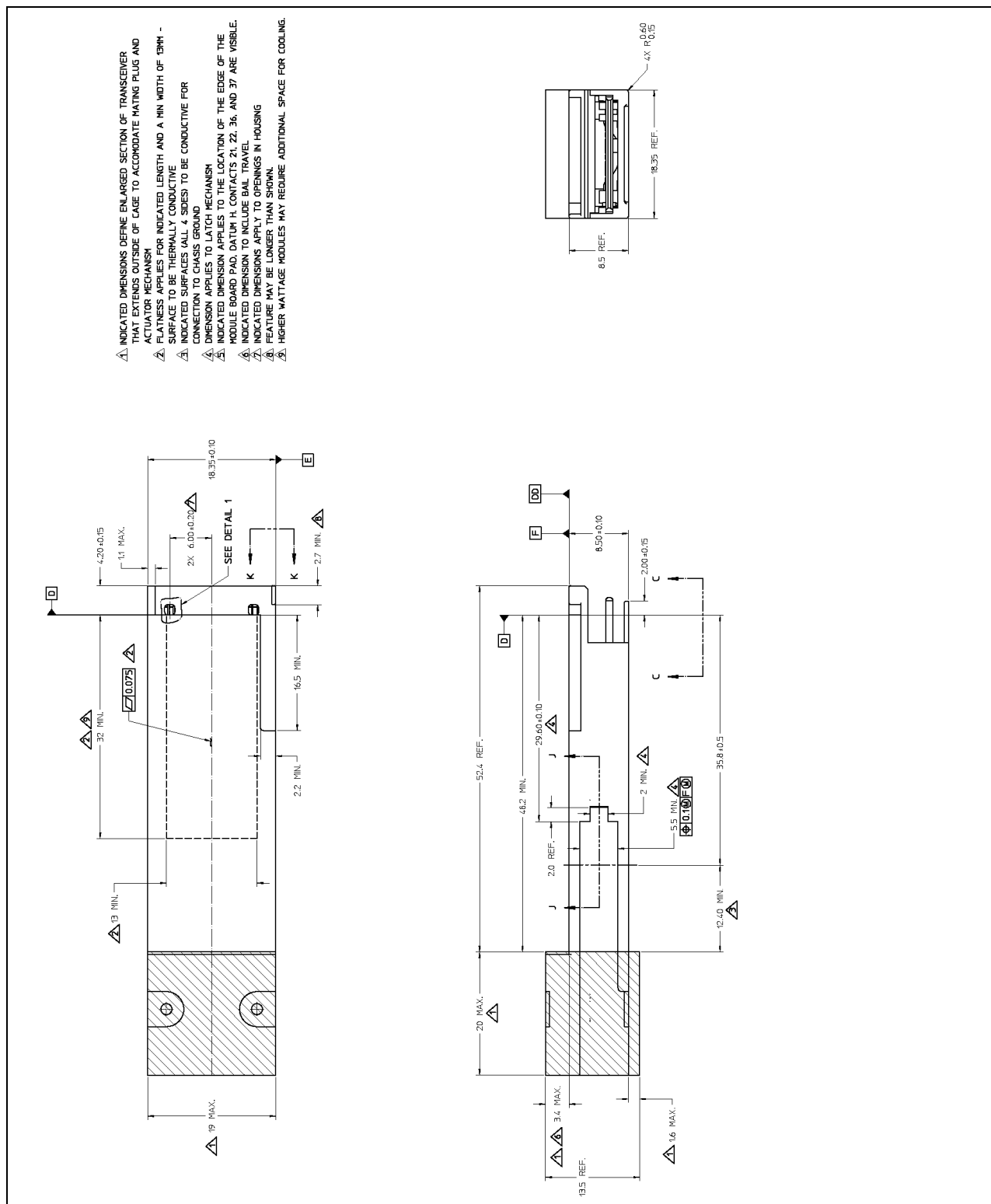


Figure 8 - Drawing of QSFP+ module