

EIA INTERIM STANDARD

IS-36

CHIP CAPACITORS, MULTI-LAYER
(CERAMIC DIELECTRIC)

IS-36

JANUARY 1987



Engineering Department

ELECTRONIC INDUSTRIES ASSOCIATION

NOTICE

EIA Engineering Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or non-member of EIA from manufacturing or selling products not conforming to such Standards and Publications, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than EIA members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by EIA without regard to whether or not their adoption may involve patents on articles, materials, or processes. By such action, EIA does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the Recommended Standard or Publication.

EIA INTERIM STANDARDS

EIA Interim Standards contain information deemed to be of technical value to the industry, and are published at the request of the originating Committee without necessarily following the rigorous public review and resolution of comments which is a procedural part of the development of an EIA Recommended Standard.

EIA Interim Standards should be reviewed on an annual basis by the formulating Committee and a decision made on whether to proceed to develop an EIA Recommended Standard on this subject. EIA Interim Standards must be cancelled by the Committee and removed from the EIA Standards Catalog before the end of their fifth year of existence.

Published by
ELECTRONIC INDUSTRIES ASSOCIATION
Engineering Department
2001 Eye Street, N.W.
Washington, D.C. 20006

PRICE: \$8.00

COPYRIGHT 1987
ELECTRONIC INDUSTRIES ASSOCIATION

Printed in U.S.A.



Documents
Document Sharing Hub

**EIA STANDARD SPECIFICATION SHEET
FOR
MULTIPLE LAYER UNENCAPSULATED CERAMIC
DIELECTRIC CHIP CAPACITORS**

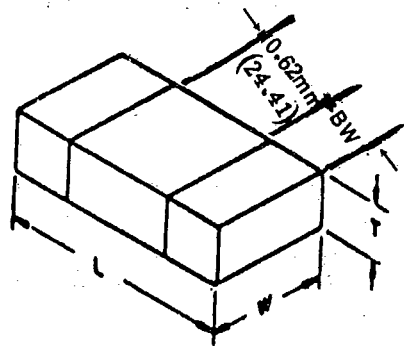


**FIGURE 1
SOLDERABLE TERMINATION DIMENSIONS**

<u>STYLE</u>	<u>LENGTH(L)</u>	<u>WIDTH(W)</u>	<u>THICKNESS(T)</u> MAX	<u>BANDWIDTH(BW)</u> MAX
CC0805	2.0(79) ± 0.2(8)	1.25(49) ± 0.2(8)	1.3(51)	0.7(28)
CC1206	3.2(126) ± 0.2(8)	1.6(63) ± 0.2(8)	1.5(59)	0.7(28)
CC1210	3.2(126) ± 0.2(8)	2.5(98) ± 0.2(8)	1.7(67)	0.7(28)
CC1812	4.5(177) ± 0.3(12)	3.2(126) ± 0.2(8)	1.7(67)	0.75(30)
CC1625	4.5(177) ± 0.3(12)	6.4(252) ± 0.4(16)	1.7(67)	0.75(30)

ALL DIMENSIONS = MILLIMETERS (MILS)

IS-36
Page 2

REQUIREMENTS

Type: Unencapsulated ceramic dielectric capacitors with solderable terminations.

Dimension and Configuration: See Figure 1.

Available Characteristics: See Tables II, III, or IV.

Operating Temperature Range: See Table I.

Capacitance Values: Tables II, III, or IV in accordance with RS-198-C-1.

Dissipation Factor (or Q): See Table I in accordance with RS-198-C-1.

Dielectric Strength: 200% of rated voltage in accordance with RS-198-C-1.

Insulation Resistance: See Table I in accordance with RS-198-C-1.

Solderability: In accordance with RS-198-C-2-B7.
RMA Flux diluted 75/25

Termination Classifications: In accordance with RS-198-C-2-B4, Procedure 1, Test Condition F through H, whichever applies. (See Table VI.)

<u>CLASSIFICATION DESIGNATION</u>	<u>SOLDER IMMERSION TEST TIME</u>	<u>TEST CONDITION</u>	<u>COMMENT</u>
1	60 seconds	F	Basically a leach-resistant termination system.
2	30 seconds	G	Controlled leaching impact.
3	10 seconds	H	Leachable termination; minimum requirement.



Documents
Document Sharing Hub

CLASS 1: Terminations are a leach-resistant metallization system not usually affected by the soldering process. Dewetting is potentially a greater problem than metallization removal during soldering. These terminations are constructed by either non-leaching metallizations or by the protection of leachable metallizations by the use of barrier layers (typically of nickel or copper). Solder bond composition is not appreciably affected by metals added to the solder by the chip termination.

CLASS 2 & CLASS 3 Terminations are of a controlled leach type or leachable systems. The impact of soldering on the termination integrity is controlled by such factors as changes in metal alloy composition, care in its application and firing, control of surface condition, and basic thickness, particularly over edges.

Lower numbered classification designations may in general be substituted for higher numbers in soldering applications. Which classifications are suitable for what soldering processes is a question beyond the scope of this specification.

Capacitance Values, Tolerances, and Voltages:

- (1) COG (NPO): Table II
- (2) X7R: Table III
- (3) Z5U: Table IV

Marking: Table V

Environmental Requirements:

- (1) The temperature coefficient of capacitance or characteristics as shown in Table I shall be as specified in RS-198-C.
- (2) When humidity tested to RS-198-C-Method B-3, Condition C, capacitors shall meet the capacitance change, the Q (dissipation factor), and insulation resistance requirement of Table I.
- (3) When life tested per RS-198-C-Method C-2, the units shall meet the capacitance change, the Q (dissipation factor), and insulation resistance requirement of Table I.