

ESDA/JEDEC JS-002-2022

ESDA/JEDEC Joint Standard

ESDA/JEDEC JS-002-2022

Revision of ANSI/ESDA/JEDEC JS-002-2018



For Electrostatic Discharge Sensitivity Testing

Charged Device Model (CDM) Device Level

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*An American National Standard
Approved June 8, 2021*

***ESDA/JEDEC Joint Standard
For Electrostatic Discharge
Sensitivity Testing***

***Charged Device Model (CDM)
Device Level***

Approved June 8, 2021

EOS/ESD Association, Inc. & JEDEC Solid State Technology Association



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(This Foreword is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Foreword

This joint standard¹ was developed under the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a joint working group composed of both ESDA and JEDEC.

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM, a device itself becomes charged (for example, by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. Similarly, a non-charged device can experience CDM stress as a charged conductive object approaches and discharges to the device. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges from other similar scenarios, such as the discharging of charged metal objects to devices at a different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the measuring equipment's limitations and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on many factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage. It has also been shown that the CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package may be less susceptible to CDM damage at a given voltage than that same IC in a package of the same type with a larger area. Clause 7.5 and Annex C address small package CDM and outlines the procedure to characterize small packages (by technology/common ESD design to those in larger packages, capacitance measurement) such that CDM testing for those small packages may not be needed.

New information includes a procedure to determine multiple level CDM withstand thresholds for subsets of device pins and a more accurate definition of verification module physical characteristics and capacitance measurement/use of modules.

¹ESD Association Standard (S): A precise statement of a set of requirements to be satisfied by a material, product, system, or process that also specifies the procedures for determining whether each of the requirements is satisfied.

Foreword (cont'd)

A companion technical report document, ESDA/JEDEC JTR002-01, has also been released to act as a “user guide” for this CDM test standard. The information presented in the user guide is intended to help users better understand the procedures and requirements specified in this standard.

References to the user guide are made throughout this standard to aid the reader in the practical elements of adhering to the requirements outlined in this document.

This standard is maintained and revised as a joint standard through a memorandum of understanding between JEDEC and ESDA. This standard is a living document, and revisions and updates will be made on a routine basis driven by the electronic industry's needs.

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Foreword (cont'd)

This document was originally approved on August 29, 2014 and was designated ANSI/ESDA/JEDEC JS-002-2014. ANSI/ESDA/JEDEC JS-002-2018 was a limited revision of ANSI/ESDA/JEDEC JS-002-2014 and was approved on February 16, 2018.

ESDA/JEDEC JS-002-2022 is a revision of ANSI/ESDA/JEDEC JS-002-2018 and was approved on June 8, 2021.

ESDA/JEDEC JS-002-2022 was prepared by the ESDA 5.3.1 Device Testing (CDM) subcommittee and the JEDEC JC14.1 ESD Task Group.

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Foreword (cont'd)

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CHARGED DEVICE MODEL (CDM) DEVICE LEVEL

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CHARGED DEVICE MODEL (CDM) DEVICE LEVEL

(From Board Ballot JCB-22-08 jointly formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee.)

1 Scope

This document establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin-film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. The devices shall be assembled into a package similar to that expected in the final application to perform the tests. This CDM document does not apply to socketed discharge model testers.

The purpose (objective) of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative References

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms²

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices³

JESD88, Dictionary of Terms for Solid-State Technology³

JESD625, Requirements for Handling Electrostatic Discharge-Sensitive (ESDS) Devices³

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)²

IEC61340-5-1 – Electrostatics – Part 5-1: Protection of Electronic Devices from Electrostatic Phenomena – General Requirements⁴

² EOS/ESD Association, Inc., 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069; 315-339-6937;
www.esda.org

³ JEDEC Global Standards for the Microelectronics Industry; www.jedec.org

⁴ IEC – International Electrotechnical Commission, www.iec.ch

3 Terms and Definitions

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at www.esda.org.

above-passivation layer (APL). A low-impedance metal plane built on the surface of a die above the passivation layer connecting a group of bumps or pins (typically power or ground).

NOTE This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

charge time (delay). The amount of time the device is allowed to charge – any additional time is added to the default (set by the manufacturer) in most cases.

charged device model electrostatic discharge (CDM ESD). An ESD stress model that simulates the discharge event that occurs when a charged component is quickly discharged to another object at a different electrostatic potential through a pin.

charged device model (CDM) electrostatic discharge (ESD) tester. Equipment (referred to as "tester" in this standard) that simulates the device level CDM ESD event using the non-socketed test method.

C_{small}: Device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below the determined value that CDM testing is not required if specified conditions are met.

dielectric layer. A thin insulator placed atop the field plate that is used to separate the device from the field plate.

discharge time (delay). The amount of time that the pogo pin remains in contact with the pin under test – any additional time is added to the default (set by the manufacturer) in most cases.

field plate. A conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling (see Figure 1).

ground plane. A conductive plate used to complete the circuitry for grounding/discharging the DUT (see Figure 1).

IPA. Isopropyl alcohol or isopropanol, with a minimum percentage of 70% alcohol.

no-connect pin. A package contact (pin, bump, or ball) that is not electrically connected to a die.

software voltage. A user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system to achieve the waveform parameters as defined in Table 1 or Table 2.

supply pin. Any device pin that provides operating current to that device.

NOTE Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current levels). For ESD testing, power and ground pins are treated as supply pins.

test condition (TC). For purposes of this document, a test condition refers to the tester plate voltage that meets the waveform parameter conditions in a particular column of Table 1 and Table 2.

4 Personnel Safety

THE EQUIPMENT SHALL NOT BE INSTALLED OR OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.

ALL PERSONNEL SHOULD RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING BEFORE USING THE EQUIPMENT.

THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES, AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.

GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.

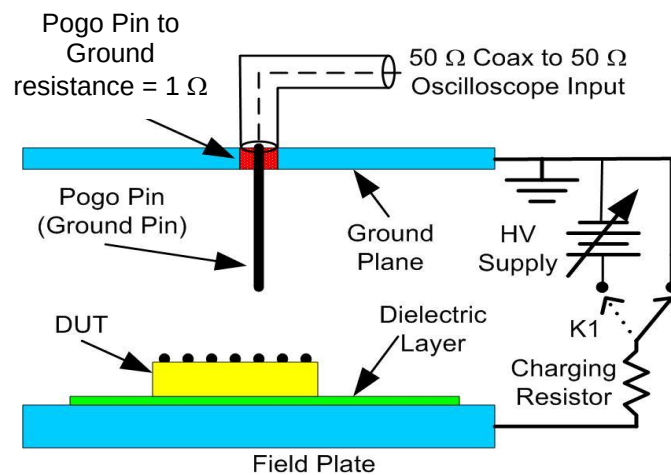
ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED, AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.

NOTE CDM testers have moving parts when in operation and care should be taken to avoid personnel contact with moving parts.

5 Required Equipment

5.1 CDM ESD Tester

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device, or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 ohm current path. When measuring waveforms, the 1 ohm pogo pin to ground connection of the resistive current sensor will be a parallel combination of a 1 ohm resistor between the pogo pin and the ground plane and the 50 ohm impedance of the oscilloscope and its coaxial cable. K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this standard shall meet the waveform characteristics specified in Figure 2, Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe assembly.



NOTE When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance, inductance, and capacitance (RLC) parasitics in the equipment greatly influence the test results.

Figure 1 — Simplified CDM Tester Hardware Schematic

5.1.1 Current Sensing Element

A current sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of $1.0\ \text{ohm} \pm 10\%$. A resistor, as specified in Clause 5.1, shall be used as the current sensing element. The value of resistance (including the 50 ohm cable and its termination) shall be measured using an ohm meter as described in Clause 5.5. The resistance value shall be used to calculate the peak currents.

The current sensing element shall have a minimum frequency response of 9 GHz (specified by maximum roll off of 3 dB at 9 GHz).

NOTE More information on the measurement of the current sensing element can be found in the user guide ESDA/JEDEC JTR002-01 “For the User Guide of ANSI/ESDA/JEDEC JS-002.

5.1.2 Ground Plane

The probe assembly shall contain a square ground plane with the probe pin centered within it, as shown in Figure 1. The dimensions of the ground plane shall be 63.5 mm x 63.5 mm $\pm$ 6.35 mm.

5.1.3 Field Plate/Field Plate Dielectric Layer

The field plate shall have a surface flatness to vary no more than 0.127 mm. The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0.381 mm $\pm$ 0.025 mm to result in a capacitance measurement (as specified in Annex B) in the range specified in Table 4 in Annex A.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table 4 in Annex A.

5.1.4 Charging Resistor

The charging resistor shown in Figure 1 shall nominally be 100 megohms or greater.

Resistor values higher than 100 megohms may be used, but this may not allow very large devices (refer to Clause 6.9 and Annex J) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 megohms, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for charging large devices. A procedure for this large device delay characterization is given in Annex J.

5.1 Waveform Measurement Equipment

The CDM waveform measurement equipment shall consist of the following components.

5.2.1 Cable Assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 5 GHz and a nominal 50 ohm impedance.

5.2.2 Equipment for High Bandwidth Waveform Measurement

5.2.2.1 High Bandwidth Oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/sec sampling rate with a nominal 50 ohm input impedance.

5.2.2.2 Attenuator

A 20 dB attenuator with a precision of ± 0.5 dB, at least 12 GHz BW, and an impedance of 50 ohms ± 5.0 ohms.

5.2.3 Equipment for 1 GHz Waveform Measurement

5.2.3.1 1 GHz Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 ohm input impedance. The sampling rate shall be ≥ 5 gigasample/sec.

NOTE The user can use a higher BW oscilloscope and use a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in Clause 5.2.3.1.

5.2.3.2 Attenuator

A 20 dB attenuator with a precision of ± 0.5 dB, at least 4 GHz BW, and an impedance of 50 ohms ± 5 ohms.

5.3 Verification Modules (Metal Discs)

The large verification module shall have a capacitance of 55 pF $\pm 13\%$ and the small verification module shall have a capacitance of 7.2 pF $\pm 13\%$. Refer to Annex A for information on the verification module physical dimensions and Annex B for information on the capacitance measurement procedure.

5.4 Capacitance Meter

Capacitance meter with a resolution of 0.2 pF, measurement accuracy of 3%, and a measurement frequency of 1.0 MHz as described in Annex B.

5.5 Ohm Meter

The ohm meter used to measure the resistive probe's resistance shall be capable of measuring to an accuracy of 0.01 ohms using a Kelvin 4-wire connection.

6 Periodic Tester Qualification, Waveform Records, and Verification Requirements

6.1 Overview of Required CDM Tester Evaluations

The CDM tester shall be qualified, requalified, and periodically verified as described in this clause. The safety precautions described in Clause 4.0 shall be followed at all times.

NOTE Changes in the shape of the discharge pulse, even though they may still be within specification, may indicate degradation of the discharge path.

6.2 Waveform Capture Hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- Oscilloscope - as specified in Clause 5.2.
- Attenuator and cable assembly as defined in Clause 5.2.
- Verification modules (as described in Clause 5.3) - with the dimensions and attributes listed in Annex A and measurement methods listed in Annex B.

6.3 Waveform Capture Setup

The procedure for waveform capture setup follows these steps:

- 1) Clean the verification modules. Avoid skin contact with the modules before and during testing. A recommended procedure is described in Annex A.
- 2) Using an IPA wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.
- 3) Attach the appropriate 20 dB attenuator as described in Clause 5.2 to the oscilloscope. Attach one end of the external cable assembly, as described in Clause 5.2.1, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See Annex G for an example of oscilloscope settings and captured waveforms.

NOTE See also the ESDA/JEDEC JTR002-01 User Guide.