

# **ESD Association Standard Practice**

***For Electrostatic Discharge  
Sensitivity Testing***

***Human Body Model (HBM) Testing –  
Component Level***

***A Method for Randomly Selecting  
Pin Pairs***



***Electrostatic Discharge Association  
7900 Turin Road, Bldg. 3  
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Sensitivity Testing –  
Human Body Model (HBM) Testing –  
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## FOREWORD

Human body model (HBM) events can theoretically happen between any two pins and therefore the HBM test should describe the stress by zapping one pin and putting the other pin to tester ground. However, even in the early 80's, when devices were assembled in low pin count DIP packages, this ended in too many stress combinations, and, consequently, pin combinations have been defined which reduce the number of stress combinations.

Those pin combinations defined in legacy industry standards are still widely used today for the qualification of modern semiconductor devices with hundreds or even thousands of pins or balls. By the 90's this resulted in a dramatic increase in test time along with the need for a lot of tester channels. The industry solved that problem by reducing the number of zaps per stress combination, the time between two zaps and by introducing optimized pin combinations such as in Table 2A of ANSI/ESDA/JEDEC JS-001.

With the trend of increasing product complexity and an increasing number of power domains, not only is the number of stress pulses (and therefore test time) increasing, but we are also seeing new spurious failure mechanisms such as gate oxide failures in the core, which occur as a result of excessive repetitive stressing to the same discharge path. The need to reduce the stress count is addressed by the current ANSI/ESDA/JEDEC JS-001 – ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level. “Partitioned testing” (see Table 2A in ANSI/ESDA/JEDEC JS-001) reduces the amount of cross-domain stressing. Sampling of non-supply cloned I/O pins reduces the overall number of stresses in components with a large number of identical (“cloned”) signal pins.

Both approaches in ANSI/ESDA/JEDEC JS-001 have two fundamental drawbacks. First, the number of stresses a component is exposed to is high compared to the real-world scenario in which a component typically sees only one zap. Secondly, it is required to have a detailed knowledge of the design of the component; e.g., associated supply pins for non-supply pins have to be identified which is often rather difficult and requires design and ESD expertise. However, this knowledge is not necessarily available for the personnel performing the qualification tests.

The approach defined in this standard practice<sup>1</sup> goes a radical new way. Instead of grouping pins into supply and non-supply pins, all pins are treated equally. Each pin is stressed (i. e. tied to Terminal A) once against one randomly selected other pin tied to Terminal B, and each pin is tied once to tester ground (Terminal B) and a randomly selected other pin is stressed against this pin. The pin-pair selection procedure hence allows a true two-pin test which can be performed by any tester that meets ANSI/ESDA/JEDEC JS-001. This standard practice defines a new method for determining a set of pin combinations which can be used instead of Table 2A or Table 2B in ANSI/ESDA/JEDEC JS-001. Stress test equipment qualification and routine verification, classification procedure, failure criteria and component classification defined in ANSI/ESDA/JEDEC JS-001 are unchanged.

Obviously, the only information of the component which is required is the pin list and possibly no-connect pins if those should be excluded from stressing. According to the data published in [1] and [2], the stress count reduction and hence the test time reduction can be up to 95 percent, depending on the complexity of the component. Experiments clearly demonstrate ([1] and [2]) that the proposed pin-pair selection method avoids wear-out due to overstress and is a more realistic test scenario. However, for the “classic” HBM failure signature, thermal overload, the stressing of these randomly selected pin-pairs leads to the same test results as stressing according to Table 2A or Table 2B in ANSI/ESDA/JEDEC JS-001. Of course, this cannot be taken for granted. The true two-pin stress approach might occasionally address fails in “weak” discharge paths, e.g. between two

<sup>1</sup> **ESD Association Standard Practice (SP):** A procedure for performing one or more operations or functions that may or may not yield a test result. Note, if a test result is obtained it may not be reproducible.