

ANSI-ESD SP5.4.1-2017

ESD Association Standard Practice

ANSI/ESD SP5.4.1-2017

***For Latch-up Sensitivity Testing of
CMOS/BiCMOS Integrated Circuits***

***Transient Latch-up Testing
Device Level***



***Electrostatic Discharge Association
7900 Turin Rd., Bldg. 3
Rome, NY 13440***

***An American National Standard
Approved February 27, 2018***

***ESD Association Standard Practice
for Latch-up Sensitivity Testing of
CMOS/BiCMOS Integrated Circuits***

***Transient Latch-up Testing
Device Level***

Approved September 20, 2017
EOS/ESD Association, Inc.



CAUTION NOTICE

Electrostatic Discharge Association (ESDA) standards and publications are designed to serve the public interest by eliminating misunderstandings between manufacturers and purchasers, facilitating the interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining the proper product for his particular needs. The existence of such standards and publications shall not in any respect preclude any member or non-member of the Association from manufacturing or selling products not conforming to such standards and publications. Nor shall the fact that a standard or publication that is published by the Association preclude its voluntary use by non-members of the Association, whether the document is to be used either domestically or internationally. Recommended standards and publications are adopted by the ESDA in accordance with the ANSI Patent policy.

Interpretation of ESDA Standards: The interpretation of standards in-so-far as it may relate to a specific product or manufacturer is a proper matter for the individual company concerned and cannot be undertaken by any person acting for the ESDA. The ESDA Standards Chairman may make comments limited to an explanation or clarification of the technical language or provisions in a standard, but not related to its application to specific products and manufacturers. No other person is authorized to comment on behalf of the ESDA on any ESDA Standard.

DISCLAIMER OF WARRANTIES

THE CONTENTS OF ESDA'S STANDARDS AND PUBLICATIONS ARE PROVIDED "AS-IS," AND ESDA MAKES NO REPRESENTATIONS OR WARRANTIES, EXPRESSED OR IMPLIED, OF ANY KIND, WITH RESPECT TO SUCH CONTENTS. ESDA DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, AND NON-INFRINGEMENT.

DISCLAIMER OF GUARANTY

ESDA STANDARDS AND PUBLICATIONS ARE CONSIDERED TECHNICALLY SOUND AT THE TIME THEY ARE APPROVED FOR PUBLICATION. THEY ARE NOT A SUBSTITUTE FOR A PRODUCT SELLERS' OR USERS' OWN JUDGEMENT WITH RESPECT TO ANY PARTICULAR PRODUCT DISCUSSED, AND ESDA DOES NOT UNDERTAKE TO GUARANTEE THE PERFORMANCE OF ANY INDIVIDUAL MANUFACTURERS' PRODUCTS BY VIRTUE OF SUCH STANDARDS OR PUBLICATIONS. THUS, ESDA EXPRESSLY DISCLAIMS ANY RESPONSIBILITY FOR DAMAGES ARISING FROM THE USE, APPLICATION, OR RELIANCE BY OTHERS ON THE INFORMATION CONTAINED IN THESE STANDARDS OR PUBLICATIONS.

LIMITATION ON ESDA's LIABILITY

NEITHER ESDA, NOR ITS MEMBERS, OFFICERS, EMPLOYEES OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES ARISING OUT OF, OR IN CONNECTION WITH, THE USE OR MISUSE OF ESDA STANDARDS OR PUBLICATIONS, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING, WITHOUT LIMITATION, LOSS OF DATA, INCOME OR PROFIT, LOSS OF OR DAMAGE TO PROPERTY, AND CLAIMS OF THIRD PARTIES.

Published by:

EOS/ESD Association, Inc.
7900 Turin Road, Bldg. 3
Rome, NY 13440

Copyright © 2018 by ESD Association
All rights reserved

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Printed in the United States of America

ISBN: 1-58537-296-X

(This foreword is not part of ESD Association Standard Practice ANSI/ESD SP5.4.1-2017)

FOREWORD

Latch-up failures can occur in products which do not show latch-up sensitivity when tested with “static” pulses (JEDEC JESD78E). The trigger for latch-up in these situations is often found to be very fast transients, either on input or output circuits or power supplies. This kind of latch-up is called transient induced latch-up, commonly known as transient latch-up (TLU). Such fast transients might be, but are not limited to, electrostatic discharges like ESD system level pulses or cable discharge events.

TLU is a real threat for integrated circuits. In technical report TR5.4-04-13 (published July 2013) written by ESDA WG 5.4, several examples of TLU are listed. Those examples can be categorized with respect to the occurrence and the root cause of the TLU and with respect to appropriate test methods to reproduce the TLU event in a lab. There are several examples published in which ICs are latch-up sensitive in stress tests which are intended to reproduce real-world stress conditions – and therefore there is a certain risk that TLU can occur in the field. There are even examples of field returns which have to be avoided by all means. Therefore, a characterization methodology to guarantee a certain robustness of potentially susceptible pins of ICs in the application is desirable.

The “static” standard latch-up qualification procedure JEDEC JESD78E currently does not cover transient threats. The former TLU standard practice¹, ANSI/ESD SP5.4 (now ESD TR5.4-03-11), is difficult to relate to real world stress. Lacking any appropriate standard, test equipment which could reproduce typical field fails is currently not available commercially. Currently TLU studies must be done using experimental prototypes which address some of the known TLU examples.

The TLU test method requires a pre-conditioning of the device, a stress pulse to the device and a latch-up detection mechanism. These steps are similar to the procedure in ESD TR5.4-03-11, however, with different constraints to the blocks which allows a more universal approach to today’s applications. This document defines pre-conditioning of the device-under-test, applying the stress pulse, detecting latch-up, and determining failure criteria with a special focus on the verification of all components of the TLU set-up. The procedures described in the standard practice shall be used as a method to characterize possible susceptible pins of a device. It is not the intention of the working group that this method be used as a “standard qualification methodology” of a product, as, for example, the static latch-up qualification according to JEDEC JESD78E.

This document was designated ANSI/ESD SP5.4.1-2017 and approved on September 20, 2017.

¹ **ESD Association Standard Practice (SP):** A procedure for performing one or more operations or functions that may or may not yield a test result. Note, if a test result is obtained it is not reproducible.

At the time ANSI/ESD SP5.4.1-2017 was prepared, the 5.4 Device Testing (TLU) Subcommittee had the following members:

Wolfgang Stadler, Chair Intel Deutschland GmbH		
Robert Ashton ON Semiconductor (Retired)	Jon Barth Barth Electronics, Inc.	Brett Carn, TAS Rep Intel Corporation
Lorenzo Cerati STMicroelectronics	Marcel Dekker MASER Engineering	Reinhold Gaertner Infineon Technologies AG
Horst Gieser Fraunhofer EMFT	Vaughn P. Gross Green Mountain ESD Labs, LLC	Evan Grund Grund Technical Solutions, Inc.
Leo G. Henry ESD/TLP Consultants	Timothy J. Maloney CAI	Tom Meuse Thermo Fisher Scientific
Gregory O'Sullivan Micron Semiconductor, Inc.	Nathaniel Peachey Qorvo, Inc.	Bill Reynolds GLOBALFOUNDRIES
Alan Righter Analog Devices, Inc.	Masanori Sawada Hanwa Electronic Ind. Co, Ltd.	Mirko Scholz imec
Theo Smedes NXP Semiconductors	Dietmar Walther Texas Instruments, Inc.	Terry Welsher Dangelmayer Associates
Xiong Ying Huawei		

The following individuals made significant contributions to ANSI/ESD SP5.4.1-2017:

Krzysztof Domanski Intel Deutschland GmbH	Steven Voldman Steven H. Voldman, LLC	Scott Ward Texas Instruments, Inc.
--	--	---------------------------------------

TABLE OF CONTENTS

1.0 PURPOSE, SCOPE, AND APPLICATION	1
1.1 PURPOSE	1
1.2 SCOPE	1
1.3 APPLICATION	1
2.0 REFERENCED DOCUMENTS	1
3.0 DEFINITION OF TERMS.....	2
4.0 PERSONNEL SAFETY	2
5.0 DEVICE HANDLING	3
6.0 GENERAL TLU CHARACTERIZATION FLOW	3
7.0 EQUIPMENT AND VERIFICATION	4
7.1 SCHEMATIC OF THE TLU CHARACTERIZATION SET-UP	4
7.1.1 Set-up for Overvoltage TLU Test of a Supply Pin (Supply Test)	4
7.1.2 Set-up for TLU Injection to IO Pin (I Test):	5
7.1.3 Set-up for TLU Injection to Signal Pin (Test of Signaling Latch-up)	6
7.2 TLU PULSE SOURCE	6
7.2.1 General Considerations	6
7.2.2 Recommended Standard Pulses	7
7.2.3 Verification Scheme	9
7.3 POWER SUPPLY	9
7.3.1 General Considerations	9
7.3.2 Power Supply Verification Scheme.....	10
7.4 GENERAL TEST EQUIPMENT	11
7.4.1 Oscilloscope.....	11
7.4.2 Current Sensor.....	11
7.4.3 Voltage Probes.....	11
7.4.4 Decoupling Device	11
8.0 TLU CHARACTERIZATION	11
8.1 GENERAL CONSIDERATIONS.....	11
8.2 PRE-CONDITIONING	11
8.3 PRE-STRESS CURRENT CONSUMPTION READ-OUT.....	12
8.4 APPLYING LATCH-UP STRESS.....	12
8.5 DETECTING LATCH-UP	13
8.5.1 Detecting Latch-up at Supply Due to Supply Overstress or IO Injection	13

8.5.2 Detecting Signaling Latch-up at Signal Pins Due to Supply Overstress or Current Injection	13
8.6 POST-STRESS READ-OUT AFTER TLU STRESS	13

ANNEXES

Annex A (Informative) – Bibliography	14
Annex B (Informative) – List of Pins Particularly Susceptible to TLU	15
Annex C (Informative) – Examples for Components for TLU Set-ups	16
Annex D (Informative) – Examples for Components for Power Supply Verification Set-ups.....	17
Annex E (Informative) – Revision History for ANSI/ESD SP5.4.1-2017	20

FIGURES

Figure 1: General TLU Test Flow	3
Figure 2: Basic Set-up for the Overvoltage Test of VDD Supply	5
Figure 3: Basic Set-up for the Current Injection Test to a Signal Pin	6
Figure 4: Pulse Parameters of the TLU Square Pulse	9
Figure 5: Circuit for Testing Power Supply Response.....	10
Figure 6: Simple Experimental TLU Set-up	16
Figure 7: Schematic of Circuit for Characterization of Power Supply Response	17
Figure 8: Drain to Source versus Gate to Source Voltage for the NTTFS4C25N	18
Figure 9: Gate to Source Voltage versus Total Gate Charge for the NTTFS4C25N	19

TABLES

Table 1: Parameters of Standard TLU Square Pulses	8
---	---

ESD Association Standard Practice for Latch-up Sensitivity Testing of CMOS/BiCMOS Integrated Circuits - Transient Latch-up Testing - Device Level

1.0 PURPOSE, SCOPE, AND APPLICATION

1.1 Purpose

This document addresses steps which are required to perform transient latch-up (TLU) characterization under well-defined conditions. It defines pre-conditioning of the device-under-test (DUT), applying the stress pulse, detecting latch-up, and determining failure criteria. Additionally, a procedure to verify the test equipment is described. The test methods enable the user to perform an application specific TLU characterization with reliable and verified test set-ups.

1.2 Scope

This document defines procedures to characterize the latch-up sensitivity of integrated circuits triggered by fast transients.

1.3 Application

This document defines a characterization methodology which is intentionally kept as flexible as possible. This document does not define a qualification standard.

The characterization can be applied to:

- Test structures (for example, process assessment, component verification).
- Distinct pins of products (stand-alone and with “simple” external circuitries).
- I/O pins of systems and subsystems.
- Integrated circuits with or without external circuitry which is typical for the application or required for pre-conditioning the IC. The IC might be mounted on a printed-circuit board (PCB).

In order to perform the TLU test one has to define the pins under test and the testing parameters. This document is intended to be a guideline for the application engineer who defines the test and the test engineer who performs the test according to the definition and prepares a report.

The characterization is application specific. Hence, the focus of this document is on the general methodology and particularly on verification of the methodology.

TLU as defined in this document does not cover changes of functional states, even if those changes would result in a low-impedance path and increased power supply consumption.

2.0 REFERENCED DOCUMENTS

Unless otherwise specified, the latest issue, revision or amendment of the following documents form a part of this standard to the extent specified herein:

ESD ADV1.0, ESD Association Glossary of Terms²

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)²

ANSI/ESD STM5.5.1, For Electrostatic Discharge Sensitivity Testing –Transmission Line Pulse (TLP) – Component Level²

IEC61340-5-1, Electrostatics–Part 5-1: Protection of Electronic Devices from Electrostatic Phenomena–General Requirements³

² EOS/ESD Association, Inc. 7900 Turin Road, Bldg. 3, Rome, NY 13440, Ph: 315-339-6937; www.esda.org

³ IEC – International Electrotechnical Commission, www.iec.ch