

ESD association standard test method

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*for Electrostatic Discharge
Sensitivity Testing –*

*Charged Device Model (CDM)
Component Level*



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ESD Association Standard Test Method
for Electrostatic Discharge
Sensitivity Testing

**Charged Device Model (CDM) -
Component Level**

Approved September 26, 1999
ESD Association



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Foreword

Existing electrostatic discharge (ESD) test models and standards model a charged object approaching a component and discharging through the component. However, with the increasing use of automated component handling systems another potentially destructive discharge mechanism, the Charged Device Model (CDM), becomes increasingly important. In the charged device model the component itself becomes charged - usually by sliding on a surface - and is rapidly discharged by (an ESD event) as it approaches a conductive object.

Accurately quantifying the CDM discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge itself. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the component will vary considerably depending on a large number of factors such as: package type and parasitics. The typical failure mechanism for the CDM model, observed in MOS components, is dielectric damage, although other damage has been noted.

The CDM sensitivity of a given component is very package dependent. The same integrated circuit (IC) chip in a small outline package (SOP) may be more susceptible to CDM damage than it is in a dual-in-line (DIL) package. ICs in thin small outline packages (TSOP), or a pin grid array (PGA) packages usually have the lowest CDM withstand voltage.

Based on results obtained with early CDM testers, which did not necessarily meet the waveforms specified in this standard, components with CDM sensitivities of 500 volts or less proved difficult to handle without damage. Components with CDM sensitivities of 1,500 volts or more did not experience major field problems using proper handling techniques.

This document does not apply to the so-called SDM testers: socketed discharge model. Waveform parameters for the 30 pF verification module should be used for guidance only. They may be subject to change in future revisions of this document.

This Standard Test Method was processed and approved for submittal to the ESD Association Standards Committee and the Association Board of Directors by the Device Testing Working Group, 5.0.

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