

ESD TR17.0-01-15

ESD Association Technical Report

***For ESD Process Assessment
Methodologies in Electronic Production
Lines – Best Practices Used in Industry***

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Process Assessment
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FOREWORD

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ESD ASSOCIATION TECHNICAL REPORT FOR ESD PROCESS ASSESSMENT METHODOLOGIES IN ELECTRONIC PRODUCTION LINES – BEST PRACTICES USED IN INDUSTRY

1.0 INTRODUCTION

For more than two decades, the robustness of integrated circuits (ICs) against electrostatic discharges (ESD) has been defined by two values, 2,000 volts human body model (HBM) robustness and 500 volts charged device model (CDM) robustness. It has been assumed that both of these robustness levels would provide a safe margin for handling of ICs during processing, assembly, and testing. Both values are “historic” values and have been commonly accepted, with some exceptions towards higher values for specific applications.

Rapid technology scaling and increasing demands for high-speed interfaces with very low pin capacitance are making it challenging to achieve the historic ESD target levels. It is not clear whether the historic target levels are justified by “real” ESD threats in electronic production and testing facilities. Depending on the ESD control, the target levels could be too high, resulting in over-engineering or performance constraints and, consequently, adding additional costs. It could be argued that with well-implemented static control process according to international standards such as ANSI/ESD S20.20 [1] or IEC 61340-5-1 [2], a HBM robustness of 2,000 volts exceeds the maximum possible charging of personnel by more than one order of magnitude and, therefore, the HBM robustness could be reduced. Additionally, in many cases during processing, assembly and testing, charging of devices could not be avoided and in many processes 500 volts charging can be exceeded easily – questioning whether a CDM robustness of 500 volts will really guarantee safe handling.

Considering today’s commonly practiced ESD control measures and the ESD design constraints, the Industry Council on ESD Targets suggests a reduction of the HBM robustness target from 2,000 volts to 1,000 volts [3] and a reduction of the CDM robustness target from 500 volts to 250 volts [4]. It is clear that future technology nodes and high-speed applications will demand further reduction of HBM and CDM robustness.

With decreasing ESD robustness of ICs, ESD control measures during handling of ICs are becoming increasingly important and detailed process assessments will be required. In many process steps, the basic principles of ESD control measures can be assessed easily. For example, the process steps in which devices are handled manually require grounded personnel; the grounding can be verified by ESD testers combined with an access control. However, in automated tools the assessment of charging and possible discharge paths can be a difficult task.

Today, there are no standards that define the steps that are required to assess a process (step) or to finally answer the question about whether an IC with known ESD robustness can be handled safely. The ESDA working group 17.0 started to work on a “standard” document which defines the required steps. As a first step, the working group (WG) decided to compile the recent publications of the members of the WG in one technical report (TR). The goal of the TR is to give the reader examples of “best practices” of process assessment methodologies and test methods. These papers (or portions of papers) were considered state of the art at the time of publication. They have been included in this document with minimal changes. While various specifics may have changed in the intervening years, the approaches to the assessment of risk and risk mitigation remain relevant.

After a short introduction in Section 2.0 on ESD threats, models, and real-life scenarios, four different approaches of process assessments are described in Section 3.0. Those examples cover a broad range of possible threats in process steps and cite examples of appropriate measurement methodologies. Section 4.0 summarizes test methods and the work in the standardization bodies. A summary including possible flow charts for process assessments and measurement methodologies and an outlook to the next steps within the ESDA standardization WG conclude the TR.

2.0 THREATS, MODELS, REAL-LIFE SCENARIOS

2.1 Threats in Electronic Production Lines

ESD threats in electronics manufacturing can be classified into three major categories:

- charged personnel,
- charged (floating) metal, and
- charged device/boards.

This categorization is useful in that each category implies a set of ESD controls to be applied in the workplace. ESD threats from personnel are minimized by grounding personnel through the use of wrist straps and/or footwear/flooring systems. Discharges from metal objects are avoided by assuring that all metal parts that might contact devices are adequately and reliably grounded. The occurrence of ESD from devices or boards is minimized by a) preventing charge (low-charging materials, ionization) or by providing low-current “soft landings” using static dissipative materials [5, 6, 7].

If these strategies could be applied flawlessly, there would be no events in production. However, since they are not perfectly deployed, the overall threat of ESD failure remains and the risk ultimately depends on how well the controls are maintained. This in turn is only known through measurements and other observations of the ESD control process. Conceptually the “suitability” of a process is also dependent on the relative sensitivity of the products being handled. For example, the attention to detail required to maintain high-yield production of very sensitive MR heads is different from that required for, say, older technology integrated circuits. In some as yet undefined way the MR control program is “more capable” than the IC program. Both can produce at high yield because of the difference in the ESD sensitivity of the items being handled.

2.2 Models to Describe the Threats

In principle, one could determine the sensitivity of a device to each individual threat in the line through specific experimentation. This of course is not practical so instead simplified models intended to simulate the most important features of the ESD stresses have been developed. This simplicity means that some details of the real world events will not be included or modeled correctly. The idea is that they are “close enough” to provide useful information about relative device sensitivity while simple enough to use for event modeling and for hardware simulation. These models have in turn been implemented as “standard test methods”. In these methods stress simulation hardware is defined so that devices can be stressed in a repeatable way from location to location and from one simulation machine to another. Further compromises are made to create the hardware definition and these make the faithful connection between reality and simulation imperfect. The correlation between the real world threats and these standard test methods are explored in the next section.

The two models and test methods which are recognized widely today are HBM (for simulation of discharges from personnel) and CDM (originally intended for simulation of discharges from charged device, including discharges caused by static induction). In the hardware realization of HBM there are three major departures from the real world stresses. First, the test method requires that the device be grounded during the discharge. This grounding does not always occur in a real world event and this makes the standard somewhat more stressful than reality on average. Second, most testers have significant parasitics that can distort the intended stress. Parasitics vary with the tester and can cause both false passing and false failing due to mechanisms that are not found in real world events. Third, the test method requires that devices be tested using many different stress/ground combinations. For practical reasons these must be done on the same device and can result unrealistic cumulative effects. Over the last decade the second and third departures have been understood and the test methods have been modified to minimize them. The first departure remains intrinsic to the standard method.

The hardware realization of CDM also has some systematic departures from the real world. The primary one is the very high equivalent capacitance of the test set up. This produces a higher discharge current than would be expected in most real world CDM events and thus makes the

CDM withstand thresholds to the measured electrostatic voltages for a given device lower than they might be expected to survive in production.

It was originally hoped that the remaining category of threats (discharges from charged metal) would be covered by a test method called the “machine model” (MM). The conceptual model schematic might have been reasonably expected to do this. However, the test method that emerged was a modification of existing HBM testers and did not do this. It has been shown that the standard MM has effects very similar to the standard HBM. The thresholds correlate within given technologies and the two produce the same failure mechanism and design fixes (see [3] and references therein). Further, the problem with tester parasitics seen in the HBM is worse for MM. Finally, MM does not include the expected fast leading edge transient expected for a metal-discharge. It has been asserted [8] that the CDM covers this part of the charge metal discharge and the slower parts of the discharge are covered by HBM. That is, if a design meets minimum requirements for HBM and CDM it will be reasonably robust to discharges from charge metal objects. Since the understanding of the situation with MM has been evolving over the last several years, the assessment techniques included in this TR will treat the MM data in different ways.

2.3 Real-Life Scenarios – Correlation Between Threats and Models Based on Waveforms

This section is a reproduction (with some modification) of [9]. See Bibliography.

2.3.1 Introduction

In order to guarantee a certain level of robustness against electrostatic discharge in processing, assembly, and manufacturing, all devices (integrated circuits, ICs) have to be tested to several ESD standard qualification tests. Today, almost exclusively, two ESD models are used on device level testing – HBM [10] and CDM [11, 12]. Both models are defined to address typical handling risks.

For any standardized test method (often called simply standard) it is of course very important that the test methodology can address “real world” risks. For ESD standards, the test methods must be able to reproduce potential or real ESD events.

When the standards are used for qualification the target threshold level must also be defined. Over decades, 2,000 volts HBM was widely used as qualification target based on “historical” analysis [3]. Recently, the Industry Council on ESD Target Levels revised this target value [3], based on the analysis of hundreds of products. The enhanced static control methods in common use all over the world justify a reduction of the HBM target level for safe handling to 1,000 volts or even lower. For CDM, the revised target level was proposed to be 250 volts instead of the commonly used 500 volts value [4]. Evidence for establishing a commonly acceptance level for CDM is less clear than it is for HBM. Discussing the test methods and the target values with respect to actual risks in the field, one has basically to answer two questions.

1. Does the model with its rather strict parameter set as defined in the standard document cover the real-world discharge events? This is easy to understand, since even for a very simple model of a real human discharge, a broad variety of parameters could occur, mainly depending on the person which discharges into the device.
2. Can the voltage corresponding to the current defined by a set-up in a test system be correlated to a voltage (charging) which can be measured during any process step? Obviously, an electrostatic voltage measured on an IC in a handler cannot be transformed easily to a voltage in a CDM test system.

In the next two sections we will discuss these questions for HBM and CDM. For both models a brief description of the test model is given, followed by potential risks and fields and examples. Finally the correlation between test model and field events are discussed.

2.3.2 Examples and Discussion: Human Body Model

2.3.2.1 Test Model

HBM is intended to reproduce the discharge of a human being into an IC which is at a different potential than the person. This model addresses handling requirements in an ESD protected area (EPA). The high energy of the discharge pulse can lead to melting of *pn* junctions (see Figure 1). Electrically, such damage typically results in increased pin leakage currents or power consumption. Less frequently, the energy of the pulse can melt small metal lines and reduce pin leakage currents. In modern processes with extremely thin gate oxides, sometimes gate-oxide damages can be observed as a result of a voltage drop caused by the peak current of the HBM pulse.

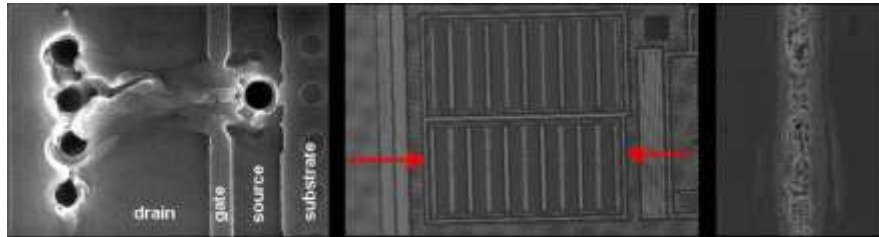


Figure 1: Typical Damages Caused by HBM-Type Stress Observed in Physical Failure Analysis after Lift-off on Silicon Level

Left: Primary ESD Protection Structure after 5.0 Kilovolts HBM Stress

Middle: Damage of Primary ESD Protection Element during Assembly (Detail: Right Picture)

2.3.2.2 HBM Failures in the Field

If you search for systematic ESD failures in the field that can clearly be assigned to bad operator grounding, it is not likely to find respective cases that happened in the last few years. Also if you talk to ESD coordinators of various companies or independent consultants, you hear about a few single failures but not about systematic HBM failures. The main reasons for this situation are the increased quality of the ESD protective elements like wrist straps and footwear/flooring systems that are used everywhere to ground the operators and for the fact that a lot of backup measures for operator grounding are installed; e.g. if the wrist strap system fails the operator at the workbench will become discharged in a controlled way every time he touches the dissipative table mat. Additionally the number of manual processes is decreasing resulting in ESD stresses coming from a charged operator is not as likely.

Nevertheless, there exist fails which on first glance appear to be an HBM failure. A typical example is the second failure image in Figure 1 (middle and right). Electrically, a short from an I/O pin to GND was detected; physical failure analysis (PFA) revealed molten contact holes in the drain area of a primary ESD protection element to GND. The damages occur across the entire width of the device; therefore, the ESD protection element was turned-on uniformly. A comparison with HBM stress on the stand-alone ESD protection device indicates that at least 3 amperes of current are required to cause this damage, corresponding to a 4,500 volts "standard" HBM stress. Although the root cause for that discharge is not yet definitively clarified, detailed process analysis could rule out any HBM event by operators.

2.3.2.3 Correlation Between Field and Test

In the test standard a *current* waveform is defined that correlates with a certain voltage in the tester. In the field we can easily measure the charging *voltage* of an operator, e.g. by using the walking test as described in IEC 61340-4-5 [13] or ANSI/ESD STM97.2 [14].

The related discharge current waveform is not measured, or at least not on a regular basis; it depends strongly on the test method, the operator, and the environment he is in. Of course, the discharge current can vary.

The dependence of the discharge current on the speed the finger of the operator approaching the target is shown in Figure 2. For simplicity, a charged operator discharges into a 4 GHz Pellegrini target [15], which of course is only an approximation of the real situation of a discharge into an integrated circuit. Obviously, none of the displayed waveforms has significant similarity with the waveform recorded in a HBM qualification test system Thermo MK-4. Depending on the speed of approach, there might be an initial current spike with a rise time of far less than 1 ns, and even without initial current spike the rise time is significantly shorter compared to the HBM test system. The “real life” waveform has a faster waveform than the one in the tester and is therefore faster in turning on the on-chip ESD protection. The HBM qualification standard models a discharge capacitance of 100 pF and a serial resistance of 1.5 kilo-ohms, while a numerical analysis of the personnel’s “real life” discharge currents of Figure 2 gives a wide variety of resistances of 1 to 3 kilo-ohms that is well in the range of the model, but with a significantly lower capacitance of less than 10 pF. The model parameters do not change significantly for different operators and even in case of modifying the capacitance of the operator artificially by increasing the spacing of the body to earth (see [9]).

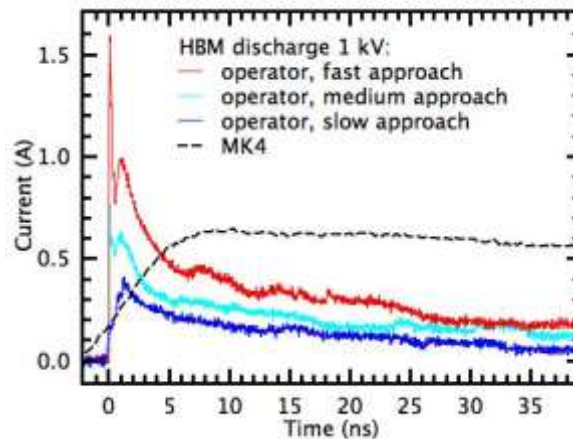


Figure 2: Current of a Discharge of Personnel into a Pellegrini Target ($V_{HBM} = 1,060$ Volts), Depending on the Speed of Approach

NOTE: The discharge current generated by a Thermo MK-4 HBM tester is shown for comparison.

The results show that the energy of a discharge of personnel is considerably lower compared to the energy of a HBM discharge of an HBM test system with the same pre-charge voltage. The peak current is typically in the same range of a personnel's and a HBM tester's discharge. Additionally, there are many tester artifacts in most of the commercially available testers that may result in failures at lower voltages than the device would fail at in the field. Hence, in general the HBM stress during qualification testing is much higher than in the field.

The next question to answer is what a realistic worst-case discharge voltage during manufacturing or assembly could be. Following ESD control standards ANSI/ESDA S20.20 [1] or IEC 61340-5-1 [2], in an electrostatic protected area (EPA), static voltages for personnel are below 100 volts. In a simple walking test experiment the maximum voltage that could be generated by heavy movement with proper ESD footwear-floor grounding was below 80 volts at a relative humidity RH of approximately 30% (see Figure 3).

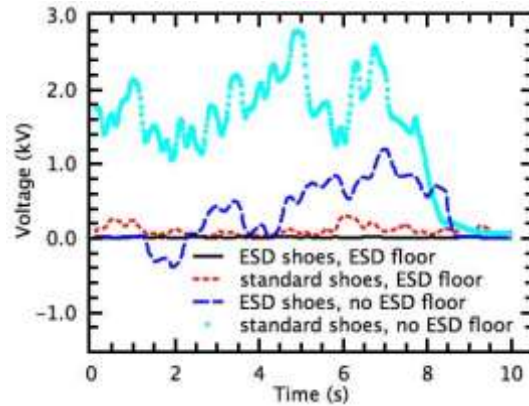


Figure 3: Static Voltages Generated by Walking Test (Heavy Movement) using Different Combinations of ESD Measures (Footwear/Floor)

NOTE: The static voltage has been recorded by a Trek 347 with standard probe and a Tektronix scope TDS 7104 (1 GHz band width).

Even in the case where the operator wears non-ESD appropriate shoes with a total resistance-to-ground of $RTG \approx 3$ gigaohm, on ESD floors under very heavy movement which is rather unrealistic in a manufacturing line, the measured static voltage in our experiments was less than 300 volts. Only in the case that grounding by flooring is not available at all and no wrist-straps are used, can higher static voltages be generated. Without ESD floor, but with ESD shoes, static voltages of 1,200 volts have been measured ($RH \approx 30\%$), with a rapid decay within some tens of milliseconds if movement stops or the operator steps on an ESD floor (in our experiment this step-down is after approximately 8.5 seconds). A discharge into a grounded device with a static voltage generated by such an experiment seems to be very unrealistic, and can certainly be easily avoided in an EPA. Only outside an EPA can higher voltages be generated. Under our experimental conditions we could achieve almost 3,000 volts. However, even this voltage would result in lower discharge energy into a grounded device than a HBM discharge of 1,000 volts in an HBM qualification tester.

Does this mean there is no correlation at all between the results we get during qualification testing and the stress in the field? Even if it is very difficult or sometimes even impossible to compare the voltage values from both sides we know by recent experience that when the charging of the operator is controlled to less than 100 volts in a factory we easily can handle devices with an HBM robustness of $V_{HBM} > 100$ volts without any problems. As HBM addresses in general energy-related fails, the model can be used to reproduce a large variety of fails (see our example), but certainly the exact model and the discharge voltage will not correlate.

2.3.3 Examples and Discussion: Charged Device Model

2.3.3.1 Test Model

In contrast to HBM and MM, in CDM the IC itself is charged and discharges when coming into close contact to a metal plane. The discharge current depends significantly on the package (size and thickness) of the IC. Typically, CDM results in gate oxide or isolation breakdowns due to the voltage drop caused by the high CDM peak currents. Electrically, such damages result often in increased current consumption and functional failures.

2.3.3.2 CDM Failures in the Field

If you search the literature for CDM failures, you will find several case studies. Very often the devices do not fail on the most CDM sensitive pins, but on pins that see the highest stress due to the process design [4]. To accomplish an analysis to find the root cause for CDM-like failures it is

on one side necessary to measure the charging of the devices and on the other side it is necessary to look carefully for any discharge possibility in the process (see examples in Sections 3.1 to 3.5). For the latter, ESD event detectors might be used, but since their accuracy is still in question and since we want to look for a correlation between the voltages during testing and in the field, ESD event detectors are not addressed here.

To measure the voltage of a device either a non-contact electrostatic voltmeter or a contact based voltmeter with high input impedance can be used. Both types of equipment have their advantages and disadvantages for each application. The voltage reading is of course dependent on the capacitance of the device or board with respect to ground.

In [9], a case study is described where a device failed on the pins that have been found during CDM testing to be the most sensitive to fast transients. The device, a chip used for telecommunication, was assembled in a BGA type package with 293 pins. During CDM testing, according JEDEC JESD22-C101 [11], most of the pins passed more than 500 volts, but the high-frequency (HF) pins passed only 250 volts and failed at 300 volts. The physical failure analysis showed exactly the same failure in the field and during CDM testing. During the ramp-up phase when the device was manufactured for the first time a high failure rate between 1 and 30% was found.

During the analysis of the different process steps it turned out that there were high charging values in the fixture used for device testing. The so-called nest (mounted on the plunger that picks up the device from a transport boat in the handler and presses the device into the test socket) was charging the device to greater than 1,000 volts.

The nest was made of insulative material and raised the potential of the device by induction. When the balls of the device made contact to the test socket, a hard discharge into the tester occurred and damaged mainly the HF-balls. Once the material of the nest was changed to a dissipative one (small cost difference), the charging was reduced dramatically and the failure was gone completely.

2.3.3.3 Correlation Between Field and Test

The voltage reading we get in the production lines is of course dependent on the capacitance of the device or board with respect to ground. When a board is running on a conveyor belt with the ground ten or more centimeters away, the voltage reading will be different (higher) compared to when the board is very close to ground or a virtual ground like it is e.g. in an in-circuit tester (ICT) even though the amount of charge remains unchanged. This is simply due to the change in capacitance and this is one of the reasons why the voltage reading obtained in the field is difficult to compare to the voltage that is used during CDM testing where the device is laying directly on a large metal surface (higher capacitance, see Figure 4).

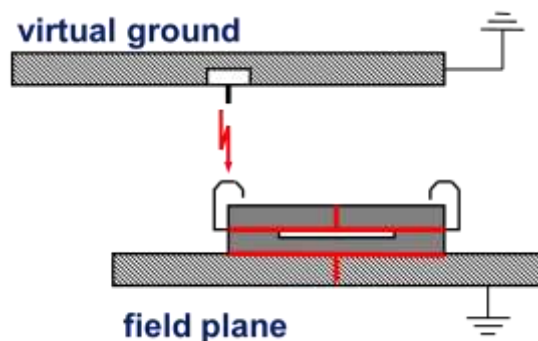


Figure 4: Simplified Schematic of a CDM Tester

Another issue that makes it difficult to compare testing and field directly is the measurement technique itself. For measuring the voltages due to charges in the field, contactless static voltmeters are often used. These meters are excellent tools but it is often difficult or impossible to place the probe close enough to the device in the affected process and the reading is dependent on the distance between the charged object and probe of the meter.

The other type of tool is the contact voltmeter. This meter does not have the problem with the distance, but depending on the process it might not be possible to touch the pins or balls of the device without interrupting the process.

Nevertheless you get valuable information with these tools, with the reading in volts. The value you get from CDM testing is also in volts, but the decisive parameter is the discharge current. And this value is typically not measured in the field.

In order to get a feeling whether discharge currents of "CDM field events" correlate with discharge currents generated by CDM qualification testers, discharge current of charged devices were measured in the field. Three typical situations have been chosen in which CDM fails have already been reported - discharge of a charged silicon wafer where all the devices are still connected to each other; discharge of a device on a molded wafer where the devices are already separated; and discharge of a single assembled (packaged) device in a handler.

For the initial experiments at the wafer level (see Figure 5), the wafer was placed on a charged plate monitor (CPM), and charged to 1,000 volts. The devices are discharged by manually contacting the devices via a JEDEC test head (see Figure 6).

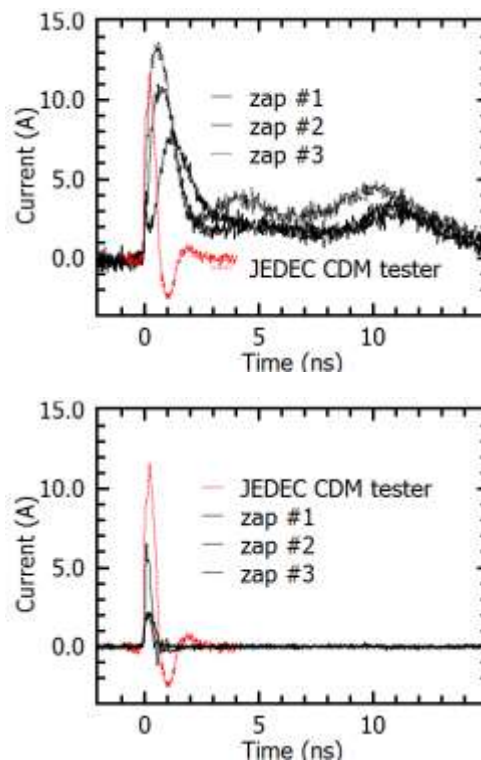


Figure 5: CDM Discharges of a Product Compared to a Typical CDM Discharge Generated by a CDM Tester (JEDEC Head and Field Plate) at a Discharge Voltage of 1 Kilovolt

Top: Product is still embedded in the silicon wafer, thus, all the devices are connected to each other.

Bottom: Product is diced and embedded in a molded wafer, and thus, all devices are separated.



Figure 6: JEDEC CDM Test Head used for Current Measurements in the Field

The waveform was recorded with a Tektronix scope TDS 6154C (15 GHz/40 giga samples per second). Certainly, the manual contact method leads to a comparably large variation of the discharge currents, as the contact point of the discharge pogo pin on the device is more or less arbitrary. The contact is well-known to influence the spark generation and, finally, the discharge current. The discharge waveform of the same device in a qualification tester was measured in a Thermo Orion-2 CDM tester also with JEDEC test head (but with a different type than during the measurements in the field) and the same 15 GHz Tektronix scope TDS 6154C.

The variation, mainly caused by the manual contacting, is about $\pm 50\%$ for both types of wafer. For the devices on the silicon wafer, the peak current is very similar to the peak current of the device in a CDM tester (see Figure 5, top). However, the pulse duration (full width half maximum, FWHM) of the discharge of the device on the silicon wafer is significantly longer (FWHM = 2 ns and a much longer tail) compared to the discharge of a single device in the CDM tester (FWHM = 500 ps). This can be explained by the fact that the charge on the wafer is of course much larger than the charge stored on a single device; the integrated current pulse form gives the total charge. However, as the crucial parameter for the CDM stress which causes the fail is normally the peak current, the CDM qualification test gives a quite reasonable estimation for the discharge of a die on a silicon wafer.

On the wafer with mold compound, the devices are separated and there is no connection via a substrate, hence, there is considerably less charge in the discharge and the FWHM is smaller compared to the discharge of the devices on the silicon wafer (see Figure 5, bottom). Theoretically, the peak current should be the same as in the qualification tester, however, due to the manual discharge methodology the contact of the pogo pin of the JEDEC discharge head to the device on the molded wafer is more or less random and hardly optimized which causes higher resistances and, therefore, a smaller peak current. Theoretically, the discharge current for the same static voltage should be similar to the discharge current in a CDM tester. Therefore, for the same discharge voltage, the CDM tester gives a very good estimation for the discharge of a molded wafer.

For a constant charge, the static voltage depends on the capacitance of the device to ground. The following experiment was performed (see Figure 7). A silicon wafer with an isolating tape on the backside and lying on a grounded metal plane was charged to 1,000 volts. After disconnecting the high-voltage supply, the wafer was raised from the metal plane. The corresponding voltage is 2,500 volts, indicating, that the effective capacitance of the wafer to ground is approximately 2.5 times smaller than at the initial position ($C \times V = Q = \text{const}$). Devices were discharged in both positions by manual contact, using the same equipment as before.

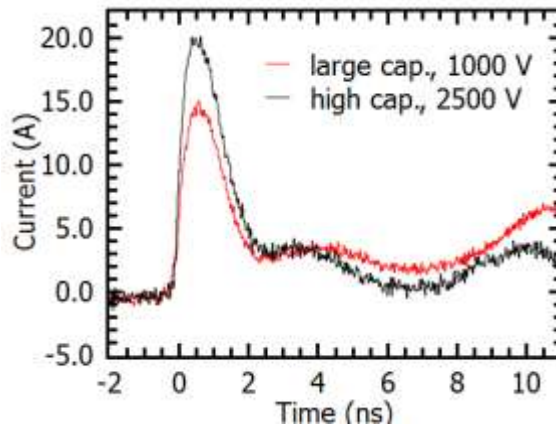


Figure 7: CDM Discharge of Devices on a Silicon Wafer with an Isolating Tape on the Backside

NOTE: For explanation of the experiment see text.

The analysis of the experiment is hindered by the manual discharge as this leads to a huge variation in the curve pulse form. In Figure 7, the average of five discharges is drawn for discharges in both positions. Obviously, the peak current of the discharge of the devices which have a higher voltage (lower capacitance to ground) is higher compared to the discharge of the devices with lower voltage (higher capacitance to ground). This could be expected, however, the difference in peak current should be higher. In first approximation using the simplified model of a discharge of a capacitor through a resistor, the peak currents and the static voltages should be proportional. In order to clarify this discrepancy, further extensive experiments which go beyond this paper are required. It looks as though the different capacitance causes a higher serial resistance in the discharge. Integrating the current waveform shows that the charge stored before the discharge is indeed almost identical. The product RC ($= \tau$) behaves inversely proportional to the measured peak currents, which gives at least a quite consistent picture.

CDM risks exist not only during manufacturing on wafer level, but also during assembling and testing of the devices. Laser marking, “pick & place”, and testing are processes with packaged devices for which charging and CDM-like discharging is a severe risk. For our experiment we have chosen the situation in which a handler (Delta Castle) feeds a test socket. In this handler, the devices are picked by a suction cup from a dissipative plastic tray and placed into a transport boat. This boat transfers the device through the soak line, where they are picked up again by a suction cup and pressed into the test socket which is connected to the functional tester.

For our experiment, the handler and tester have been disconnected and the handler process was stopped just at the moment before the device was released to the test socket (see Figure 8). During the normal process the charging of the devices was pretty low (< 50 volts, measured with both static voltmeter and contact voltmeter) due to the efficient ionizers that were in place. Therefore the device was charged manually by a high-voltage source and discharged by a manual contact of a JEDEC discharge head (see Figure 8). For assembled devices, it was comparably easy to hit a ball.

As expected, the peak current is very similar to the discharge current in a CDM tester. However, the FWHM of the discharge in the handler is significantly larger. This can be explained by the fact that the capacitance of the device in the handler is larger compared to the JEDEC test set-up with an additional dielectric layer between grounding plane and the device. Therefore, for the same voltage, the charge is higher in the handler and consequently also the area under the discharge current waveform which correlates roughly to the width of the CDM current peak (FWHM).

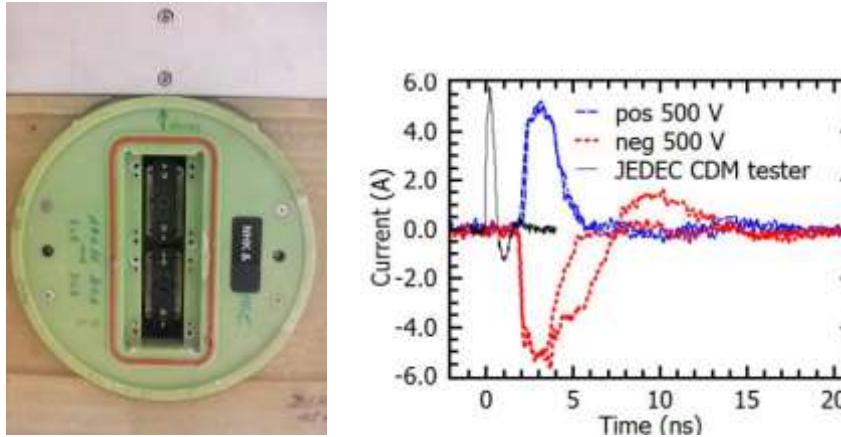


Figure 8: CDM Discharges in a Delta Castle Handler

*Left: Tester side of handler with opening where plunger with rubber suction cup presses device into test socket.
Right: CDM discharges of a product in a handler compared to a typical CDM discharge generated by a CDM tester (JEDEC head) at a discharge voltage of 500 volts.*

Again, it appears that there is no direct correlation between the field and the testing. But it has been shown that CDM addresses the same failure as in the field for certain types of discharges, so CDM is a very important test. There are several examples that pins with reduced CDM robustness (e.g. RF pins) tend to fail with a higher rate than other pins. It is also known by experience, that when the reading on the devices measured in production is below 100 volts devices can be handled with CDM robustness of lower than 100 volts without problems. Because of the capacitance-dependence of the measured voltage, this is only true when the measurement is made in the position where potential events would occur.

2.3.4 Summary

HBM and CDM address different failure modes which might occur during handling and assembly. Therefore, it is necessary to guarantee a certain level of robustness according to HBM and CDM. HBM and CDM qualification procedures define basically a current value. For HBM, the current correlates to a voltage which might be measured also on human beings and roughly lead to similar discharge currents. The energy in the qualification test system is considerably higher so the qualification test can be considered as a worst case stress.

In contrast, the voltage in a CDM tester by no means correlates directly to an electrostatic charging in the field because of the capacitance effect, therefore, the currents at the same voltage level can differ significantly.

2.4 Description of Different Types of Processes in General Terms – Manual, Semi-Automated, Fully Automated

While manufacturing processes take many and varied forms today, the considerations related to electrostatic discharge (ESD) threats can be summarized as the following:

- Manual operations – predominantly human handling activities using hand-held tools and equipment, table top fixtures, manual packing and unpacking.
 - Main threat is from electrostatic charging of people that are handling unprotected ESDS. Another threat is related to CDM where parts become charged by handling, removal from packaging materials. Charge sources within the work area may lead to electric field induction issues resulting in CDM.
 - Activities include assembly operations where ESDS are manually placed on circuit boards or into the next higher level; repair activities where assemblies or subassemblies

are evaluated and parts replaced; and field service operations where ESDS are replaced while equipment is in use within the end-user environment.

- **Semi-Automated Processes** – The consideration here results in risks from both personnel and equipment. The same threats listed above in manual operations apply along with the additional risks from automated equipment. Isolated conductors within the process line add the risk of charged conductors. Grounding and bonding considerations for all parts of the equipment in the process flow for unprotected ESDS are paramount.
- **Fully Automated Processes** – Many of the manufacturing assembly operations for electronic equipment are automated where there is little human interaction except to implement repairs or correct faults that may occur. Electrostatic charging of personnel is still as much an issue as in manual operations since personnel can still cause ESD damage. Electrostatic charging within the equipment is more often of increased importance as are the grounding and bonding requirements to ensure no isolated conductors in the process path. CDM issues also exist at a higher risk level due to high speed processes involving removal of ESDS from packaging materials (tape and reel, trays, tubes etc.).

3.0 RISK ASSESSMENT AND PROCESS CAPABILITIES

In this section, four published documents are summarized which are typical examples of process risk assessment and process capabilities. Those documents are either published at recent EOS/ESD Symposia (Section 3.1, 3.2, 3.4) or by a national ESD standardization committee (Section 3.3). All examples discussed in these documents focus on the methodology of process assessment; the methodologies can be used as “best practices” known today in industry.

3.1 Do We Expect ESD-Failures in an EPA Designed According to International Standards? The Need for a Process Related Risk Analysis

This section is a reproduction (with some modification) of [16]. See Bibliography.

Many people are afraid that they cannot handle sensitive devices. But if the ESD-protective measures in the assembly lines are set up according to international standards like ANSI/ESD S20.20 or IEC 61340-5-1, this shouldn't be a problem. Both standards (in their latest versions) are more or less aligned and give rules for handling of “electrical or electronic parts, assemblies, and equipment susceptible to damage by electrostatic discharges greater than or equal to 100 volts HBM” [1]. Therefore, we do not expect any ESD failures related to HBM, if an ESD program is implemented that follows one of the respective international standards. But HBM-like hazards are only one risk inside an assembly line.

It is also important to take into account that the devices or printed circuit boards (PCBs) become charged and discharge to ground (CDM-like events). The CDM robustness of device is decreasing due to technology trends. The ESDA website (www.esda.org) gives a trend chart for CDM robustness.

What do international standards require to avoid CDM like ESD hazards? They require the removal of non-essential insulators that can charge up quite high and require a strategy on how to handle process relevant insulators.

But the charging alone is not critical and can also not always be avoided. Therefore, a detailed analysis of how devices become charged and how devices discharge has to be performed for every single process step.

3.1.1 Process-Related Risk Analysis

Ideally, an EPA will be designed in a way that there are no highly chargeable materials (insulators) allowed. This is not always possible in modern manufacturing lines since a lot of these insulative materials are required for the process itself.

As an example, consider the wafer saw process in semiconductor manufacturing. This is normally done while the wafer is attached to a highly insulative tape, which can be charged to very high levels. This material is needed for its mechanical properties and for cleanliness. Another example

of a necessary insulator is the device package which is formed from an insulative mold compound.

Insulators are required in the PCB manufacturing process, e.g. the PCB material itself or the plastic housing and the packing materials of the passive components or connectors, which are often made of highly chargeable plastic materials. To cover these competing requirements of highly insulative (and therefore eventually highly charging) materials on one side and ESD-protective production (at reasonable costs) on the other side, it is necessary to analyze every process step to determine whether there is a risk for high charging followed by a damaging discharge.

Very often the ESD program controls only the charging of the environment and improves these points by investing a lot of money while the charging of the assembled object itself is not analyzed. The ESD program controls only the environment to minimize device charging while the charging of the assembled object themselves is not analyzed.

While doing the investigation of charging, it also has to be taken into account whether or not these charging values are dangerous for the object; i.e. it has to be analyzed whether the charged object can contact ground (or another conductive object at a different potential), which is introducing a damaging discharge (CDM-like event) to the charged object. If it can be shown that a damaging discharge cannot take place, the charging of the device, while not ideal, will not create a failure of the device. (Electrostatic problems like attraction of particles by charged objects will not be discussed here.) This results in an analysis of every single process step by asking the following questions:

- Is there a charging of the object in the process?
- Is there a chance for a damaging discharge in this or the next process step?

If there is no charging, there is no possibility for a hard discharge. If there is no hard discharge, there is normally no possibility for ESD damage. This will be explained in some simple examples that can happen in a typical PCB assembly line.

3.1.1.1 Example 1

An uncharged PCB is transported on a conveyor belt from process step A to process step B in a closed tunnel. To be able to look into the tunnel, the cover is transparent; to keep costs low, the cover is made of insulative, highly chargeable Plexiglas. While the (initially neutral) PCB is running underneath the highly charged Plexiglas the electrostatic field of the Plexiglas results in a charge separation on the PCB, but this is not damaging the PCB. If the PCB is coming out of the charged transport tunnel without having seen a metallic contact (or an arc to a nearby piece of metal) the charge separation recombines and a neutral undamaged PCB arrives at the next process step.

NOTE: The use of a grounded, dissipative cover avoids the charging of the cover and therefore avoids the field-induced charge separation on the PCB. This makes the risk analysis much easier but is not absolutely necessary.

3.1.1.2 Example 2

The same initially uncharged PCB is now coming to a process step where it is charged during the process. A possible example is when the barcode label is attached, or when the PCB is held by a stopper while the conveyor belt continues to run and charges up the PCB by rubbing. Such processes can charge up the PCB to several hundred volts. If the metal parts of the PCB (e.g. connectors or metal lines) are not contacted or are not coming close to a grounded conductive object, there is no chance for a damaging discharge (or arc) and the process step can be quoted "no risk" independent of the charging.

Additionally it must be considered what happens to the PCB in the next process steps. If it comes to a process step where it discharges slowly and in a controlled way (e.g. by the temperature at reflow soldering or by the relative humidity while storing in a magazine), then no further measures are necessary.

If the charged PCB is going directly to a process where it is contacted (e.g. at testing), the charges must be drained off before the first contact happens (e.g. by using ionization).

3.1.1.3 Example 3

The same initially uncharged PCB is now coming to a process step where it is charged during the process and contacted immediately afterwards, i.e. a damaging discharge can happen immediately after the charging event. In this case there is a risk for a CDM-like ESD event. A typical example for this is the ICT. The PCB is pressed down by plastic pins made very often of highly chargeable material. This charging is transferred to the PCB by induction. During the electrical measurement the PCB is contacted with metallic Pogo-Pins and a damaging discharge from the PCB into the tester can occur.

NOTE: Very critical during such “closed” process steps is the fact that the problem can be overlooked very easily since the PCB is not charged before and after the process but can nevertheless be damaged during the process.

Table 1 shows possible ESD risks during different process steps in a typical assembly line for PCBs or control units. Of course such a table cannot be complete, since the process steps can vary from assembly line to assembly line. The processes can be very specific, especially during electrical testing.

Some of the control units will be delivered as PCBs, which are put into a (bigger) housing at the customer site (e.g. PCBs for main frame computers). Other PCBs are pressed into a plastic (charging!) or metal housing immediately before electrical testing.

Depending on the process and the charging/discharging situation, the ESD risk can vary. Table 1 gives an overview of the risk during standard process steps and shows additionally how to perform a process-related risk analysis.

How to use the table is explained using the second process step labeled “placement of ESDS” onto the PCB (ESDS = ESD sensitive device). Two different ESD risks can occur:

- i) The PCB can get charged during the process step before and discharges into the ESDS.
- ii) The ESDS gets charged because an ungrounded or insulative pick-up tool (suction cup) is used for picking and placing and the charged ESDS discharges into the PCB. This can especially be risky if a lot of other components are already placed onto the PCB (bigger capacitance). In both cases the charging voltage should be measured using an electrostatic voltmeter.

For case i) the board should be measured, especially if the metal lines on the boards are charged. If the charging voltage is too high it should be reduced, e.g. by using an ionizer.

For case ii), it is best to measure the charging of the device while it is hanging on the suction cup. If that's not possible during assembly, measure the charging of the bare suction cup in a “park” position and the charging of a device needs to be derived from this measurement. If that's also not possible, at least the resistance to ground of the suction cup should be measured. If the charging voltage is too high, the use of a dissipative and grounded suction cup can improve the situation. Additionally an ionizer might be necessary.

NOTE: The use of grounded, dissipative (or conductive) suction cups is recommended wherever possible.

For the rest of the process steps described in Table 1 (and of course also for those not described there) the ESD risk analysis always has to be performed in the same way:

- Check whether there is a high charging of the devices or the PCB.
- Check whether there is a risk for a damaging discharge of the charged device or PCB.

It is the best to do such a process-related risk analysis together with the respective process engineer, since he should be able to explain how the process is really running and he should also be able to run the process in a single step mode (if necessary). This allows doing all the necessary measurements in a “real life” situation.