

ESD TR22.0-01-14

ESD Association Technical Report

ESD TR22.0-01-14

Relevant ESD Foundry Parameters for Seamless ESD Design and Verification Flow

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Glossary

BCD	Bipolar CMOS DMOS (technology)
BEOL	BackEnd Of Line
BJT	Bipolar Junction Transistor
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DRC	Design Rule Check
DRM	Design Rule Manual
DUT	Device under test
EDA	Electronic design automation
ESD	Electrostatic Discharge
GOX	Gate Oxide
HBM	Human Body Model
IC	Integrated Circuit
It1	Trigger current of a snapback device
It2	Second breakdown current
IDM	Integrated Device Manufacturer
LVS	Layout Versus Schematic (check)
IP	Intellectual Property
PDK	Process Design Kit
SoC	System-on-Chip
SCR	Silicon Controlled Rectifier
MIM	Metal Insulator Metal (capacitor)
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MDR	Minimum Design Rule
NVM	Non Volatile Memory
TLP	Transmission Line Pulsing
td	Pulse width
tr	Pulse rise time
Vbd	breakdown voltage
vf-TLP	Very fast Transmission Line Pulsing
VPP	Vertical Parallel Plate (capacitor)
Vhold	Holding voltage of a snapback device
Vt1	Trigger voltage of a snapback device
Vt2	Second breakdown voltage

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1.0 MISSION & SCOPE

In this report the essential requirements on ESD-related technology data will be described which need to be delivered to design customers by a foundry vendor. Design customers can be design houses, IDMs following a foundry strategy or IP vendors. The purpose is to ensure seamless design integration and ESD EDA verification of IC level ESD concepts [1, 2].

Partial information e.g. on HBM robustness of certain ESD structures or even IO cells, is not sufficient to guarantee a successful IC level ESD concept. To adapt ESD structures to performance requirements in mixed signal design blocks and to use pre-designed IP blocks correctly, certain knowledge of the ESD behavior of the technology and devices is needed for the ESD expert integrating the various concepts on IC product level.

It is economically not feasible for foundries to cover all aspects of customer specific ESD solutions and the related parameters. Also these ESD concepts are typically not known to the foundry in an early phase of technology development, when test structures for ESD are defined.

Thus, an adequate set of parameters and their extraction method needs to be aligned between foundry industry and IC design customers. This allows foundries to plan test structures and measurement procedures in the initial phase of the development of a technology. Foundry customers can use this basic set of parameters to make decisions regarding their own ESD design solutions. In total, an alignment on a set of parameters and their extraction methodology is a win-win situation for foundries and foundry customers.

The document will present a generic set of ESD parameters, which is applicable to most types of foundry technologies ranging from CMOS, embedded NVM technologies to high voltage BCD technologies. It will be focused on a functional description of test structures and test procedures with minimum information on implementation details to avoid conflict with the design rules and electrical parameters of the various technologies. This is to provide for the most general application of the recommendations. Consequently, the user of the document will need to 'translate' the described structures and test conditions for the technology under consideration with its specific design rules and device types. However, it is expected that the explanation of the functional purpose of a test structure and test procedure should give enough guidance, both to the ESD device expert of foundry and the ESD design expert of customer, to provide the relevant information.

No target levels will be defined for the same reason. Each technology will need its own range of acceptable parameter values, which will be examined and defined by foundries and their customers. Once the target values have been fixed, regular monitoring is requested to ensure the compliance of the defined parameters with the actual technology capability. Any major modification of the technology has to result in a reevaluation of the parameter set. Beside this, delta checks should be performed in regular intervals to capture any drift effects. It is the responsibility of the foundry to define the time intervals to guarantee a stable set of ESD parameters.

This document is intended to become a guideline for best practice which is consolidated between foundries and foundry customers. It has been drafted by an open working group regularly reporting to industry and collecting feedback for further improvement.

2.0 INTERACTION BETWEEN FOUNDRY - IP & EDA VENDOR - IC DESIGN TEAM

ESD protection concepts require seamless ESD protection paths between any pin combinations on the IC. This has to be guaranteed at the **IC design** level. This requires information and data exchange between foundry supplier, IP vendor, and IC design integration (Figure 2-1, Figure 2-2, and Table 1).

Initial provision of ESD foundry process development kits (PDK) information → involves ❶.

- Enabling check of ESD rules (device layout and usage) by EDA checkers → involves ❸+❹.
- Support of design integration of IP blocks (I/O interfaces, any analog or digital blocks) to top level IC design (especially for complex SoC) by foundries (should support IP vendors ESD design and IP vendors (should support ESD robust IP integration). This also needs to be verified by EDA checkers → involves ❷+❺+❻.

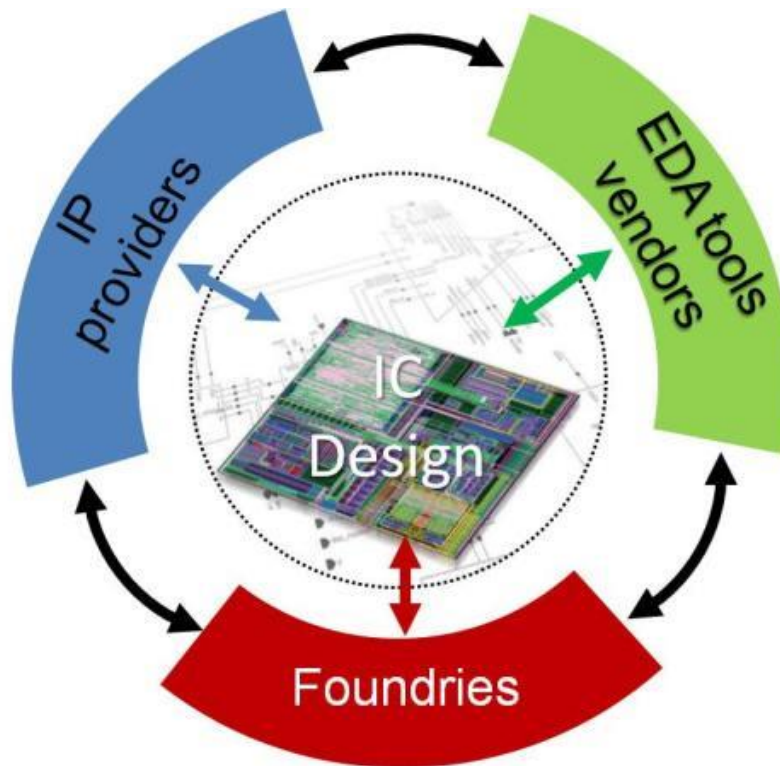


Figure 2-1: Foundry / IP & EDA Vendor / IC Design Interactions for ESD Robust IC Design

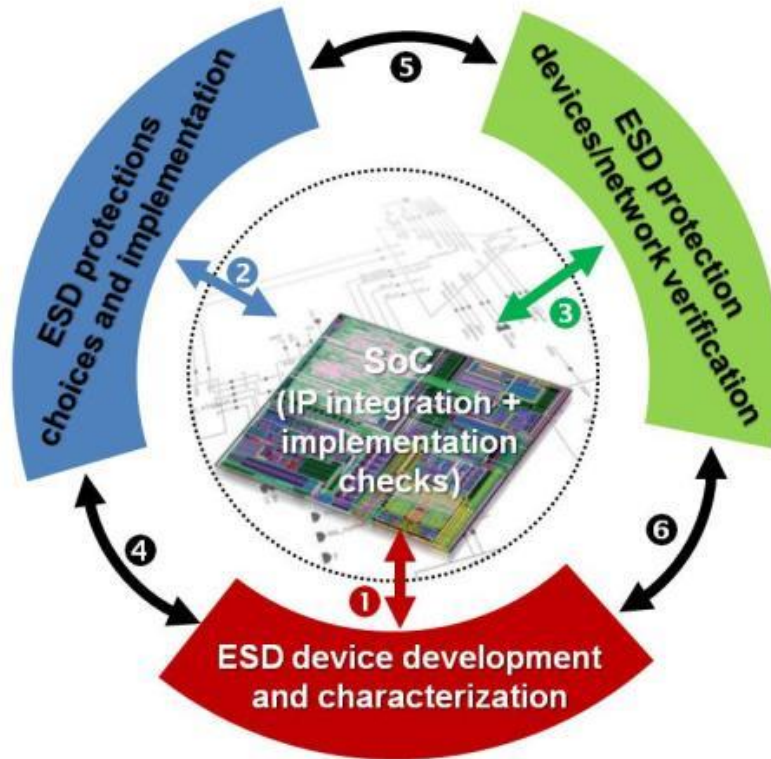


Figure 2-2: Typical Activities and Interactions Required for ESD Robust IC Design between the Various Stakeholders (*foundry / IP & EDA vendor / IC Design*)

Table 1. Proposed Best Practice of the Interaction of Foundry, IP Vendor, and IC Design for IC ESD Protection Design

❶	DRM (including ESD design & layout rules for ESD-DRC or even more advanced checkers) + ESD process data (TLP & vf-TLP devices characterization results)
❷	IP User Guide and application notes, IP integration review on request + ESD technology file (+ ESD EDA views) to enable IP vendor specific ESD rules checks.
❸	Some ESD checkers: Topology & DRC / Network efficiency and victims detection / Current Density & Path Resistor => continuously improved to increase the test coverage, targeting the “pre-silicon ESD qualification”
❹	See ❶
❺	Data & support for IP level ESD checker enablement: I/O ring checker, any ESD specific EDA views or technology files
❻	All ❶ + technology files (interconnects or substrate parasitic)

General assumptions when using ESD protection devices:

In the following sections, several assumptions are made. Fundamentally, any device recommended by the DRM or any ESD document from the foundry must be fully supported in the PDK.

Therefore, the expectations are:

- **ESD device layout is supported** by the foundry, either with a PCell or at least a layout (sample layout or fixed-layout) available in a library.
- **LVS is supported** by the foundry with device symbol/schematic for any ESD device to allow state-of-the-art design flow (no “black boxing” of device for LVS = marking for exclusion of check), even when using layout specificities (i.e. NMOS with drain extension and silicide blocking layer).
- **Electrical models are available** and accurate for all ESD devices under normal operating conditions. Accurate values for leakage current and capacitive load across the full operating range are expected for every allowed layout geometrical variation and device variant of the ESD devices (typical example being the NMOS with silicide blocked drain extension, with major influence on the drain junction capacitance, source/drain resistance R_{ds} and other secondary effects). ESD conduction mode cannot be expected to be covered by electrical models.

NOTE: Both LVS and electrical models support may not be available in the general technology package for very specific ESD device (i.e. like for SCR devices) by default. This needs to be resolved commonly by foundry ESD team and ESD design engineer in order to be finally supported within the PDK. However, this has to be understood as an exception and definitely delays the turn-around time for a first design.

3.0 TESTING METHODOLOGY

Even though the testing procedures used to extract the ESD parameters might vary significantly depending on the specific device type, a basic description of the DC measurements (voltage or current ramp methods, current force method) as well as transmission line pulsing (TLP) tests used for device characterization purposes is provided in this section.

Any aspect that may differ or have to be considered in addition to the general test descriptions will be specifically addressed in each device related Section 4.0.

3.1 DC Measurements

Four different DC measurement methods are described in the section:

- 1) Voltage Ramp Method
- 2) Current Ramp Method
- 3) Voltage Force method
- 4) Current Force Method

3.1.1 Pre-Conditioning Before all Measurements

Due to consecutive measurements some charge can remain in the silicon. This can lead to an erroneous measurement result. Therefore, all test pins should be grounded before test.

Procedure

Apply 0 volts through a resistance of 10 kilohms or higher to all pins under test for at least 1 ms.

3.1.2 Voltage Ramp Method (V-Ramp)

In case of voltage ramp method the voltage drop across the device under test is increased by a certain step size (e.g. 100 millivolts) starting either at 0 volts or at an appropriate voltage reasonably below the voltage range of interest. At each voltage step the related current is

measured. The measurement is stopped either as the final voltage is reached, or when the measured current exceeds the defined compliance value.

Procedure

- a. Preconditioning procedure (see above)
- b. Apply VOLTAGE = 0 volts (or appropriate voltage)
- c. Measure CURRENT
- d. If CURRENT < CURRENT compliance, increase VOLTAGE by 100 millivolts.
- e. Otherwise stop

3.1.3 Current Ramp Method (I-Ramp)

In case of current ramp method the DC current flowing through the device under test is increased by a certain step size (e.g. 10 μ A) starting at 0 amperes.

At each current step the correspondent voltage drop is measured.

The measurement is stopped either as the final current is reached, or when the measured voltage exceeds the defined compliance value.

Procedure

- a. Define the final CURRENT
- b. Preconditioning procedure (see above)
- c. Apply CURRENT = 0 amperes
- d. Measure VOLTAGE
- e. If (VOLTAGE < VOLTAGE compliance & CURRENT < final CURRENT), increase CURRENT by 10 μ A
- f. Otherwise stop

3.1.4 Voltage Force Method (Voltage Spot Measurement)

In the voltage force method a predefined voltage is applied and the resulting current is measured.

Procedure

- a. Preconditioning procedure (see above)
- b. Apply VOLTAGE = VDDMAX (blocking device) as specified by design manual or ~ 0.5 volt (conducting device)
- c. Measure CURRENT

3.1.5 Current Force Method (Current Spot Measurement)

In the current force method a predefined current is applied (e.g. 10 μ A) and the resulting voltage is measured.

Procedure

- a. Preconditioning Procedure (see above)
- b. Apply CURRENT = 10 μ A
- c. Measure VOLTAGE

3.2 TLP Measurements

Transmission line pulse (TLP) measurements with defined pulse duration (t_d) and rise time (t_r) are used in order to extract the device specific parameters in the ESD pulse time domain. For measurement setup and calibration please refer to test methods of TLP [3] and vf-TLP [4].

Generally TLP tests with $t_d=100\text{ns}$ and $t_r = 10\text{ ns}$ are applied, which correlates with HBM in terms of energy. In specific TLP waveform measurements, which investigate the turn-on behavior of DUTs a faster rise time of 100 ps is recommended. This can also be realized in a vf-TLP tester.

A 4-point Kelvin measurement setup is recommended, especially for conducting devices showing low-voltage IV characteristics (e.g. forward diodes), in order to optimize the voltage sensing accuracy. TLP pulses are applied between the test structure pads, while the transient current flowing through the DUT is measured by means of a current probe embedded in the 50-ohm line. In a Kelvin setup the transient voltage drop across the DUT is monitored at the same pads by means of dedicated high-ohmic probes. Alternatively, a voltage sensing line has to be connected to the 50-ohm pulse line by means of a high-ohmic (e.g. 5 kilohm) pickoff tee.

Increasing TLP pulse levels with an appropriate step size are applied up to the device failure detection.

The quasi-static IV curve is obtained by averaging the measured TLP current and voltage values at each step in a time window close to the falling edge of the pulse (e.g. between 70 ns and 90 ns if 100 ns TLP pulses are applied), in order to eliminate the impact of voltage overshoots in the first several tens of nanoseconds and to take self-heating effects into account.

At the beginning of the TLP test and after each TLP pulse, either DC voltage or current spot measurements are applied across the test structure and the related current or voltage drop is monitored in order to detect any degradation of the DUT in terms of DC electrical parameters (e.g., leakage current or breakdown voltage) (see Section 3.1).

The spot voltage must be chosen in a range where no device degradation due to the DC measurements occurs. However, the spot should be set to be as sensitive as possible to device degradation by the pulse (e.g. by detecting current increase in μA regime). For dielectrics it is recommended to define the DC spot voltage at the highest operational voltage specified for the tested device type.

For current spot measurements, the forced DC current level should enable a good voltage resolution without damaging or degrading the device.

3.2.1 Failure Detection and Leakage Criterion

The progression of the DC voltage or current spot values measured after each step of a TLP test is used as an indicator for degradation of the DUT (e.g., leakage current, breakdown voltage). In general, a deviation in the spot measurement sequence exceeding or violating a defined failure criterion corresponds to the detection of the device failure and, thus, enables the extraction of the failure current I_{t2} and voltage V_{t2} .

When characterizing reverse biased junctions or dielectrics, DC voltage spot measurements are applied in order to monitor the leakage current progression. Blocking devices typically show a sudden and significant leakage current increase at the TLP failure level, resulting from a junction melting or a dielectric breakdown.

The failure criterion is therefore defined as the detection of a step discontinuity larger than one order of magnitude in the leakage current progression.

An example of TLP and DC spot measurements in case of a high impedance device is shown in Figure 3.2-1.

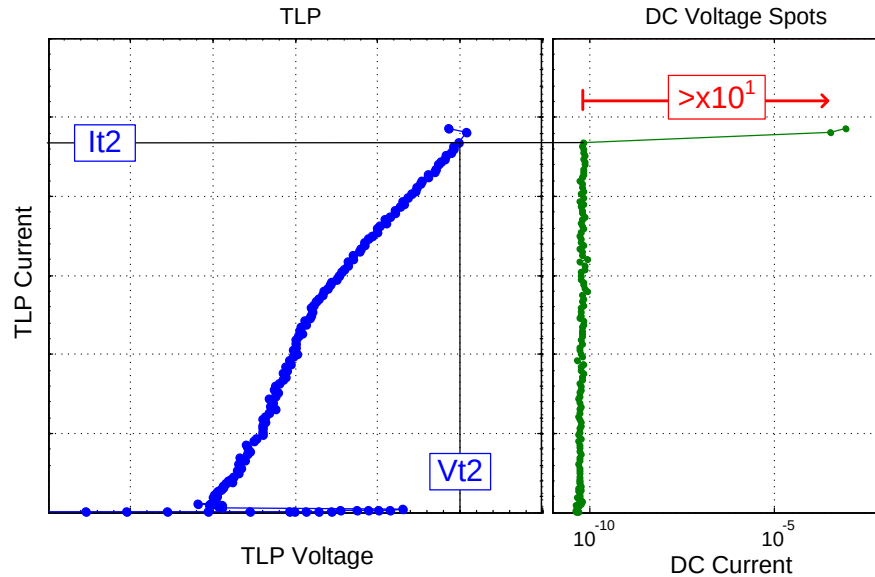


Figure 3.2-1: Failure Detection Methodology for Blocking Devices

However, in some structures a degradation of the leakage value happens gradually with each step increase of the TLP current (Figure 3.2.2 - left). In this case it is recommended to report the lowest TLP current at which either the maximum device leakage value specified in the electrical parameters is exceeded or a significant change of leakage by an order of magnitude for subsequent TLP steps. The degradation characteristic should be monitored and reported.

In some cases a 'recovery' of the leakage value after a massive change of leakage has been seen at even higher TLP currents (Figure 3.2.2 - right). As these outliers might be due to instability in the set-up or temporary change in device behavior, it is recommended to measure at least three TLP current steps above the first detection of leakage increase to validate the change in leakage.

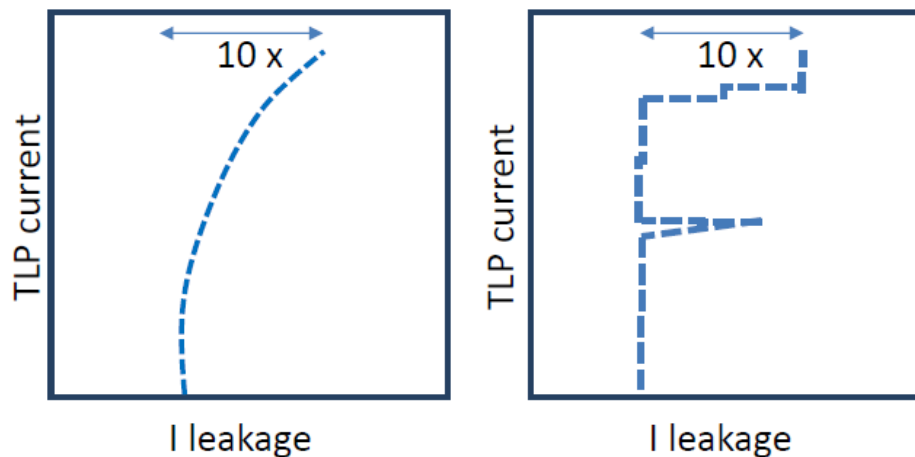


Figure 3.2-2: Spot Measurements of Blocking Devices - Leakage Current Degradation (left) and Occurrence of Leakage Outliers at Lower TLP Levels (right)

3.2.2 Failure Detection of Conducting Devices

TLP tests on conducting devices, such as poly resistors or metal lines, generally show a slight and progressive degradation of the monitored DC voltage or current starting from a specific TLP pulse amplitude.

For such a device type the definition of a failure criterion based on point-to-point (relative) variations of the DC spot measurement progression is recommended to efficiently capture the degradation of the DUT in its early stage (Figure 3.2-3).

- The failure criterion based on a 10% relative deviation of the monitored DC voltage is described in the example below: extract the minimum (V_{min}) and maximum (V_{max}) DC voltage values when forcing current for the first 10 steps of the TLP test (it is assumed that the step size is sufficiently small so that no degradation occurs in the first 10 measurement steps). Other criteria using higher relative deviation might be applied depending on the technology and device type. Degradation due to multi-zaps can be avoided by using single zaps at higher level.
- V_{min} and V_{max} set the limits of the band in which the variation of the DC voltage measurements is rated as “normal”, or caused by measurement noise.
- A failure is detected at the first current spot measurement, where the voltage consistently drops below $0.9 V_{min}$ or exceeds $1.1 V_{max}$.

The graphical representation of the failure detection procedure for conducting devices is shown in Figure 3.2-3.

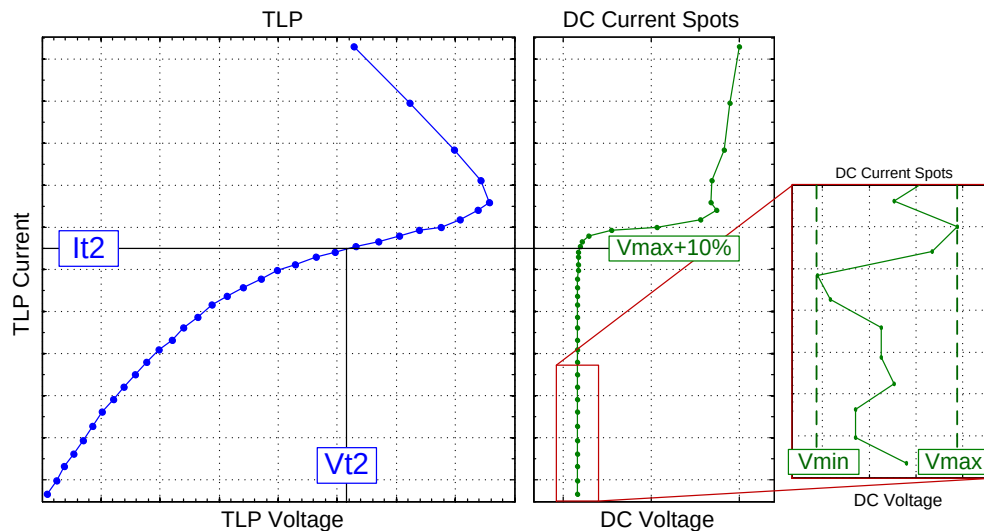


Figure 3.2-3: Failure Detection Methodology for Conducting Devices

In specific cases more stringent or relaxed DC spot limits defining the failure criterion might be chosen.

Together with the extracted I_{t2} and V_{t2} parameters the complete TLP IV curve and DC current or voltage measurements progression should be provided.

3.2.3 ESD Parameter Extraction

Figure 3.2-4 shows the IV TLP characteristic of a snapback device with the related monitored leakage current progression. The extracted ESD parameters are briefly discussed.

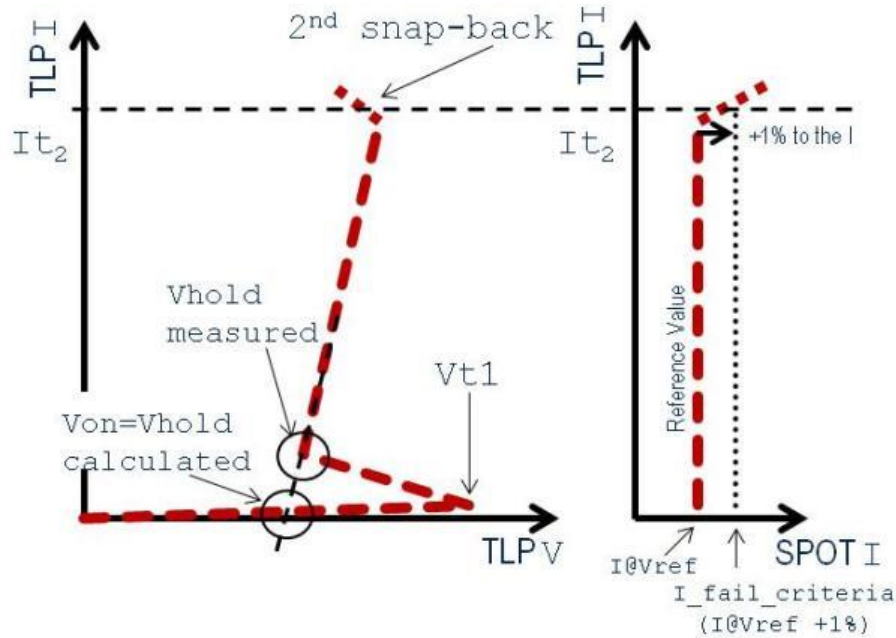


Figure 3.2-4: TLP Measurement Example

- V_{t1} , I_{t1} : Trigger point – The voltage/current at which bipolar action starts in a snapback device. Depending on the technology and device type V_{t1} can be strongly dependent on the rise time of the TLP pulse. For a comprehensive characterization TLP pulses with a rise time of $t_r = 100$ ps, 1 ns, and 10 ns ranges should be applied.
- V_{on} : Turn-on voltage – The point at which the linear fit through the TLP I-V curve crosses the voltage axis.
- V_{hold} , I_{hold} : Holding point – The voltage at the apparent lowest current after snapback. This point depends on the DUT and the source impedance of the measurement setup.

The detection of V_{hold} depends on the load line resistivity (typically 50 ohm) and the lowest current in the holding voltage regime measured by the 50 ohm system is $I_{hold} = (2 * V_{incid} - V_{hold}) / 50$ ohm, where V_{incid} is the voltage pulse voltage going to the DUT.

V_{on} and V_{hold} , are very important in case of maximum operating conditions where you are not allowed to exceed these voltages.

Multi-finger structures or multi bipolar structures can exhibit snap-back type behavior at multiple current levels. In this case the TLP curve does not look as smooth as seen in Figure 3.2-4. The snapback at lowest currents is considered for extraction of V_{hold} and V_{on} . The TLP test procedure is described in Figure 3.2-5.

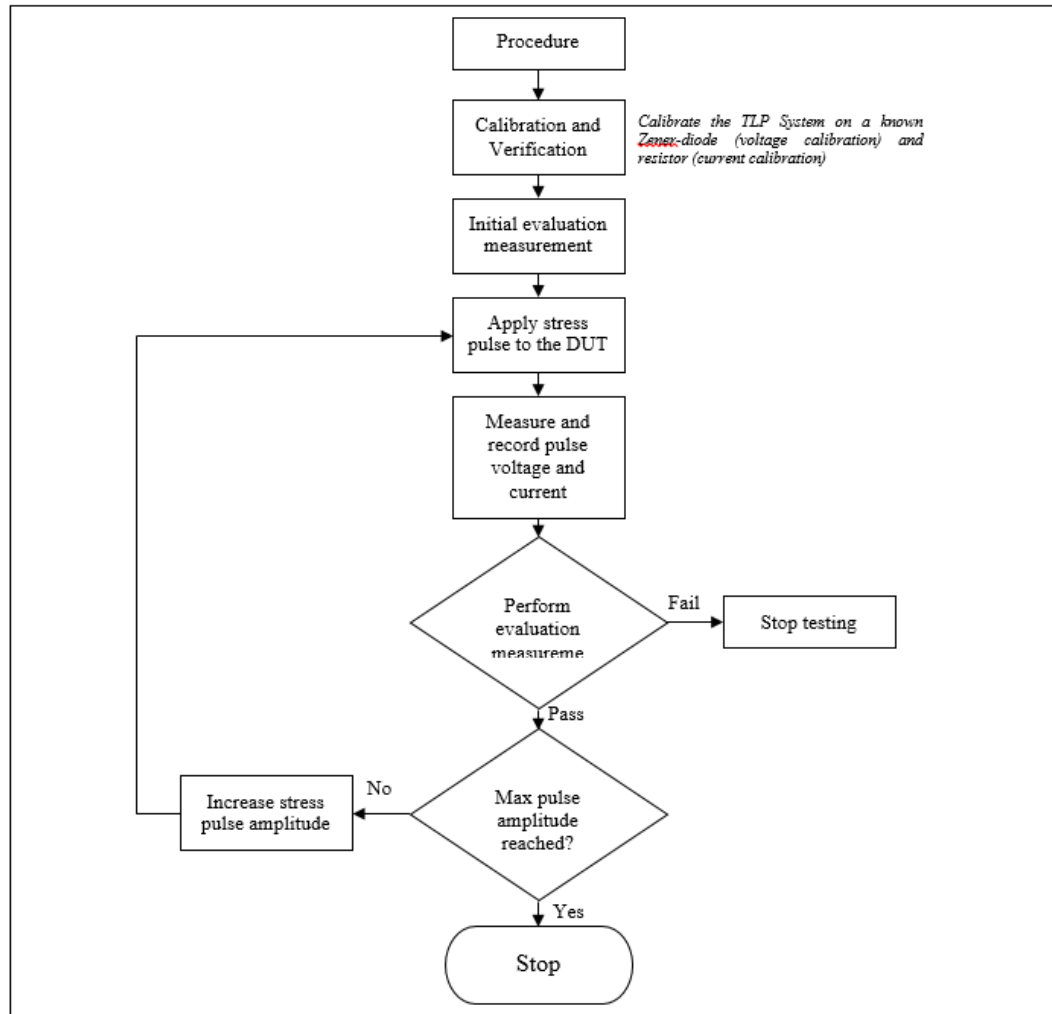


Figure 3.2-5: TLP Test Procedure

4.0 RELEVANT ESD PARAMETERS

The description of ESD parameters is focused on purpose, type of extraction structure, test condition and format for data reporting. Restrictions of disclosing technology information and effort invested by foundries as well as providing meaningful data to the design customer are taken into account.

Apart from the mentioned constraints for delivering data, there is a technical challenge to provide a generic description of test structures and test methods which applies to all kinds of technologies varying from very advanced CMOS to high voltage BCD technology. In many cases the final decision on the details of an extraction structure has to be done by the ESD expert at the foundry. This limits the direct comparison of parameters between technology families. However, within a technology family, like advanced CMOS, a trend of parameters can be assessed. Thus, it provides guidance when going from node to node within a technology family and, when benchmarking different foundry suppliers for the same technology node.

It should be emphasized that under any circumstances the exact testing conditions, both dc and TLP, and the essential design parameters should be reported by the foundry ESD expert.

In the following the relevant ESD parameters are discussed grouped into various device types, dielectrics and interconnects.

4.1 Dielectrics

4.1.1 Overview of Parameters

As dielectrics are not able to withstand any relevant breakdown current, the purpose of the characterization of dielectrics is to find the minimum critical breakdown voltage under short pulse stress. There is a dependence of this value on the pulse duration [5]. For practical terms the focus is on 100 ns stress pulses using standard TLP. In addition, vf-TLP can be applied to accomplish the set of parameters especially for thin gate oxides. The dielectrics of interest are:

- thinGOX
- thickGOX
- BEOL dielectric
- Dielectrics of Metal-Insulator-Metal (MIM) caps
- Dielectrics of Vertical Parallel Plate (VPP) caps

In high voltage technologies even more types of gate oxide stacks might be in use, which add to the list above. The analysis of BEOL dielectrics could lead to a complex analysis of various Mx-Mx and My-Mx topologies including various sets of minimum distance rules depending on the voltage class of wired nets. To simplify the data set only a minimum breakdown voltage of a complete stack of any metal combination using minimum design rules is required. Different values might be extracted for high voltage minimum distance rules.

4.1.2 Reference Test Structures

Different types of dielectrics differ in their test structures. The gate oxide test structures split into 3 subtypes as shown in Figure 4.1-1.

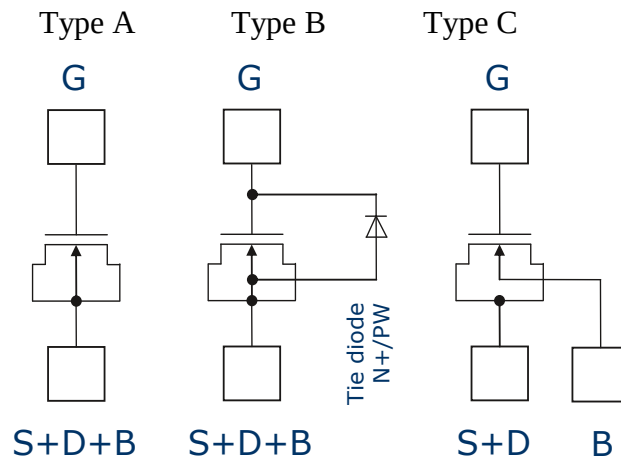


Figure 4.1-1: Schematics of Gate Dielectric Test Structures (B: body, S/D: source/drain, G: gate)

Type A allows the extraction of the minimum breakdown voltage for both stress polarities. However, this configuration might be harmed by plasma charging. Thus, to detect any influence from this, type B allows a delta assessment for positive stress on gate up to the tie diode breakdown. Finally type C allows one to distinguish between breakdown to source/drain and bulk. The larger headroom for gate to bulk breakdown voltage helps e.g. for stacked transistor topologies. A generic layout topology of a unit cell for gate oxide device stress test is shown in Figure 4.1-2.