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ESD Association Technical Report

***For Electrostatic Discharge
Sensitivity Testing –***

Charged Board Event (CBE)

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FOREWORD

In early 2009 an increased number of inquiries were received about a certain type of unexplained "component-on-board" failures that resembled ESD at times and EOS at other times. However, these failures could not be duplicated by using any of the existing ESD Models. Further research indicated that these problems were related to the so-called Charged Board Event (CBE), an ESD phenomenon pertaining to the charging up of the boards and creating stress on the components or ICs mounted on them. CBE type of ESD events have been recognized already since 1983, but there is still not commonly agreed methods to classify or analyze CBE cases. Purpose of this Technical Report is to clarify the CBE phenomena, present failure cases where CBE has been the main ESD stress scenario, and collect the existing knowledge for further development of ESD protection methods.

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ESD Association Technical Report for the Protection of Electrostatic Discharge Susceptible Items – Charged Board Event (CBE)**1.0 INTRODUCTION**

In reviewing existing publications, such as ESDA White Paper 2 by Olney and Henry [1] as well as publications by Frank [2], McFarland [3], and Thompson [4], it was found that only anecdotal evidence existed up to 1983 for ESD failures of integrated circuits (ICs) mounted on printed circuit boards (PCBs). These failures had occurred after improperly grounded personnel handled the IC-populated PCBs during the many stages of manufacturing up to and including actual placement in the completed electronic equipment/system. Between 1984 [4] and 1987 [5], it was reported that most components which reportedly failed for the ESD transients on the printed circuit board (PCB), had failed functional testing (that is, the board was inoperable when originally built). Failure analysis (FA), which included de-processing, delayering, and scanning electron microscope (SEM) analysis, of the ICs removed from the PCB, showed that a physical damage showing dielectric or silicon punch-through.

As of 1986, this PCB-related electrostatic discharge (ESD) event was referred to as a “charged board model” (CBM) by Enoch and Shaw [6], and CBM ESD testing was initiated. The measured PCB capacitance (>125 pF) was always much larger than that of the typical 25 pF for the IC devices being built at that time. In 1986, Enoch and Shaw [8], in their study of board-mounted ICs, used the field induced charged device model (CDM) method to charge the board (PCB), then grounded the PCB via one of the input connectors. Koyler et al [5] in 1987 regarded the PCB to be an extended device package but with a much higher capacitance. They suggested two modes by which the board-mounted IC can fail: (i) during the insertion of the device into the board, and (ii) when the PCB discharges into the device, an external to internal mechanism. In 2003 Paasi [9] found board mounted IC failures after they were charged by transportation on conveyor belts. Also in 2003, Olney et al [10] used a standard CDM tester to perform the field-induced stress testing of the components on the PCBs. They modified the boards to fit on the tester table.

Conceptually, the CBM is similar to CDM. During a CDM event, the charge stored by a packaged IC discharges (typically < 100 ps rise time) just before contact is made with a conductive object at or near ground potential. During a CBM event, the charge stored by an entire PCB discharges (similarly, about 100 ps rise time) just before contact is made with a conductive object at or near ground potential. Thus, the named CBM can be thought of as an extension of CDM where the PCB is the “device” that stores the charge. It is suggested that CBM be renamed charged board event (CBE) because CBE does not actually represent a new model, it is just a more severe CDM event. So severe in fact, that the failure can be mistaken for electrical overstress (EOS) damage in some cases. The FA pictures of these CBE failures can be found in later sections as well as in the literature referenced throughout this report.

A usable document that the industry can rely on is needed. The question is: which industries need this? In the working group, the different industrial segments that have been discussed include the PCB, the cell phone, the “board stuffing”, the automotive, and the medical industries. CBE is not as well-known as the classic ESD models but it represents a major real-world ESD threat. Even if all the individual components used for a given PCB have high device or component-level ESD robustness, one or more of these components could be very susceptible to ESD damage after mounting to a PCB since a PCB in general has much higher capacitance [11] than an individual device. CBE damage can be much more severe compared to the CDM damage, therefore, before attributing an extremely severe-looking IC failure on a PCB to other root causes of EOS such as powered handling or AC switching issues.

In 2007, Reinvuo et al [7] modeled the CBE pulses to determine the sensitivity of the electrical components on the board. They argued that the main difference between CDM and CBE is the discharge energy through the component. They discussed and used the physical and essential parameters for the CBE simulation using different sizes of boards (length, width, height, and distance between the charged board and the ground plane of the board). They used and discussed the discharge path parameters (length and point of contact). Their simulations included a

capacitance only model, a combined capacitance and inductance model, a 2-D transmission line model, and a 3-D *RLC* electromagnetic model. They compared different peak currents and different resonant frequencies for all the models, and then concluded that ringing must also be considered in addition to peak currents; finally establishing that the capacitance-only model is inadequate to fully simulate the CBE phenomena.

In 2011, Tamminen and Viheriäkoski [12] used a low inductance (100 nH) pogo pin to contact PCBs on a test bench, simulating a high capacitance situation. They obtained capacitance, potential, charge, and energy without measuring the current waveform. They pointed to the huge difference/discrepancy in the data for voltage and capacitance obtained between the bench setup and measurements obtained in the manufacturing area. They reported that the components had high CDM protection, but when placed on the board with no on-board protection, the antenna-related discharge into the components on the board failed the components at a much lower potential.

In summary, while no industry standard currently exists for CBE testing, this technical report (TR) aims to fill the gap of knowledge for its various aspects. A standard practice contains a procedure for performing one or more operations or functions that may or may not yield a test result. However, if a test result is obtained, it may not be reproducible. Trying to standardize the CBE stress testing procedure will be very challenging because PCB designs and layouts vary significantly and each PCB may have several tens to hundreds of potential discharge points. Therefore, specifying precise discharge points in a standardized test method (STM) is not easy. However, a SP, which are just the best practices that are being used, can be developed after a TR is published.

2.0 CHARGED BOARD EVENT AND CHARGED DEVICE MODEL: COMPARISONS AND DIFFERENCES

Conceptually, a CBE has similarities to the CDM event for a packaged component [12], [13], [15], [30]. During a CDM event, the charge stored by a packaged IC discharges in just nanoseconds or picoseconds before physical contact is made with a conductive object. On the other hand, during a CBE the charge stored by an entire PCB with several electronic components or ICs discharges just before a contact is made with another conductive object having a different potential. Thus, a CBE can be thought of as an extension of CDM where the board is the “device” which stores the charge. However, since a PCB can store far more charge (due to a higher capacitance) than a single IC, the peak discharge current and the charge transfer for a CBE is typically much higher, and pulse duration longer compared to a CDM event [29]. Consequently, the damage from CBE can be quite severe and can be easily mistaken to other root causes of EOS damage.

One way to compare CDM and CBE is to compare the basic discharge source parameters. ANSI/JEDEC/ESDA JS-002 [13] CDM standard defines two calibration disks – 6.8 pF (small) and 55 pF (large) – to set the reference current waveforms in a CDM tester. The capacitance of the IC component will typically vary between these two values. The combined probe and air spark resistance is close to 20 ohms and the inductance of the discharge head is typically below 12 nH. In CBE the capacitance of the board varies from about 10 pF to hundreds of picofarads while the inductance ranges from tens to hundreds of nH. Finally the resistance varies from the value of the air spark resistance to kilo ohms depending upon the DUT design and the voltage level. Thereby, the source parameters partially overlap with the large size ICs in a CDM tester and with small size products in a CBE scenario. Likewise the discharge waveform will change when the environment and discharge path *RLC* parameters are varied. The discharge parameters are summarized in Table 1.

Table 1. Typical *RLC* Network Parameters for CDM and CBE Discharges

	<i>R</i> [Ω]	<i>L</i> [nH]	<i>C</i> [pF]
CDM	< 20	< 12	< 55
CBE	20 - 1000	10 - 10000	10 - 1000

In addition to similarities, the CBE has some major differences with the CDM. In the charged board event, the charge is not necessarily stored in the electronic assembly itself, but the discharge can come from another charged conductive object (another electrical or metallic sub-assembly component). In addition, the discharge event can take place between two non-grounded objects with a potential difference. In that case the objects will equalize the potential difference during the discharge event but the system will still have a net charge after the first discharge event. The level of ESD stress depends on the amount of total charge displaced and the capacitive coupling between the objects just before the discharge. In principle, a second discharge event can also take place when the unified charged assembly is grounded. The objects taking part in the event can vary significantly from the perspective of the physical size and the electrical design. Therefore, the discharge waveform can have a greater variation compared to the CDM events and CBE is able to produce adiabatic CDM-like damage with short pulses, and non-adiabatic or EOS-like damage with long pulses as well as a mix of these types of two pulses.

Six typical CBE discharge waveforms with initial 1 kilovolt potential and varying RLC values shown in Table 2 are presented in Figure 1. These waveforms represent the current flow between the DUT and the ground contact and are not necessarily the same current waveforms which will flow through the ICs on the PCB. In Figure 1a) the waveform A has a higher inductance and smaller serial resistance than B. In Figure 1b) the waveform C is a faster discharge than D due to a small source capacitance (the air spark closes after 42 ns in D). The waveform C is also similar to a CDM event. In Figure 1c) the waveform E has two parallel RLC components producing both a high frequency and a low frequency oscillation. The waveform F is over-damped and has high inductance and resistance values. F has also an initial high frequency component which attenuates within the first 20 nanoseconds.

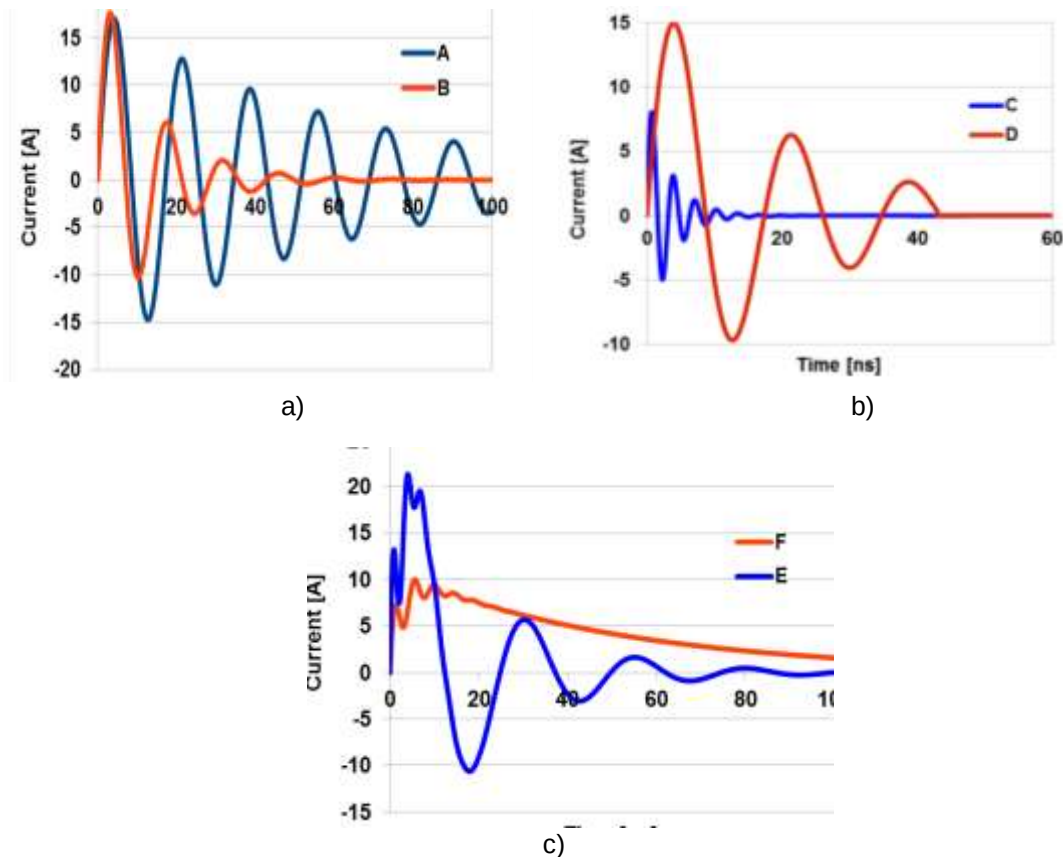


Figure 1: Typical CBE Discharge Waveforms

Table 2. RLC Values for the CBE Discharge Waveforms Shown in Figure 1

	C [pF]	L [nH]	R [Ω]	C₂ [pF]	L₂ [nH]	R₂ [Ω]
A	50	150	5			
B	50	100	15			
C	5	50	30			
D	50	150	15			
E	100	150	15	5	50	30
F	135	1000	400	10	50	20

The parasitic inductance of traces and connectors on a system board can slow down the CBE discharge current rise time. On the other hand, the current change rate di/dt can be higher in the CBE than in the CDM when the inductance is low and the initial charge and capacitance values are high. Additionally, an impedance mismatch can exist between the discharge source and the target. Because of the extra inductance, the CBE waveform often oscillates and can also have discontinuities due to multiple air discharges or dielectric breakdowns. These secondary discharges can occur within a nano second to a milli second interval. The waveform *D* in Figure 1b) shows an example of how the current flow stops after 42 ns due to the discharge channel closure.

The waveform *C* in the same figure shows a CBE discharge with a rise time of about 500 ps – close to a CDM event. This kind of discharge requires a small source ($C < 10$ pF) and a short discharge path ($L < 50$ nH). Events associated with large boards will likely have slower values of rise time, but may have a fast initial discharge either followed by or sometimes occurring simultaneously to a slower pulse. This is similar to the system ESD event as described by IEC61000-4-2 [14] standard where a fast initial peak current from a low capacitance gun tip precedes the slower secondary pulse. The existence of this fast event depends a lot on the product construction, discharge point and parasitics of the discharge path. This initial fast pulse is able to produce similar failures as found in cases related to CDM.

A CDM event in a CDM tester is fairly repeatable due to the fixed discharge environment. A CBE test method has not been defined and it is more challenging to get repeatable CBE testing performed in real life; this is due to the large variation in environmental parameters. Additionally, the potential difference can play a substantial role in influencing the main parameters. A very low potential difference (less than 100 volts) may not trigger ESD event at all and a high potential difference (> 2 kilovolts) may lead to corona discharges before the main discharge event. The corona may also cause the effective potential decrease before the spark is created, and the strength of discharge event may even decrease when the voltage is increased.

3.0 CASE STUDIES OF CUSTOMER RETURNS

3.1 Case Study I: Dual Operational Amplifier

During board-level testing, a customer experienced a very high failure rate (6.7%) on a double-level-metal submicron CMOS dual operational amplifier packaged in an 8-lead SOIC package [10]. The failure mode was consistently a resistive short (typically < 100 ohms) between pins 2 (-IN A) and 4 (-V / substrate) that rendered the side A operational amplifier non-functional. Interestingly, although each PCB used five of these same dual operational amplifier ICs, the failing units were always from the same board location (Position #5). Given the high failure rate, this board dependency ruled-out the possibility that the failing dual operational amplifiers were defective as received by the customer. A thorough review of the customer's application circuit showed no reason that the absolute maximum ratings of the Position #5 dual operational amplifier would ever be exceeded.

Failure analysis of the dual operational amplifier board failures consistently revealed emission sites at the anode of the input EOS/ESD protection diode between pins 2 and 4. Subsequent de-processing showed that these emission sites were due to silicon damage and melted or reflowed AlCu that shorted this protection diode (see Figure 2). Neither human body model (HBM) nor field-induced charged device model (FICDM) testing was able to replicate the relatively severe damage seen on the customer board failures. At the component-level, this dual operational amplifier in an 8-lead SOIC is robust to ESD events, passing at least 2000 volts HBM and 1000 volts FICDM testing to ESDA standards. Testing at 3000 volts HBM or 1500 volts FICDM caused the bias current at the input pins to exceed the 50 pico-amperes maximum specification, but the dual operational amplifier samples remained fully functional. Not surprisingly, the damage at the EOS/ESD protection diodes on the high-voltage HBM and FICDM samples was much more subtle than that shown in Figure 2 (i.e., the AlCu did not melt or reflow).

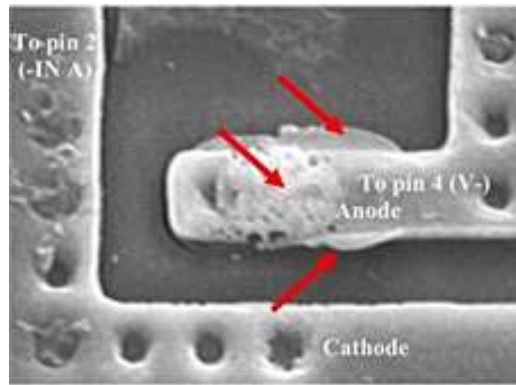


Figure 2: Scanning Electron Microscope (SEM) Image of the Melted / Reflowed AlCu (see arrows) at the Anode of the Input Protection Diode on a Customer Dual Operational Amplifier Board Failure

NOTE: The sample was deprocessed to the METAL1 layer.

The well-defined CDM simulates a charged component discharging just before it comes in contact with a conductive object that is at or near ground potential. Detailed test methods described by ESDA [15] and JEDEC [13] exist for conducting CDM testing using commercially available systems. (These two standards have been merged into a joint standard document; ANSI/ESDA/JEDEC JS-002-2014 - ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model – Component Level [13]). These test methods and systems were developed in terms of individual components. In an attempt to duplicate the damage shown in Figure 2, a field-induced charged board event (FICBE) test environment was developed and implemented in a manner similar to a method described by Lin [17]. The CBE simulates a charged PCB discharging just before contact is made with a conductive object that is at or near ground potential.

For the present work, a KeyTek Verifier Robotic CDM test system was used for FICBE testing of PCBs. This test system has a 127 mm (5 inches) diameter field charging plate covered by a thin (~ 13 μm) Mylar tape dielectric layer. This system conformed to ANSI/ESD STM5.3.1-1999 [15] and produced discharge waveforms that pass waveform verification testing with both 4 pF and 30 pF verification modules.

A compact, high-capacitance evaluation board (EB) was developed for CBE test purposes. This EB consisted of a decapsulated dual operational amplifier (i.e., the die was exposed) in a 150 mil, 8-lead SOIC package soldered at the center of a small 75 mm x 75 mm x 1.52 mm (3 inches x 3 inches x 60 mils) two-layer FR4 board. The bottom layer consisted of a 36 μm (1.41 mils) thick copper power plane, connected to volts - / ground power plane that covered the entire EB, while the top layer consisted of a 36 μm (1.41 mils) thick copper power plane, connected to volts + power plane that covered the surface of the EB except for the eight test pads that were connected to the

SOIC package pads via 0.61 mm (24 mils) wide copper traces. The volts - and volts + pins on the dual operational amplifier were connected to the ground and volts + power planes, respectively, while the remaining pins were connected to traces / test pads that were floating. No other components were soldered to the evaluation board (EB).

The FICBE test method for each EB was as follows:

1. The EB was centered on the charging plate (Figure 3). In this configuration, the EB capacitance measured between the ground plane and the field charging plate was ~ 1.6 nF.
2. The charging plate was raised to +125 volts and then the pin 2 (-IN A) PCB test pad (see Figure 3) was discharged. Consistent with the methodology in ANSI/ESD STM5.3.1-1999 [15], this was repeated two more times.
3. The I-V characteristics between pads 2 (-IN A) and 4 (V-) were checked for degradation.
4. The charging plate was brought to negative 125 volts and then test pad 2 was discharged. This was repeated two more times.
5. The I-V characteristics between pads 2 and 4 were again checked for degradation.
6. Consistent with the procedure in Steps 2-5, pad 2 on the same EB was subjected to FICBE testing in 125 volt charge voltage increments until degradation was observed in the I-V characteristics between pads 2 and 4.

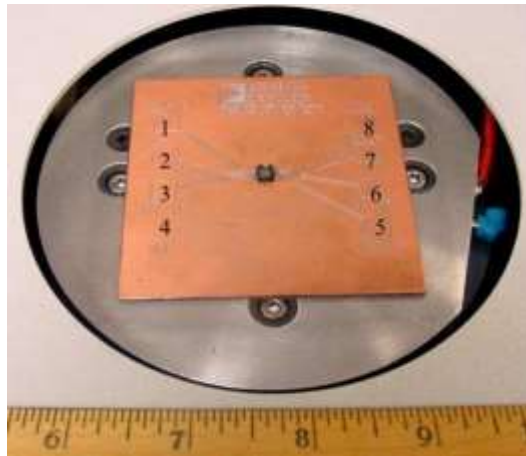


Figure 3: FICBE Test Method Setup for the Evaluation Board with the Decapsulated Dual Operational Amplifier and Eight Labeled Test Pads

For three samples that were FICBE-tested as per the previous section, no degradation occurred to the dual operational amplifiers after ± 250 volt stressing but leakage was detected between pads 2 (-IN A) and 4 (volts -) after negative 375 volt stressing. On three new samples that were FICBE tested at ± 500 volts, a resistive short of < 100 ohms occurred between pads 2 and 4 after - 500 volt stressing. FA of the negative 500 volt FICBE failures consistently revealed emission sites at the anode of the input EOS/ESD protection diode between pins 2 and 4. Subsequent de-processing revealed silicon damage and melted / reflowed AlCu at this protection diode (Figure 4). Thus, FICBE testing at negative 500 volts successfully replicated the failure mode and failure mechanism observed on the real-world board failures (Figure 2). CBE stressing of fresh samples at higher voltages resulted in severe damage that could easily be mistaken for other root causes of EOS damage. Figure 5 shows the catastrophic damage at the input EOS/ESD protection diode after negative 625 volt FICBE stressing. For negative charge voltage magnitudes of 625 volts and above, the AlCu anode interconnect was completely fused open.