

***MACHINE MODEL (MM)
Electrostatic Discharge (ESD) Investigation –
Reduction in Pulse Number
and Delay Time***

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*Device Testing
Machine Model (MM) Working Group WG-5.2*

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2.0 Purpose

The proliferation of high pin-count package configurations within the electronics industry has resulted in increasing stress times for all Electrostatic Discharge (ESD) test methodologies and models. One of these ESD models, Machine Model (MM), is an electrostatic simulation approximating the discharge event produced by machinery, furniture, or automated handling equipment. Present MM test methodology requires the application of three ESD pulses to a pin under test using several stressing configurations (referred to as pin combinations). Further requirements state that a one second delay between consecutive ESD pulses must be used.

Given the advancements made with present ESD test systems, discharge waveforms delivered to a device under test have a high degree of repeatability. When test system design was in its infancy, a user was often required to deliver several ESD pulses to be assured of at least one discharge waveform meeting the specified waveform parameters. The technical advance in electronics has resulted in an improved repeatability, each discharge waveform is identical to the one preceding it. Based upon the premise that a single ESD pulse is sufficient to damage a device, the MM Working Group (WG5.2) began an investigation into reducing the number of ESD pulses required during a MM test. In addition, MM energy dissipation time has been the topic of many discussions. Data has been presented [1] showing that the duration of the MM discharge event is short enough to allow for a reduction in the delay time between consecutive ESD pulses.

WG5.2 established a set of procedures to evaluate a proposed change from 3 pulses (present requirement) to 1 pulse while using a delay time of both 1 second (present requirement) and 0.5 second. This report documents the procedures, results, and conclusions.

At the time this report was approved, the MM Working Group WG5.2 had the following members:

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3.0 Background

The Machine Model (MM) is intended to simulate a machine (e.g., test equipment, furniture, etc.) discharging accumulated static charge through a device to ground. The discharge network is comprised of a charged 200pF capacitor and (nominally) zero ohms of series resistance (see Figure 1). Actual series resistance and inductance are specified in terms of the current discharge waveform through a shorting wire and 500Ω load (see Figures 2 and 3). Waveform parameters often used to monitor test system performance include first peak current (I_{p1}), second peak current (I_{p2}), and “first zero crossing - third zero crossing” period (T_{PM}).

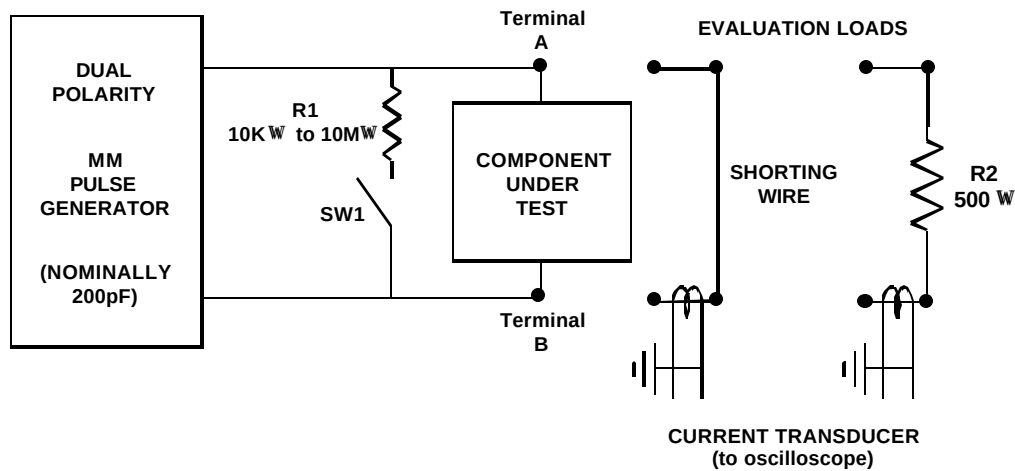


Figure 1: Typical equivalent MM ESD stress test circuit

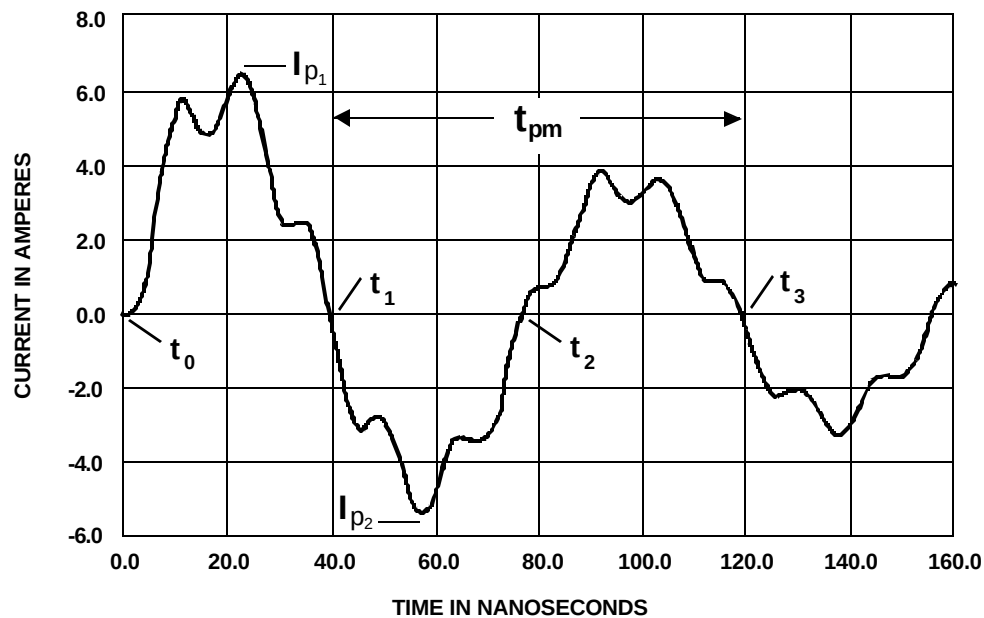


Figure 2: Current waveform through a shorting wire

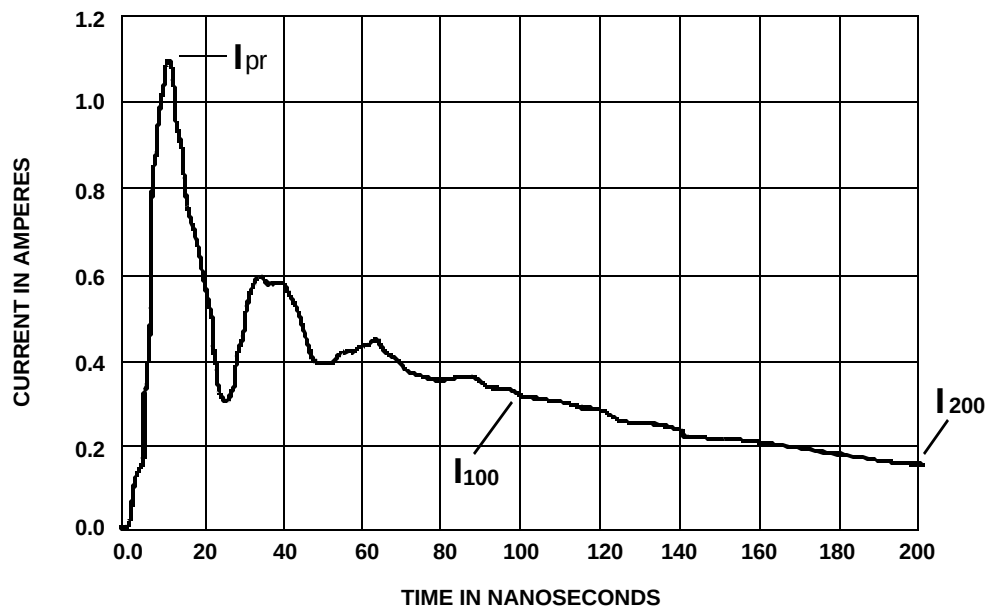


Figure 3: Current waveform through a 500Ω load

Recently, electronics industry Human Body Model (HBM) standards organizations approved a reduction in stress pulses from three to one with a 0.3 second minimum delay time between consecutive pulses. Given the similarities between the HBM and MM test methodologies, the effects of these changes on MM test results (including repeatability and correlation) required the development of an investigation. Members of MM WG5.2 were assigned the task of evaluating the effects of the number of ESD pulses and the delay time between consecutive pulses on actual devices. In the following sections, a detailed description of the investigation, device test results, and conclusions based upon those finding will be presented.

4.0 Experimental Set-up/Procedure

All Machine Model (MM) ESD stressing was performed at five different locations using five different commercially available ESD simulators (see Table 1). To ensure proper simulation and repeatable ESD results, simulator waveform performance was verified following the procedure outlined in the ESD Association MM ESD specification [2].

Table 1: Test location, test system, and test pin-count capability

Test Location	MM Simulator	Test Pin Capability
A	T1	256
B	T2	256
C	T3	256
D	T4	256
E	T5	256
F	T6	640

To represent as many device CMOS technologies and packaging configurations as possible, device codes of various pin counts were submitted for MM ESD characterization. Table 2 lists the devices chosen for the evaluation with the corresponding technology and packaging configuration. These devices represent “real world” examples.

Table 2: Device codes, technologies, and package configurations

Device Code	Device Technology	Package Configuration
R	0.8μm CMOS	32 PDIP
S	0.8μm CMOS	40 PDIP
T	0.4μm CMOS	44 PLCC
W	0.55μm CMOS	160 QFP
X	0.65μm CMOS	16 SOIC
Y	0.55μm CMOS	16 SOIC
Z	0.8μm CMOS	44 PLCC (only 22 pins used)

Prior to all MM stressing, test samples were datalogged by the originating member using Automated Test Equipment (ATE). Data typically included complete DC parametric and functional testing per applicable device specification requirements. A sample size of three devices was stressed at each voltage level following a matrix of pulse and delay combinations (see Table 3). Stress voltage levels and susceptible pin combinations for each device were selected based upon prior experience with the device under test. Once the starting stress voltage level and pin combination were identified, stress voltages were incremented using 50V steps. When stressing was completed, all devices were returned to the originating member for final end-point ATE datalogging. Results of these end-point tests were then used to determine the ESD threshold for each device code. A number of devices failing the electrical testing criteria were then submitted for failure analysis to determine failure location and mechanism.

Table 3: Test matrix example (voltage level and device serial number)

Stress Voltage	3 pulses w/ 1 second delay	3 pulses w/ 0.5 second delay	1 pulse w/ 1 second delay	1 pulse w/ 0.5 second delay
100V	#1, #2, #3	#4, #5, #6	#7, #8, #9	#10, #11, #12
150V	#13, #14, #15	#16, #17, #18	#19, #20, #21	#22, #23, #24
200V	#25, #26, #27	#28, #29, #30	#31, #32, #33	#34, #35, #36
250V	#37, #38, #39	#40, #41, #42	#43, #44, #45	#46, #47, #48

The investigation involved four separate areas of interest:

- **Test To Fail:** Three different device codes (R, S, and T) were stressed at location A using ESD simulator #T1. Due to a limited number of test samples, a stress to failure methodology was used. Devices were stressed at a given voltage level, submitted for end-point testing, and then (if passing) re-stressed at the next higher voltage level.
- **Failure Threshold Characterization:** Two different device codes (W and X) were stressed at location B using ESD simulator #T2. New devices were used at each stress voltage level.
- **Round-robin Stressing:** Two different device codes (Y and Z) were stressed at locations B, C, D, and E using a round-robin test methodology. Each test location stressed new devices at each stress voltage level using the ESD simulator (#T2, #T3, #T4, and #T5) at that location. Once stressing was completed, all test samples were returned to the originating member for end-point testing.
- **Discharge Waveform Comparison:** Discharge waveforms were acquired from five different ESD simulators (#T2, #T3, #T4, #T5, and #T6) and various waveform parameters were compared.