

TRANSIENT INDUCED LATCH-UP (TLU)

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2.0 Background

Complementary-Metal-Oxide-Semiconductor (CMOS) has become the dominant integrated circuit technology due to its low power and high packing density capabilities. The need to implement complementary (both N and P-channel) transistors in an affordable fashion results in potential current paths parallel to the desired functional circuit. Current flow through the MOSFET channels is not the only conduction path. The schematic representation of a CMOS inverter shown in Figure 1 also includes the often overlooked parasitic bipolar components. Under normal conditions, the circuit functions as intended because the bipolar transistors are usually turned-off.

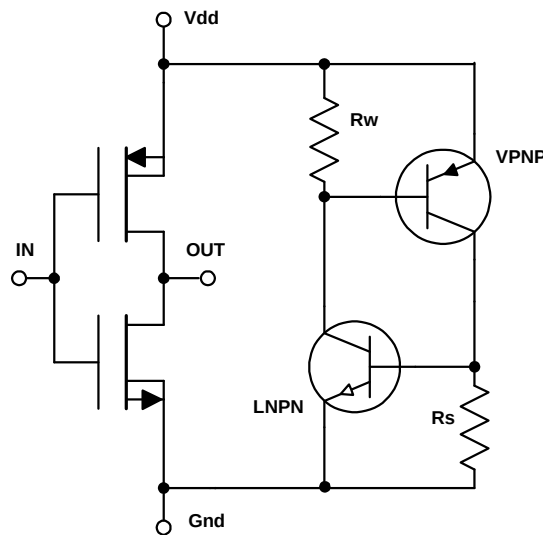


Figure 1: Latch-up current path for inverter

Latch-up (LU) occurs from the activation of four-layer pnpn structures (thyristors) that are formed by complimentary bipolar junctions. Under abnormal conditions, the bipolar transistors can turn-on. In the latter instance, large amounts of current may be drawn from the power supply causing circuit malfunction and/or irreversible damage to metal or junctions along the current path. Figure 2 shows a cross-section of a CMOS inverter with the undesirable parallel conduction path composed of bipolar transistors.

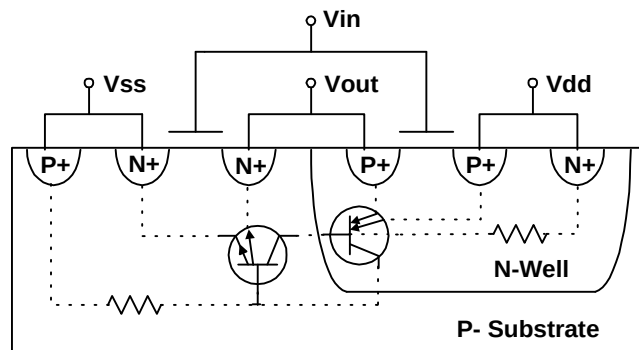


Figure 2: Parasitic bipolar transistors in a CMOS inverter

The classical ESD protection diode scheme for MOS inputs and outputs can even facilitate the onset of an undesirable LU condition [1, 2]. Therefore, both ESD and LU are interactive considerations in the design of reliable CMOS technologies. Modern-day designs make use of input/output (I/O) guard rings, adequate transistor spacing, and epitaxial silicon wafers to minimize LU sensitivity. A comprehensive treatment of LU and its dependence on process and design parameters can be found in references [3] and [4].

Testing of new CMOS designs to ensure that customers systems will not be burdened by LU is critical. The majority of LU characterization is performed using JEDEC Standard No.17 [5] and JEDEC JESD78 [6]. These test procedures are a static stress composed of I/O voltage/current overshoot and undershoot and power supply overvoltage. The stress is generally considered to be static because the specified stress transitions are between 5 μ s and 5ms. New designs rarely fail using the JEDEC LU procedure and industry compatible pass/fail criteria [7]. Despite this apparent success, some devices are found to latch in field applications or during 150°C burn-in, particularly when poor socket contacts and surface-mount parts were involved. Floating nodes and high temperatures can represent worst-case conditions for LU.

Static and/or dynamic stress in various time domains may trigger LU. Several studies [8, 9, 10] have shown that fast transient test methods are better for identifying LU weak devices. These findings suggest that the static nature of the JEDEC standard may be a “less than ideal” method of determining LU susceptibility. Even worse, this old standard appears to be less effective with each new scaling of process technology. The reason for this worsening assessment capability for LU sensitivity is readily apparent. Recall that latch-up robustness can only be appraised by using overvoltage stresses. At some specific overvoltage level, however, a device will be irreversibly destroyed; LU sensitivity can only be measured up to this level. Unfortunately, the “destruct level” decreases each time a technology is scaled-down to produce small, dense transistor structures. Figure 3 illustrates the balancing act required to accelerate LU stress without actually damaging the device. The “LU without damage” constraint is a requirement of JESD78; unfortunately, the margin allowable for stressing without damage is slowly disappearing, as shown in Figure 4. Recognition of the LU appraisal deficiency established the investigation of different trigger stimuli to identify potentially sensitive circuit designs [11].

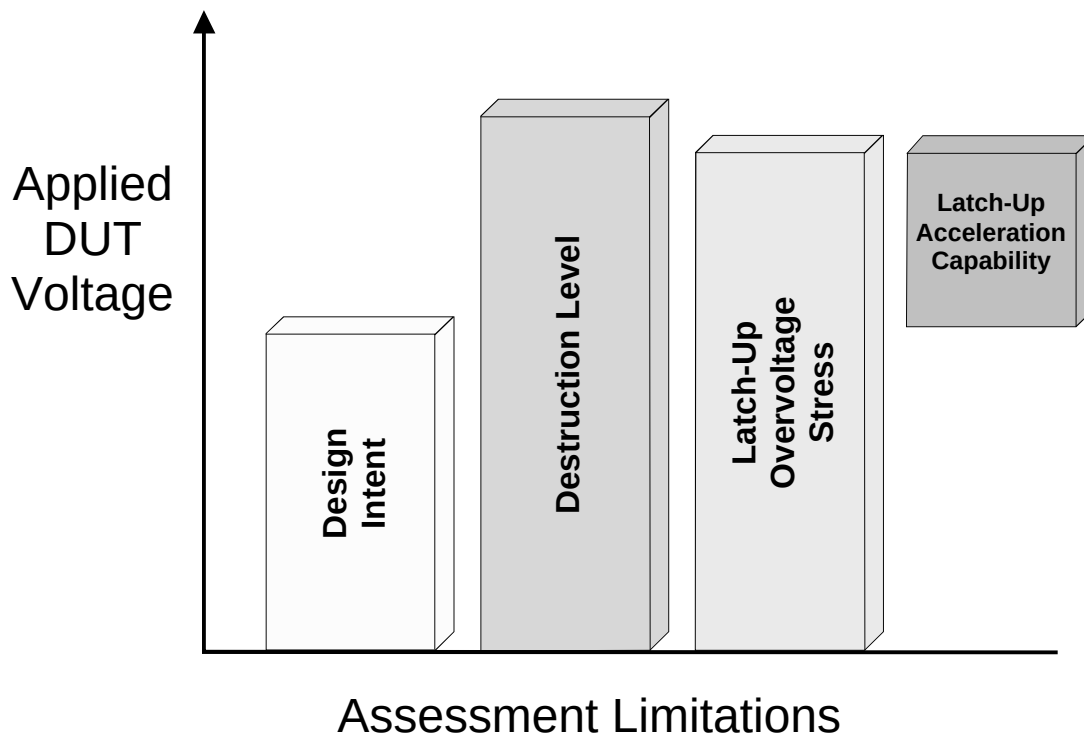


Figure 3: Latch-up assessment limitations

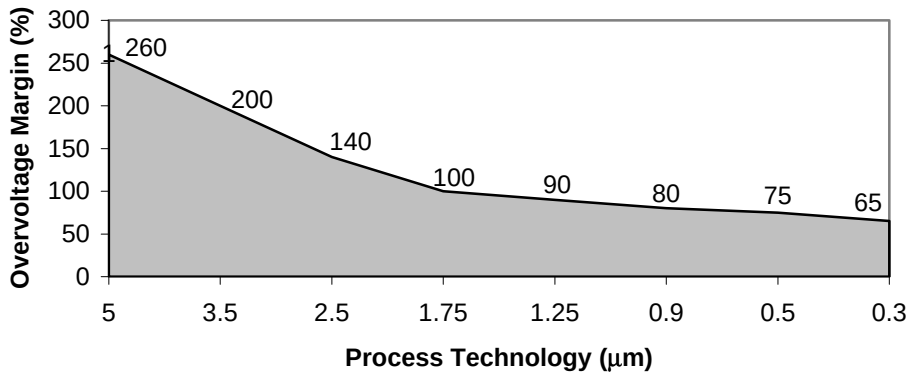


Figure 4: Reduction in overvoltage margin due to process scaling

Earlier work [12,13,14] served as the foundation for the creation of the ESD Association (ESDA) Transient Induced Latch-Up (TLU) working group WG-5.4. The development of a new standard for latch-up testing not only builds upon previous test standards but also requires the collaborative efforts of many individuals from different companies. Each contributor brings a unique perspective derived from experience with a particular mixture of technologies, device applications, and test equipment. The present ESDA WG-5.4 has members from ten different companies and includes representatives from four equipment manufacturers. Collection of data using new techniques is facilitated by the sharing of known problematic devices among the members in round-robin testing. Identification and removal of obstacles hindering the implementation of new automated equipment LU stress techniques is also a major objective for the working group.

Working group WG-5.4 attempted to improve the efficiency of latch-up screening in two different ways. Since LU is initiated by a collection of charge carriers at diffused layers (resistance) acting in combination with parasitic bipolar transistors, the goal was to maximize this charge density while minimizing the total transferred energy. Too much injected energy could result in thermal damage before useful measurements could be made. This consideration and the finite lifetime of injected carriers support the greater effectiveness of short transients for assessing LU immunity.

Also, the collective experience within the working group indicates that a majority of device LU sensitivity can be triggered through power pin stressing. This is not surprising since designers have many years of experience in optimizing I/O buffer guard-ring layout and computer-aided checks for appropriate implementation. Because power connections must go to every sub-circuit on the chip, the opportunity exists to stimulate circuit structures that have not been given the benefit of more robust layout. Therefore, additional test efficiency can be achieved by improving the traditional over-voltage power supply LU stress.

In this report, we first present a brief background on early LU work and then review the issues surrounding the power supply response requirements. We then discuss the efforts on RLC TLU testing, transmission line pulse (TLP) stressing, and the new bi-polar stress TLU methodology.

3.0 First Generation TLU

Earlier work [15, 16] reported success using simple RLC networks to produce a transient pulse able to trigger the latch condition. It was also discovered that transient stresses place more stringent requirements on the supply used to power the device-under-test (DUT). Success was achieved on 1.5μm technology devices when robust output or power pins were stressed using a 20Ω/100nF discharge network (see Figure 5). Collaborative

efforts within the newly established ESDA working group WG-5.4 resulted in the construction of the BEI-790 ($\pm 200\text{V}$) Test Set [17]. The waveform produced is shown in Figure 6 and was measured using a 100 megasamples per second single shot oscilloscope that had a bandwidth (BW) of 350MHz. The evaluation load used to measure the current was a solid shorting wire: 18-24 AWG (0.83mm^2 to 0.21mm^2 cross section) made of tinned copper not longer than 75mm. The wire was then inserted through a TEK CT-2 current probe having a bandwidth range of 1.2KHz to 200MHz.

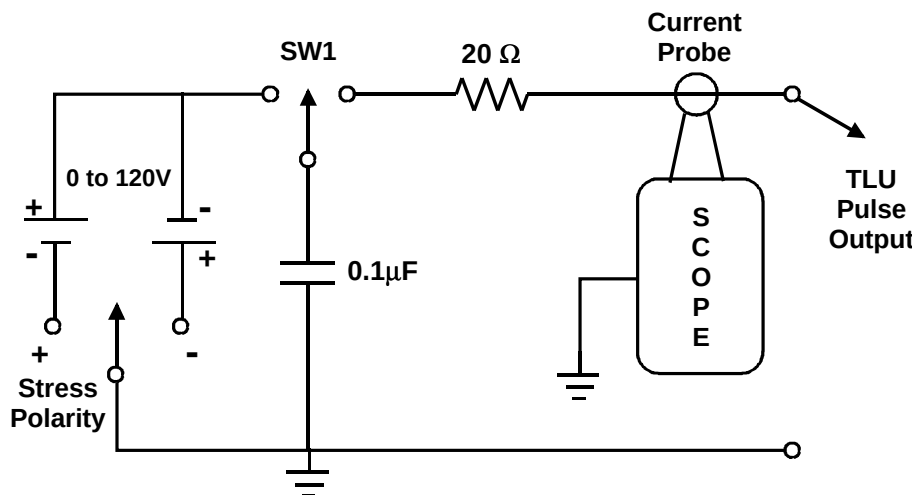


Figure 5: First generation dual-polarity TLU pulse generator

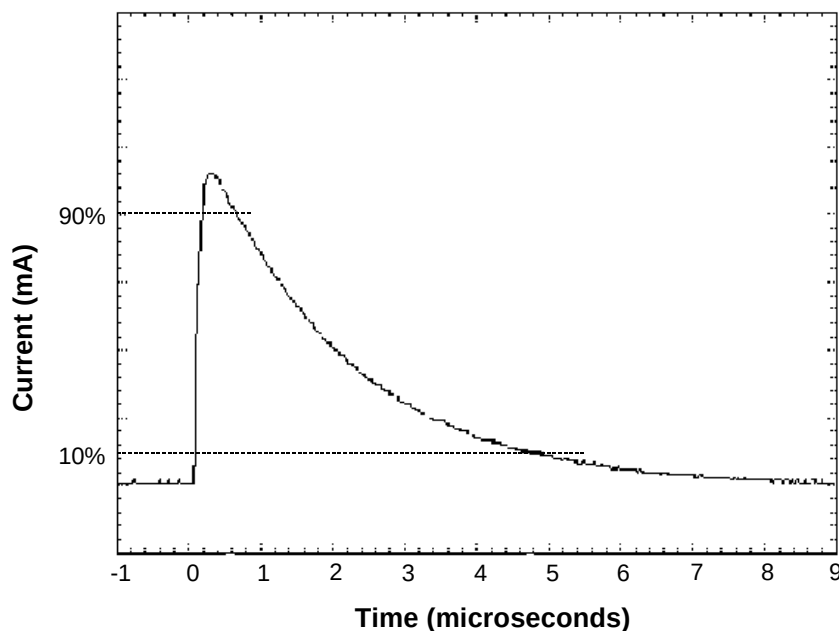


Figure 6: First generation TLU waveform

The shape of the waveform is a double exponential with less than 150ns risetime ($2L/R$), implying a low circuit inductance (L) of less than $1.5\mu\text{H}$. The fall time (90-10%) is approximately $5\mu\text{s}$ with an RC time constant of $2\mu\text{s}$. Waveform parameters at several voltages are as shown in Table 1.

Table 1: TLU waveform parameters

Voltage (V)	I _{peak} (mA)	Trise (ns)	Tfall (ns)
1.0	44.2 – 44.6	50 – 150	4.2 ± 10%
5.0	223 – 235	50 – 150	4.2 ± 10%
20	868 – 932	50 – 150	4.2 ± 10%
100	4300 - 4580	50 - 150	4.2 ± 10%

Figure 7 illustrates a typical TLU test configuration where a device-under-test (DUT) is appropriately biased while being stressed via the dual polarity TLU pulse generator. With several of the BEI-790 generators available to the working group, specification issues such as pulse rise-time, fall-time, and peak current amplitude were explored. During the period from 12/95 to 9/97, these evaluations resulted in the establishment of a TLU test method [18]. It was quickly recognized that newer technologies (<1μm) were becoming less robust for pulses longer than 150ns in duration. On-chip ESD protection networks generally cannot protect against this long time-constant electrical overstress (EOS). Consequently, many devices would be thermally damaged before a latch-up threshold could be determined. The quest for a new, shorter duration transient stress was then initiated. This set-back came as a surprise to many within the working group; proving that constantly changing technology often results in the pursuit of a moving target.

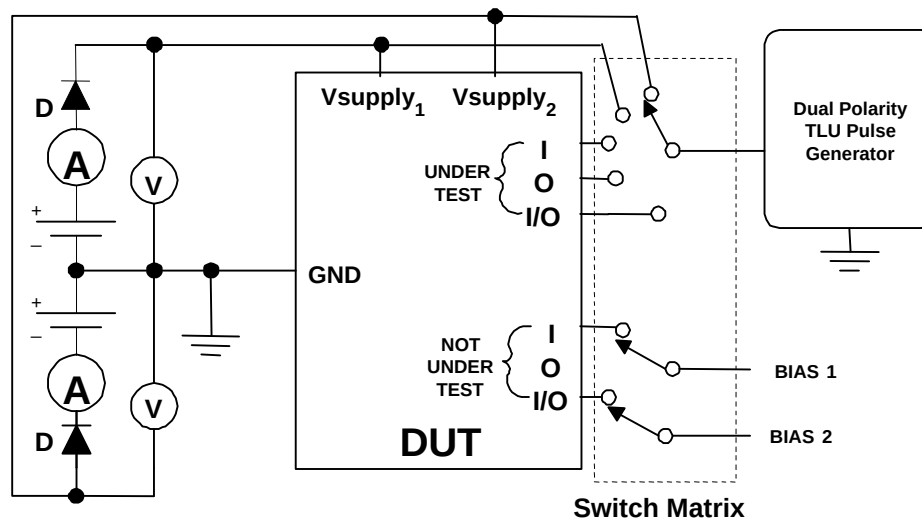


Figure 7: Typical TLU test configuration

4.0 Power Supply Response

When latch-up (LU) occurs in integrated circuits, a low impedance path is created between the power supply and ground. Consequently, the power supply experiences an abrupt increase in current demand and a sudden drop in voltage. To sustain a latch event, the increased current must be delivered to the DUT in a timely manner (before the transient stress has subsided) and the voltage supplied to the DUT must quickly recover to near-original voltage levels. This is not a concern when static stresses are used. In addition, the voltage supply (regardless of the stress duration) must limit the current to the DUT during LU to avoid excessive thermal damage to the DUT.

4.1 Power Supply Response (PSR) Test

To determine whether the power supply and connection network can meet the above requirements, a new test was developed. The Power Supply Response (PSR) test (Figure 8) allows for the measurement of recovery time due to an abrupt load change. This is crucial because LU in a device will not be sustained if the power supply cannot provide the necessary current during the transient period. Another way to explain this is to say there must not be a significant drop in the power supply voltage for the duration of the transient pulse in the device. Typical recoveries during a load change are shown in Figure 9. The acceptable power supply voltage response and recovery time (dark trace) is much faster than an unacceptable power supply response and recovery (light trace). The PSR test, performed by abruptly changing the power supply load from 510Ω to 10Ω , is accomplished by shorting out the 500Ω resistor with a very fast and bounce-free mercury (Hg) wetted relay. To measure the voltage recovery (Figure 9) and current risetime (Figure 10), a voltage probe, current transducer, and oscilloscope are used. Power supply test data established that an acceptable power supply must have voltage return to within 90% of its initial voltage level within 500ns of the application of a load change (510Ω to 10Ω). In addition, the current rise-time (10 to 90%) must be within 500ns. Different tests revealed that a number of available power supplies did not meet the required response to the rapid load change of 510Ω to 10Ω (see Figure 9, light trace).

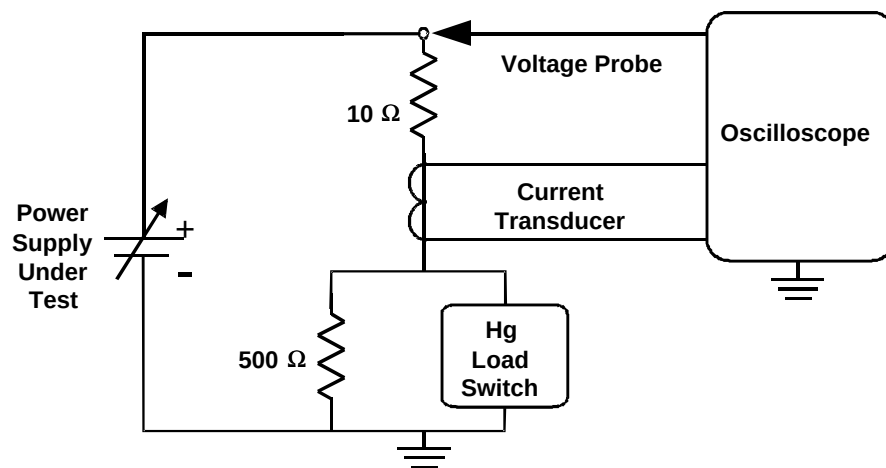


Figure 8: Power supply response test circuit