

ESD TR5.4-02-08

ESD Association Technical Report

Determination of CMOS Latch-up Susceptibility

Transient Latch-up – Technical Report No. 2



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***ESD Association Technical Report for the Determination of CMOS
Latch-up Susceptibility***

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Approved April 25, 2008
ESD Association



**TLU
Technical
Report
No. 2**

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FOREWORD

This document was prepared by the ESD Association Working Group 5.4, Transient Latch-up. It is intended to provide background information pertaining to the development of the TLU Standard Practice originally published in 2004 and additional data presented to the group since then. Summary data from various experiments is presented herein. The data supports the technical decisions made while developing the standard practice. Some background is provided as well as conclusions predicting the direction of the test method and recommendations about work that still needs to be done before advancing the standard practice on to a standard test method.

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**ESD Association Technical Report – Determination of CMOS Latch-up Susceptibility –
Transient Latch-up – Technical Report No. 2****1.0 BACKGROUND AND INTRODUCTION**

In developing the standard practice (SP) for transient latch-up (TLU) [Ref 1] a number of goals were considered. The primary goal was to design a test that would induce latch-up in susceptible CMOS IC devices as a result of a short duration “transient” electrical disturbance. At the outset of the investigations, this transient could take many forms, such as; fast slewing ESD like pulses, long ringing events, short duration supply bounce, and any other EMI or RFI induced noise in a subject circuit. Ultimately though, a waveform that can be scientifically controlled, reliably recreated and which reflects real-world surges on a variety of test equipment and bench setups was desired.

Also of importance was the need to develop a test method that is repeatable (can repeat on same setup) and reproducible (can repeat on another setup) on equipment having a variety of designs. In this effort, several waveforms for triggering latch-up were investigated and many were seen to cause latch-up in CMOS devices though some were difficult to repeat on the same equipment and virtually impossible to reproduce on equipment with different fixture or sources. These triggers were predominately ESD like events with fast rise-time and high amplitudes. While reproducible, these triggers were often responsible for physical ESD or EOS damage as a result of the trigger rather than a high current latch-up state. Ultimately, the negative going square pulse waveform was derived to satisfy these requirements. Its slower rise-time is easier to transmit through device fixturing and its polarity causes the trigger current to enter through a forward biased well-substrate junction, injecting it safely into the substrate rather than relying on potentially destructive mechanisms like avalanche breakdown or junction leakage to inject current through reverse biased junctions as is the case with most positive going transients.

Additional goals included a desire to overcome some limitations of the JEDEC latch-up test. In particular the V_{DD} overvoltage test has become increasingly destructive as device technologies scale to smaller sizes and lower operating voltages. To limit the complexity of the test and in an acknowledgement that the JEDEC current test (I-test) is still adequate for the purpose it is used for, the working group focused its efforts on a V_{DD} transient trigger. Reasoning that if one could increase test coverage to the whole die, the test could uncover latch-up susceptibilities at any location in the device.

1.1 Scope

The information presented in this technical report covers the time period from January 2000 when the first technical report was published through the development and release of the TLU SP to present. The data contained herein represents a wide variety of hardware but is primarily based on the procedure in the SP or experiments that led to that method. Data demonstrating the latch-up effect is presented. This data is used to determine the shape of the waveform used in the test method as well as justify some of the limits for the parameters defined such as polarity, pulse width and rise-time (slew rate).

1.2 Technical Report #1

As background to this report, the reader may want to review the contents of the group's previous technical report TR1 [ref 2]. In that document, several methods for triggering latch-up using fast changing pulses were described. Methods based on system level ESD, Transmission Line Pulsing (TLP) and RC networks were all discussed. Most of these methods were not used because they either induced physical damage to the device or the waveform was too difficult to reproduce under changing fixturing conditions.

Also described in TR1 are the elements of the bipolar stress TLU which was the starting point for development of the SP. The original drafts of the SP included elements of this waveform in the now removed Procedure A (see Section 3.2). Further simplifications of the waveform and introduction of new hardware methods resulted in the SP as it was published.

1.3 ANSI/ESD SP5.4

In 2004 the working group published a document describing the TLU test method [Ref 1]. This method used the negative going square pulse to trigger latch-up. The document contains a description of the waveform, specifications for hardware needed to create it and a procedure for implementing the test. Also contained are

guidelines on how to bias a device during testing, definitions and suggestions for alternate waveforms and testing multiple V_{DD} devices.

2.0 REPLICATING REAL-WORLD LATCH-UP THREATS

A debate continues in the TLU testing community about the test coverage of the negative going square pulse defined in the SP as opposed to other triggers that resemble real world noise. In particular, ESD like pulses are available to test engineers via modified ESD test systems and TLP characterization equipment [Ref 2]. Additionally the simplified nature of the pulse in the SP is more difficult to accept as an adequate tool for uncovering latch-up. The simplified waveform eliminates portions likely to cause EOS and limits the number of parameters thereby limiting the number of variables needed to control during experiments.

In application, circuit designers use bypass capacitors. While this will eliminate many access paths for transients to enter or exit a device, some threats like ESD can enter the assembly and be modified by the network of traces and bypass caps until it is ringing in the amplitude and frequency range relevant to the pulse in ANSI/ESD SP5.4. Furthermore, poor design practices like insufficient grounding or bypass can make a design even more susceptible to admitting noise to a device. While difficult to measure, the transient pulse reaching a pin on a DUT in a powered circuit would likely be moving much slower and have lower amplitude than the incident ESD pulse which excited it.

At least two predominant means for creating transient noise have been devised for device level testing. Other means may exist. Transient voltage noise has been created by either directly driving a pin or node with a programmable source with sufficient power or by releasing a stored charge onto a pin or node. The SP mainly concerns itself with the source driven transient; however, members have shown similar results and have presented data using ESD like pulses. Data from the group is primarily limited to the source-driven transient. Stress is mainly applied to supplies; however, there was also work performed on stress to I/O pins.

2.1 Source Driven Transient

A source driven transient is one where V_{DD} and the transient are directly supplied and under full control of the source that powers the DUT. In its most basic form this configuration consists of a pulse source and a broadband power amplifier capable of buffering the high impedance pulse source to a power level capable of simultaneously supplying DC power to V_{DD} and AC power for the transient noise signal.

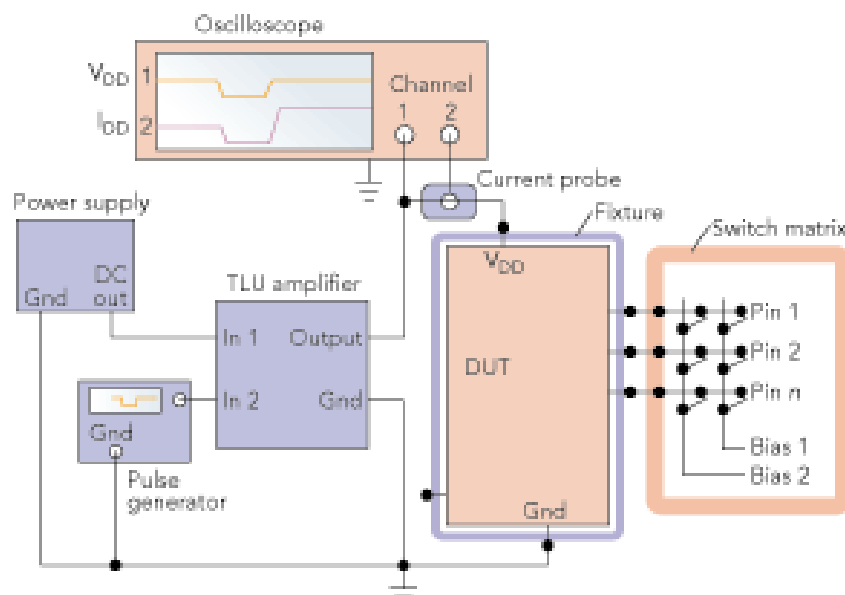


Figure 1: Basic Implementation of Broadband Amplifier for Creating TLU Events

A Broadband Power Amplifier is DC and AC coupled to the output. Any amplifier capable of faithfully buffering the specified transient noise signal and having a DC offset in the range of V_{DD} required by the DUT is a candidate. Ideally this instrument would have a DC to ≥ 1 MHz bandwidth and have a wide voltage and current range allowing it to reproduce complex waveforms with slow and fast changing features. Fast acting current limiting to protect the DUT and voltage clamping to protect fixture equipment like switch matrices are valuable features to distinguish between TLU and EOS but not required to perform the test.

The main advantage to the source driven method is the very wide variety of transients that can be tried. Virtually any noise signature within the bandwidth and amplitude limitations can be reproduced. The transient pulse source can be a basic instrument like a function generator or pulse source or an advanced tool like an arbitrary waveform generator (ARB) or a recorded waveform or the output from a purpose built circuit. These fast changing power amplifiers cover a wide range of real world noise that can be found on actual products and experimentally controlled signals like that used in ANSI/ESD SP5.4. Another advantage is the ability to integrate this method into ATE and specifically built TLU test systems.

The main disadvantage is that any amplifier will have a maximum slew rate and amplitude thereby excluding ESD like events. It is thought that ESD like triggers may induce latch-up via a different mode. Commercially available pulse generators may bridge the differences between amplifiers and ESD generators.

2.2 Stored Charge Transient (powered ESD threats)

Stored charge transients are electrical disturbances caused by the discharge of an electrostatically charged object into the power supply (V_{DD}) of the DUT. These transients are similar to ESD triggers used in conventional HBM, CDM and MM device testing but they have generally lower amplitude to avoid causing ESD damage. Furthermore, unlike ESD testing, these pulses are applied to powered devices.

Equipment used for traditional ESD testing can be used for TLU when a power source for V_{DD} is added. Combination ESD/latch-up testers can be adapted to this task with proper decoupling of the DC source, provided that the DC source is fast enough to react within the pulse duration.

The advantage to this method is that it can be readily adapted from existing test systems already used for similar testing. The waveform is familiar and readily accepted as representing a real world threat. The disadvantage is that this method often results in ESD or EOS damage rather than latch-up. Another problem is one that persists for all very fast changing signals; it is difficult to reproduce precisely in different fixtures or on different equipment. Only broad features of the waveform like peak amplitude and rise-time are controlled while more precise control of the shape would be desirable.

Another type of equipment capable of delivering a stored charge to a V_{DD} source is a Transmission Line Pulse (TLP) test system. These systems are engineered to deliver a precisely metered amount of energy at a variety of fixed rise-times and pulse widths. The test systems are already in use for characterization of IC buffer structures and thus are tuned to not cause EOS or ESD damage which makes them suitable for triggering non-destructive latch-up.

The advantage for TLP is the present availability of equipment from several vendors and that amplitude and pulse wave form can be rather easily controlled. The higher slew rates attainable on the TLP waveforms will allow characterization of faster classes of transients and extension of the data showing sensitivity of slew rate on trigger level. While the disadvantage is that the systems are generally bench top and need additional fixturing to bias the device for testing. The speed of the signal generally prevents it from reliably being transmitted through a switch matrix but future development may overcome this limitation. These systems also can only produce a limited range of waveforms and continuous control of most features of the wave shape is not easily possible.

2.3 RF Coupled or Capacitively coupled transients

It is also possible to induce transient voltage and current surges in equipment by inductively or capacitively coupling environmental or RF noise to the circuit and interconnect components of an assembly. To a lesser degree this noise may also be coupled directly to the IC device itself. Several system level specifications already deal with this type of noise at an equipment level. Since this working group's objective is to develop a device level test and that these types of noise injection are difficult to reproduce at a device level, the focus of the testing was directed toward a method that could definitively be reproduced and controlled.

3.0 DEVELOPMENT OF THE PRESENT STANDARD PRACTICE SP TLU-1

The development of the waveform used in the SP is a result of a series of experiments and the systematic elimination of portions of waveforms until all that is left are the essential features that cause latch-up.

If one were to review the first technical report written by the TLU working group one would see that a variety of ESD like fast rising waveforms had already been tried and successfully shown to trigger latch-up. It was generally agreed that these methods were difficult to make reproducible due to the fast rising waveforms and test systems would be necessarily expensive and complicated.

Another leading technique was a capacitor switched into a power supply connected to the DUT. This caused uncontrolled oscillations as the power supply struggled to regulate with the new load. This method was very difficult to repeat as the transient waveform would be altered by any change in the fixturing including length of wires and model of power supply. Although the SP started out with this method it was eventually dropped due to these difficulties.

With the switched capacitor method and other methods, bipolar damped sine transients were shown to trigger latch-up [Ref 3]. These were classic damped sinusoid transients and initially it was not clear which parameters were most important to triggering latch-up. More recent work has shown in greater detail, the same bipolar noise waveform [Ref 4], triggering TLU in a test structure. When the broadband power amplifier (TLU amplifier) became available, engineers were able to recreate these transients precisely and dissect them to determine what parameters were most influential in triggering latch-up.

Initially, the damped sine transient was shortened to a single cycle of a sine wave. By trying different frequencies, various phases and half sine forms of this trigger it was determined that the rising portion of the waveform was always the point where latch-up would occur. For devices which triggered from a positive half sine, these devices were often already known to be susceptible in the JEDEC overvoltage test. A variety of other devices were shown to be triggered from a negative half sine, some of which had no other known latch-up sensitivity.

Eventually the positive half of the sine wave was eliminated as it was felt that failures in this mode are already adequately screened for with the JEDEC overvoltage test. Finally, the sine shape was changed to a square shape. This simplification had the effect of delineating the portions of the waveform when charge is injected (falling edge and lower plateau) and when charge carriers are evacuated from the substrate (rising edge) and triggering can occur according to the Electron Flood Theory. This separation of parameters is not possible with a sine waveform as the pulse width and the rise and fall times are mathematically linked.

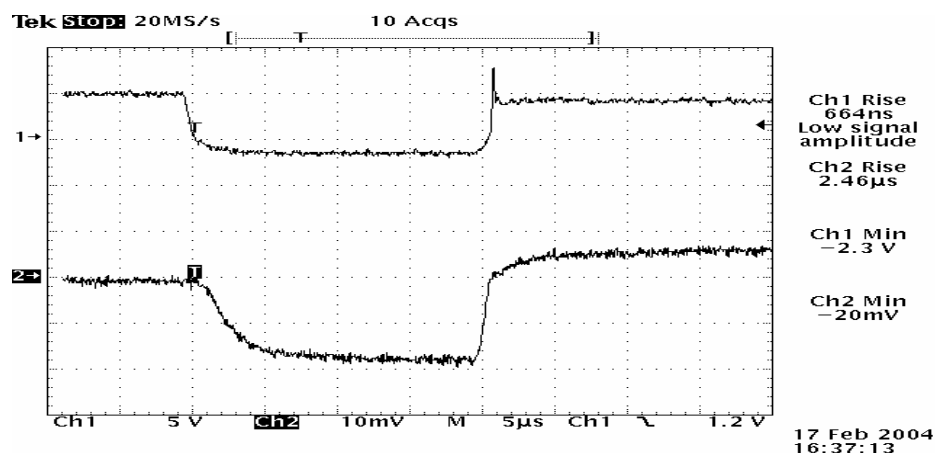


Figure 2: Oscilloscope waveform showing TLU failure using Method in ANSI/ESD SP5.4. Top trace is V_{DD} and the Bottom Trace is I_{DD} (500 mA/div)

3.1 Electron Flood Theory (Proposed Trigger Mechanism)

The mechanism that has been proposed as the trigger for latch-up when using the negative going square pulse goes as follows: Initially a device is powered and functioning normally. Suddenly V_{DD} is pulled below ground by at least one diode threshold (V_T) which causes supply current to reverse and flow into ground due to the forward biasing of the well-substrate junctions which are connected everywhere across the die. In a very short time, the substrate is saturated with these charge carriers (ANSI/ESD SP5.4 allows 20 μ s for this to occur, before the

risk EOS). Next V_{DD} is rapidly returned to normal, when this happens, the injected charge carriers evacuate the substrate creating a current along the path to the ground and V_{DD} pads; this is essentially the Trigger Current. The magnitude of this current is proportional to the trigger voltage (undershoot on V_{DD}) and the rate that V_{DD} returns to normal (rise-time). This current flows through the substrate and other structures and creates voltage gradients according to the resistivity of those local structures. If this voltage gradient is situated in such a way as to invert a P-N junction, the resulting current flow can initiate and sustain latch-up. Since this injected current is in all areas of the substrate, the latch-up could potentially be triggered anywhere.

Other mechanisms for latch-up triggering have also been proposed. One way is a parallel to the phenomenon known as dv/dt triggering of an SCR. This parameter is known as “Critical Rate of Rise of Off State Voltage” or “ dv/dt ”. In this well known effect, excessive voltage rise on the anode and cathode of a discrete SCR can capacitively couple charge into the trigger and turn on the device without application of an external trigger.

3.2 Defunct Procedure A

Early versions of the draft document for the TLU SP contained an alternate test procedure referred to as “Procedure A”. This procedure used a linear power supply in conjunction with an Inductive-Capacitive (LC) Pulse Generator network to produce an oscillation of the power supply voltage. When connected to certain devices, this setup was shown to induce latch-up. Recreating the same waveform on other similar apparatus proved to be almost impossible. The small changes in R , C and L caused by any change in equipment such as conductor length, interconnect resistance or DUT socket would produce a very different waveform in terms of amplitude, damping and frequency. After attempts to normalize the setup and combine both procedures into one document, the procedure was judged to be unrepeatable and was replaced by the procedure now published in the SP. While Procedure A was irreproducible, it did appear to trigger latch-up during the negative undershoot portion of the waveform.

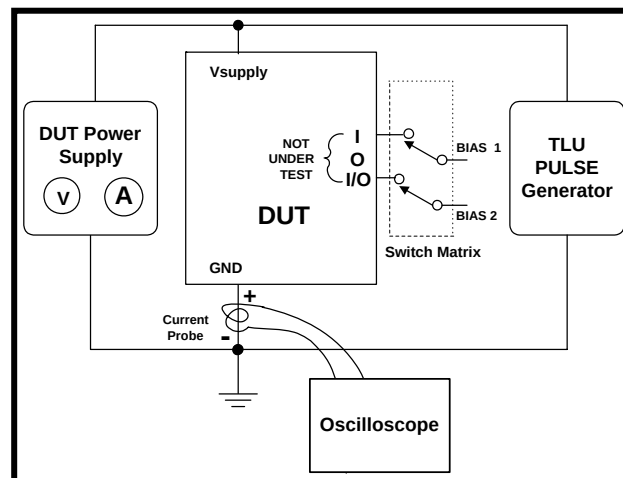


Figure 3: Basic Hardware Configuration for Procedure A.

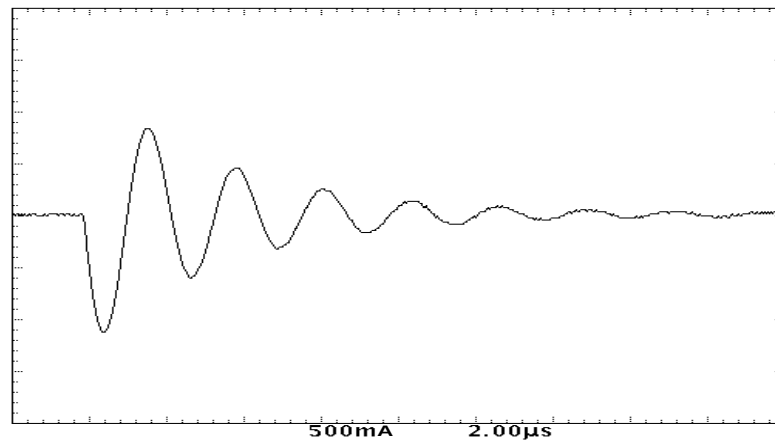


Figure 4: Typical I_{DD} waveform produced by "Procedure A" Apparatus with No Load, also known as a Damped Bipolar Sine Wave

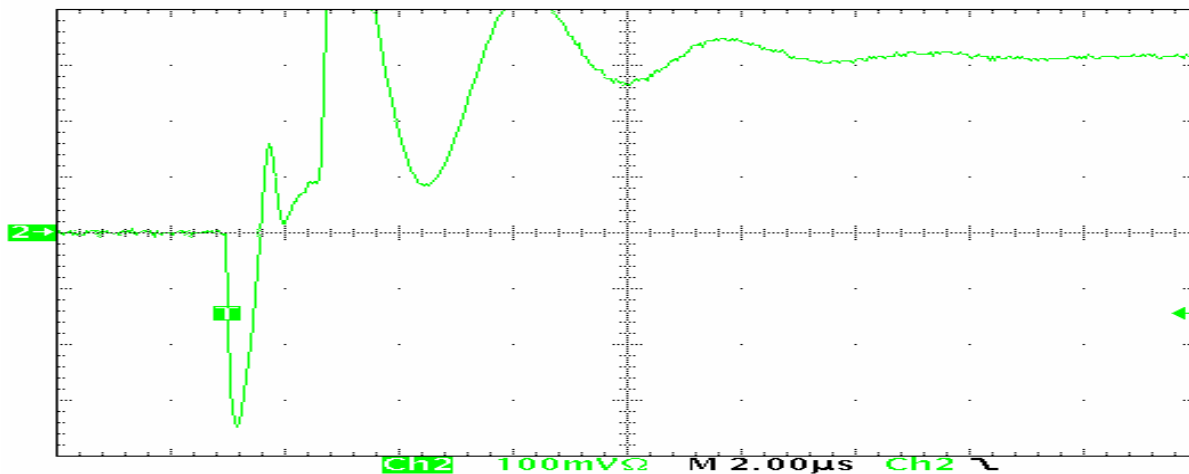


Figure 5: Actual I_{DD} waveform from Procedure A with DUT connected

3.3 Negative-going Square Pulse

With the introduction of the TLU Broadband Amplifier, experimenters were able to try a variety of waveforms that were previously difficult to reproduce. The amplifier made programming repeatable and continuously adjustable waveforms possible. Initially waveforms similar to the bipolar damped sine were tried then these were simplified to a single sine cycle or half cycle. Several experiments with the half sine triggers convinced experimenters that latch-up was being triggered at the point where the waveform returns to normal V_{DD} levels after briefly going below ground. While some devices did trigger latch-up due to positive going half sine transient triggers, these failures correlated well with the JEDEC JESD78A overvoltage results and thus were considered already covered by previous test methods.

After determining that latch-up can be triggered after undershooting ground, additional experiments were undertaken to determine what other parameters were significant. To aid in this research, the waveform was further simplified to a negative going square wave. While still having the undershoot features of the half sine, this final waveform could now be dissected into several parts. The falling edge, the time held below ground

(pulse width) and the time it takes to return to V_{DD} (rise-time) are all measurable and controllable quantities. In order to design a repeatable experiment, some of these variables must be held constant. If the falling and rising edge slew rates were made to be the same, then only the pulse width needs to be made constant.

Several experiments were undertaken to determine an optimal pulse width. This testing showed that triggers with excessively long durations (>100 ms) risked causing EOS damage due simply to heating caused by the trigger current (which can exceed 1 A). On the other end of the scale, triggers with very short durations (<50 ns) might not trigger latch-up at all. It became apparent a range of time durations would be acceptable. A 20 μ s pulse width was adopted as a compromise between the two extremes and judged to be useful on a very wide range of devices.

Determining the optimal value for the rise-time is a subject of active research. Evidence shows that there definitely is a correlation with rise-time (or slew rate) and latch-up sensitivity.

Section 5 seeks to highlight the experimental data along the path of reasoning leading to the negative going square pulse.

3.4 Effect of Rise-time or Slew Rate on Latch-up Sensitivity

As the bandwidth of the broadband amplifier increased when new models became available, it became apparent that data thought to be repeatable was now failing at a smaller trigger level than before. Investigations showed a strong correlation between rise-time on the way back to V_{DD} and the voltage undershoot amplitude needed to trigger latch-up (failure point). When the rise-time of the faster equipment was slowed, the data began to match again.

It was now apparent the rate at which V_{DD} is returned to normal (rise-time) is important. If the rise-time is too slow, insufficient current will flow in the substrate and voltage gradients will be too small to invert any junctions. Research into the range of slew rate that is significant to the result is ongoing. It is desired to find a speed that is fast enough to trigger latch-up at the lowest trigger voltage but slow enough that it can be transmitted through typical ATE or bench-top device fixtures.

Figure 6 shows the results of TLU testing on four devices with known latch-up sensitivities (see Section 6.4.3 for data). It is apparent that as the slew rate slows to 1 V/ μ s the trigger threshold for latch-up increases up to -7 V (actual voltage below ground) after which slower rise-time would not trigger latch-up at any voltage. At this point the slew rate of V_{DD} was insufficient to establish the electric field needed to produce a sufficient trigger current. As the slew rate is increased, the trigger voltage seems to saturate at a minimum voltage and only gradually decrease as faster slew rates are tried. This suggests another mechanism such as carrier mobility is now dominant in determining the trigger current rather than the electric field created by the changing V_{DD} voltage.

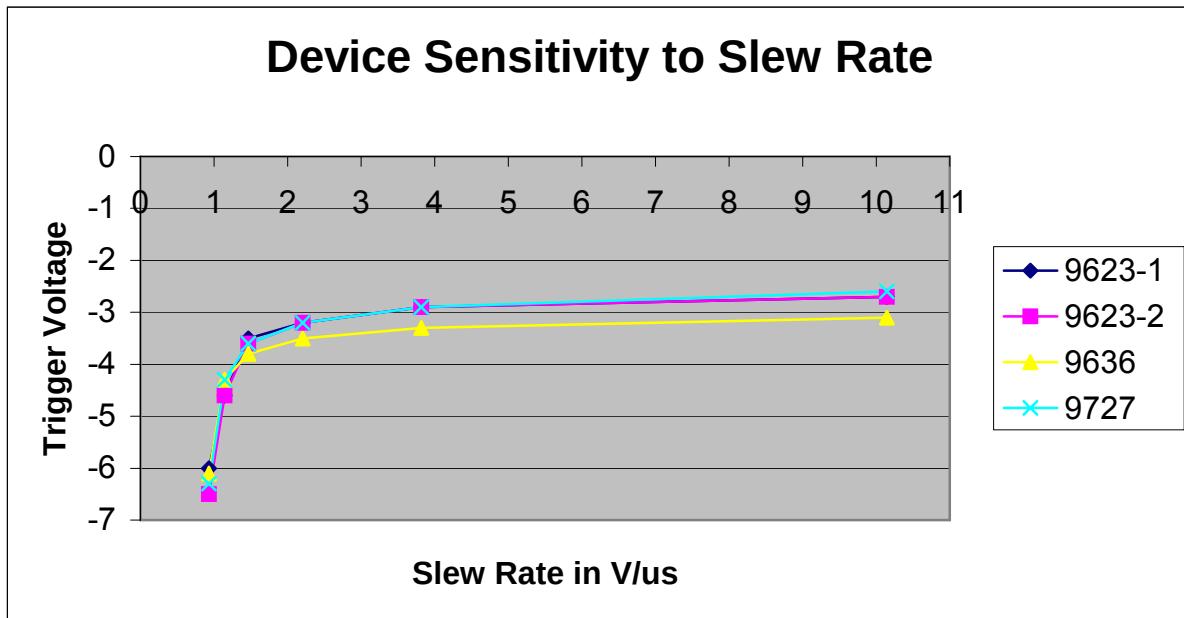


Figure 6: Slew rate dependency of latch-up sensitivity using the procedure in ANSI/ESD SP5.4 and a 74HCT00 device with known latch-up sensitivity.

If this pattern holds true for a wide variety of devices, it would suggest that there is a slew rate that is fast enough to serve as a characterization metric without needing to go faster and complicate the fixturing needed to deliver such a high frequency transient. This is an area of current research.

3.5 Experimenting with Other Waveforms

The SP as written (in appendix 10.3) allows the user to experiment with any other waveform that they think is significant. The hardware setup described in the SP allows the user to apply any transient waveform within the technical limitations of the test system (signal amplifier and device fixturing). At present this limitation is ± 35 V, ± 3 A, DC to 1 MHz bandwidth. This allows a wide range of transient waveforms to be tried. It is the hope of the working group that users of the SP will discover alternative or even more optimal trigger waveforms while using the SP. Furthermore, experiments on devices with multiple and bipolar or negative power supplies would confirm if this procedure is universally applicable. This new information may be incorporated into future versions of the SP or its evolution into a STM.

3.6 Advantages and Disadvantages to the Method in ANSI/ESD SP5.4

The clear advantage to this method is the lower likelihood of inducing EOS just as a result of attempting to trigger latch-up. Also the test coverage (w.r.t. the area of the die queried by the test) is as high as one could expect with this type of testing, presumably all areas of the die in a particular V_{DD} domain are flooded with charge, and any structure within that domain could become susceptible to latch-up. Additionally the slew rate of the waveform is slow enough to implement on a wide variety of test systems as the effective bandwidth of the waveform is 1 MHz or lower. Biasing the device using existing switching or ATE based systems should be possible.

The main disadvantage is that it only stimulates one likely trigger mechanism. There exist other possibilities for triggering latch-up such as energy capacitively coupled into circuits and other non-destructive circuit breakdown events yet to be described in detail. Triggers with faster rise-time may become more or less sensitive or switch to being sensitive to positive overshoot transients.

4.0 TEST HARDWARE

Several forms of test hardware have been used to successfully induce transient latch-up. The ANSI/ESD SP5.4 method uses the source driven transient but recent work by members of the device testing working group using TLP and ESD test systems has produced useful results and in some ways correlating with the method in the SP with respect to its sensitivity to rise-time.

In all cases the experimental setup needs to have a means for fixturing the device and a means for measuring V_{DD} and I_{DD} . Fixturing can be a simple breadboard or manual switch box with DUT card or as complex as an ATE switch matrix. Measuring V_{DD} is simple requiring only an oscilloscope probe placed close to the DUT but measuring I_{DD} will require either a clamp on DC/AC current probe (Hall Effect probe) or instrumentation built into the power amplifier or other test instrumentation. The current probe must have sufficient bandwidth to track with the rapidly changing transient.

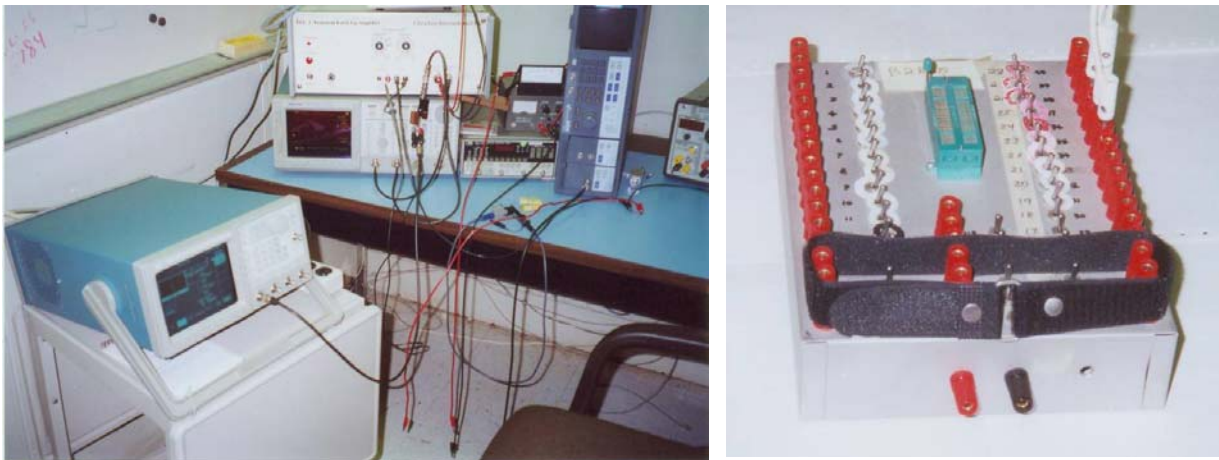


Figure 7: Bench setup for TLU testing. Note the TLU amplifier at the top center of the photo. On the right is a photo of a typical manual switch box used to bias simple devices.

4.1 TLU1–TLU5 Equipment

One vendor (UltraTest International) has been developing test hardware to go along with the Standard Procedure. To date, five prototype versions have been developed and made available to the working group to generate the data reported in this document. With each new hardware version, the speed of the instrument in terms of bandwidth or slew rate is improved upon allowing for faster rising waveforms to be tried. Additionally improvements in the response time of the current limit and new features like inputs with different gain have made the equipment more useful for TLU testing.

All versions of the UltraTest International hardware include an integrated current measurement output to facilitate the measurement of I_{DD} which is critical to assessing the device's response.

4.2 TLU Broadband Amplifier Specifications

The Target specification for a TLU amplifier is defined in the SP.

Table 1. Target Specification for a TLU Amplifier

Spec	TLU-5	TLU-4	TLU-3	TLU-2	TLU-1
Output Voltage Range	± 30 V	± 30 V	± 30 V	± 30 V	± 15 V
Output Current Range	± 5 A	± 3 A	± 3 A	± 3 A	± 1 A
Input-output propagation delay	75 ns (OL) 100ns (CL)		230 ns		
Rise-time	50 ns (OL) 200 ns (CL) (10V rise)	493 ns (5 V rise)	3 μ s (20 V rise)		
Max Slew Rate Calculated from rise-time	200 V/ μ s (OL) 50 V/ μ s (CL)	10 V/ μ s	6 V/ μ s		
Maximum bandwidth before amplitude degrades below 80 %	>2 Mhz (OL) 1 Mhz (CL)	1 Mhz	100 khz	40 khz	
Maximum frequency before waveform distorts	2 MHz	1 Mhz	300 khz	300 khz	
PSR Test	500 ns voltage 800 ns current		1.5 μ s Voltage	2 μ s	
Current limit response time	3.3 μ s		12 μ s	20 μ s	NA
Voltage limit response time	1.2 μ s	NA	NA	NA	NA
Inputs	1 $\times$, 2 $\times$, 5 $\times$, 10 $\times$	1 $\times$, 10 $\times$	1 $\times$, 10 $\times$	1 $\times$, 10 $\times$	
Feedback mode	Open loop / Closed loop	Open loop / Closed loop	Closed loop	Closed loop	Closed loop
Output Slew rate limit feature	Yes	No	No	No	No
Current measurement feature	Yes	No	Yes	Yes	No

OL= Open Loop, CL= Closed Loop mode

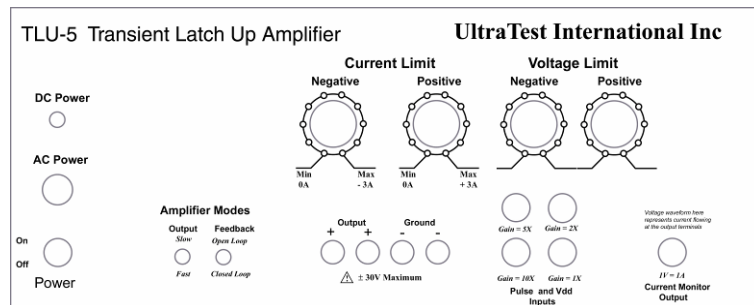


Figure 8: Left: TLU-2 Hardware; right: TLU-5 Hardware front panel

4.3 Infineon's Setup

In 2001, Infineon experienced a problem with a CMOS product during lab testing. Although passing the JEDEC latch-up qualification (Class II) without any failures, several dies failed during functional lab testing, showing typical "latch-up" behavior. The devices are electrically shorted and physical failure analysis revealed large molten silicon areas. Those failure signatures could point to a TLU phenomenon which causes the device failure. After careful analysis, it turned out that voltage overshoots in the experimental setup causes the triggering of the latch-up.