

# **ESD association technical report**

## ***Voltage and Energy Susceptible Device Concepts, Including Latency Considerations***

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## Purpose

This Technical Report (TR) contains information to promote an understanding of the differences between energy and voltage susceptible types of devices and their sensitivity levels. (See Appendix for definitions of susceptible and sensitivity.) Understanding these susceptibilities and their differences, aids personnel involved in electrostatic discharge (ESD) protective program planning and tailoring. This TR emphasizes the importance of identifying device technology differences and contains simple analogies along with more advanced information for both non-technical and technical personnel. The two types of susceptibility and their vulnerability to be damaged from different static sources or events will be explained.

This TR also helps in the understanding of why and how different device susceptibility types need to be considered in the specifications for an ESD protection program. Proper protection methods for computer disk drives and other susceptible components, like chip capacitors and thin film resistors also need to be understood. Once the different characteristics of the two susceptibility types are apparent, it will be clear that these devices must be handled, packaged, processed, assembled, or serviced with different procedures.

The concept of latency is explored with regard to various ESD exposures that are claimed to result in latent failures. The controversial issue of latent failures is discussed, based on the characteristics of the two basic types of susceptibility, to provide insight and possibly reduce latency concerns. This TR shows that susceptibility type identification is essential to plan and implement an effective ESD prevention program for all types of production facilities and field services. Susceptibility type identification is also intended to reduce the concerns about latent failures by understanding how different electrostatic sources can damage these devices.

## Introduction

Semiconductors and other devices are susceptible to ESD damage. Many people have become aware of this fact, but some people are still not convinced about the necessity of basic ESD protection procedures. They also may not be convinced that the requirements need to be tailored to the susceptibility type as well as the sensitivity level. Until there is a full understanding of device susceptibility characteristics and device sensitivity levels, staff personnel at facilities cannot implement ESD protection procedures that are proper for assuring ESD protection. Also when staff is discussing upgrading ESD protection, they will not know if an upgrade is needed and if it will be cost effective.

Some ESD practitioners feel a basic ESD program is sufficient while others continually perceive a need to upgrade their programs. There are several reasons for different opinions about proper ESD protection procedures. The main reason is that device technology is so varied. This makes it difficult for everyone to have the same information and to be able to have an appreciation for susceptible device differences.

An investigation of how and where an ESD event may have caused the failure is generally not carried out. Failure analysis is usually not done very often and seldom is it done for every failure. Generally, little attention is given to the identification of the susceptibility type. Susceptibility type can be important information, as it may help to determine and confirm that a failure is due to ESD, EOS, or processing defect or flaw that results in an infant failure.

Another reason for this difference of opinion is that there are many ESD sources. As a result, the stored energy levels and electrostatic field strengths will vary from source to source, depending on the tribocharging materials, the local physical configuration (geometry) and the operations

being performed. The probability for a catastrophic ESD event also increases for different geographical locations and weather conditions. Hot desert and very cold (below freezing) geographical areas have low humidity conditions. These conditions can result in far more charge generation than hot and humid areas or environments.

The difference of opinion discussed above may also be due in part to misconceptions about the classification methods and the lack of understanding device susceptibility. Only the sensitivity of a device is determined by present standards, not the susceptibility as is defined in this TR. The human body model (HBM) is the most popular test method for sensitivity level classification. The stored energy that results in device damage is reported as a voltage level. Voltage classifies transistors and integrated circuits (ICs) by placing them in a sensitivity class [1, 2]. The device sensitivity level can be listed as a class or it can be reported more exactly as a specific voltage level if finer stress voltage steps are used during testing. The problem is that people may believe the test method's stored energy (reported in volts) is required in practical situations to damage devices. This will be shown to be an incorrect assumption when the HBM circuit is closely examined.

Susceptible devices are different and are not differentiated by present test methods. Device classification test methods that determine the sensitivity level of susceptible devices will be discussed along with their shortcomings. A new test method standard is needed to differentiate susceptible types of devices; this TR may initiate that effort. Because there are no standard test methods to determine and identify the two susceptibility types, how to determine or obtain information about device susceptibility types is discussed.

## **Types of Susceptibility**

### Basic Susceptible Device Analogies

Susceptibility can be represented by two different damage processes, a current mode and voltage mode. A very simple analogy can be used to illustrate the two susceptibility types, and damage modes. A fine wire (like a fuse) and a wire with a small gap (gap filled with a dielectric material) can be an example for the purposes of discussing and comparing the two damage mechanisms (See Appendix Fig. 1 & 2). The fine wire represents a current mode of an energy susceptible type of device. The wire, that has a dielectric material filled gap, represents a voltage susceptible type of device. Theoretically, and in actual HBM tests, both examples can have the same sensitivity levels in terms of a reported HBM voltage sensitivity. Actually, in the HBM test or even in the case of a real world ESD event, the energy level threshold to cause device damage may be quite different.

The destruction of the thin wire depends on current and time. The instant a voltage is applied to the wire a current will flow. When the current is low, the wire temperature rises slightly. If the current is sufficiently high, the wire can melt, or in the extreme case, vaporize. The voltage versus current curve is shown in Figure 1 and is not representative of actual devices, but is shown to differential current mode failures from voltage breakdown devices. P/N junctions and other current mode devices can be nonlinear and have various turn-on voltages. It is not necessary to cover them in detail to understand the concept of the two models represented in Figures 1 & 2.

In the case of the voltage mode (wire gap), the instant a voltage is applied, essentially no current in the dielectric materials flows (the gap capacitance charging current is minuscule and neglected). An ESD voltage, or an induced voltage just below the breakdown level, will not damage the dielectric material. Still, at this point there is no current in the circuit, if we neglect

dielectric the charging current (dielectric polarization current) to keep the example simple. The instant a voltage is applied that is at or above the breakdown level, current flows, and the dielectric material is damaged. The destruction of the dielectric material is then due to current, just as it is in the wire. The trace in figure 2 shows the voltage versus current curves.

In establishing the two modes of damage, these simplified models have ignored many characteristic and things that are present in practical devices. Such issues as leakage and nonlinear currents in P/N junctions, tunneling current in very thin (Angstroms thick) gate oxides, contamination caused failure modes, etc. have to be addressed by personnel qualified in those areas. Also, very thin (Angstroms thick) gate oxides will start to conduct substantial current when voltages around 6 volts are applied to the dielectric materials. These gate oxide devices will respond like voltage susceptible devices and therefore are not susceptible to electrostatic induced voltages.

In actual devices, the end-point of a failure can be quite different, depending on the technology and the design of the device. For example, a P/N junction device may have a leakage current at a low voltage (soft knee turn on curve), be completely shorted, or open circuited. A gate oxide may also be shorted or completely open. A gate oxide may be damaged and the damage can be totally undetectable. A damaged gate may have a high leakage current, or the short may have formed and been vaporized to an open. Also, the minuscule energy that is expended during the time that there is a current that is charging the capacitance is neglected for this simple example. Essentially no energy is expended in the gap (dielectric material) until there is an avalanche of charge through the dielectric. At that onset of breakdown, the current damages the dielectric material, even if there is not sufficient energy to vaporize the material. This may result in latent damage, a latent defect or flaw. This type of damage can come from electrostatic induced voltage produced by charged surfaces, ionizers that are unbalanced, or ionizers that have a long pulse duration. [4]

For the lack of any better terminology, the two types of susceptibility in this TR will be designated as energy susceptible (ES) and voltage susceptible (VS). Although a brief generic definition is given in the Appendix, a more complete and thorough explanation is given in following sections.

### Semiconductor Susceptibility Types

Semiconductor device susceptibility can be placed into the two basic types given in the above analogy. 1.) Current driven devices are one type. These are P/N junction devices that are damaged by energy due to an excessive current. Typically, diodes and bi-polar transistors represent this type of device. 2.) Voltage driven devices are the second type. These are high impedance devices that are driven by voltage sources. Typically, they are metal oxide field effect transistors (FETs) that have voltages applied to dielectric isolated metal gates, with essentially no current. These devices are damaged by an excessive voltage that causes the dielectric material breakdown. Figures 3 and 4 are simple analogies for personnel not familiar with device characteristics.

The user may not know when one or the other, or both types of susceptibility types are present in the same device. The user may have to make this determination from the test data or data sheets. "On-chip" protected gate oxide ICs and disk drive recording heads [3] have both types of susceptible components together in the same device. "On-chip" protected ICs respond to induced voltages as if they are P/N junction devices because the protection structures at the pins generally respond that way.

The characteristics of the two types of ESD susceptible devices are discussed in more detail for technical and engineering personnel in the following paragraphs. After a more detailed discussion, it will become clear why the susceptibility type is important information for personnel working on, handling and packaging devices.

### Energy Susceptible Devices (Conductive)

A P/N junction device allows a certain amount of current of either polarity to pass through the junction without harm when certain voltage levels are reached. P/N junction devices normally operate in a current mode. A P/N junction's forward turn-on voltage is low whereas the reverse breakdown (turn-on) voltage is usually much higher. When these voltages are reached, low levels of current in both the forward and reverse direction are normal and do not harm the device. Heat is dissipated from P/N junctions during normal operation. Because damage to P/N junctions depends on the time rate of energy deposition, these types of devices are energy susceptible (ES) devices.

When the HBM voltage (stored energy) results in a sufficiently high discharge current, Joule heating damages the device because the temperature rises above a transition point. The HBM current pulse results in an energy deposition rate that is very fast, much less than a microsecond. The amount of energy, deposited in a volume of the P/N junction over a given time period, determines the temperature rise in the material.

Figure 3 presents the characteristics of a semiconductor ES device. The analogy of melting solder represents damage. The larger the solder wire size, the more energy is required to bring the volume up to the transition point melt temperature and cause the solder to flow. Melting solder or any other material is function of the energy deposited and the heat dissipated. However, for most P/N junction ESD events, the heat loss is non-existent and can be assumed to be adiabatic. That is, there is no time for heat loss.

### Voltage Susceptible Devices (Insulator)

Voltage susceptible devices can be characterized as having dielectric materials that are damaged by a voltage breakdown (punch-thru) of an insulative layer that is required for the device to function properly. The voltage breakdown of an insulative layer, such as a gate-oxide or some other insulation, starts the damage process. Figure 4 presents the characteristics of a voltage susceptible device. Since gate electrodes are isolated from the conduction channel by a dielectric material (gate-oxide), few electrons ( $e^-$ ) should normally pass through or into the oxide of an ideal device (Erasable memory cells are an exception). When no electrons (current) flow, no joule heating occurs. Gate-oxide devices are known as a metal oxide semi-conductor (MOS) field effect transistors (FETs). MOSFETs are most commonly used in integrated circuits (ICs). ICs may also have bi-polar structures on the same chip. If these devices do not have "On-chip" protection circuits, they are susceptible to excessive voltages, which can cause dielectric breakdown and subsequent damage. Therefore, these devices are referred to as voltage susceptible (VS). Small, but normal leakage currents, that meet the data specifications for the VS device, can be ignored for susceptibility type determination.

### Energy Susceptible Device Failure Modes

Energy susceptible device failures are due ESD events that produce currents, which cause Joule heating. An ESD pulse has a very short time interval (usually less than a microsecond) and the volume is generally heated adiabatically (without any conduction of heat away for the material).

During a short time period, Joule heating can occur repeatedly as long as the temperature of the device's material does not become excessively high and pass through the transition temperature of the material. (Note: Disk drive MR heads appear to be an exception, because of magnetic structural changes peculiar to the multiple thin pinned layers in computer hard drive read write heads.) If an insufficient amount of energy is deposited at a junction site, the transition temperature is not reached and there is no diffusion of the semiconductor dopant in the P/N junction so no damage occurs. When the deposited energy (Joule heating) is too high for any given time interval (due to excessive current), the transition temperature is reached and damage occurs. Joule heating may be due to an ESD or electrical overstress (EOS) event.

The transition temperature is the start of the solid liquidous (melt) phase for a given material. An ESD event that causes the peak temperature of the semiconductor material to go above the transition point will cause a failure due to disruption of the crystalline structure and diffusion of the dopant (See Appendix Fig. 5.). A P/N junction temperature can be just below the transition point repeatedly for a short time period without being damaged because, diffusion rate is a time/temperature function. P/N junctions are routinely annealed at 320 °C for 20 minutes, with some devices raised to 750°C. The 20 minute anneal is well below the silicon melting point. That allows a long heat time compared to an ESD event, which can raise the temperature to near the transition point, but it will only be there for a very short period of time without failure.

### Voltage Susceptible Device Failure Mode

A voltage susceptible device failure occurs when an excessive voltage is applied to an insulative layer. ESD damage to a gate-oxide semiconductor can only occur after the breakdown voltage level of the dielectric material is exceeded. (Note: It is possible to "wear out" dielectric below the breakdown voltage. However, that is a reliability concern and generally not relevant to ESD.) Then, as in all semiconductor devices, Joule heating occurs and causes the destruction of VS unprotected MOS devices. (Note: by unprotected device, we mean no "on-chip" protection circuit is present.)

The breakdown voltage range (window) of an ideal insulator, and many devices, is very narrow and at a very uniform value for a specific thickness. A string analogy can be used to represent the gate-oxide breakdown. Figure 4 shows the characteristics of a voltage susceptible device. When a specific force is applied to a string (small thread), two conditions may result. If the pull on the string is moderate, nothing happens. If the pull exceeds the breaking force of the string, it breaks suddenly. If a bigger, stronger string is used, the breaking point force is higher and this represents a higher gate-oxide breakdown voltage. A broken string demonstrates a voltage device's sudden failure. In an actual device, heat conduction away from the breakdown site is not a factor because the damage occurs in a very short time period, usually with much less deposited energy than P/N junctions.

In a MOS device, a damaged oxide layer can no longer insulate the metal gate electrode; therefore, the device usually fails. Very little energy is needed to damage the oxide. In some cases, the device may have a high leakage resistance, but it can still operate. If the current is severely limited or the energy source is small, an ESD event may not result in any detectable indication of an oxide failure. [4] A MOS transistor may even operate with no indication that the oxide layer has been broken down. In this case, the device has a latent defect. Latent defects have been investigated in P/N junctions, but not in gate-oxide to determine if defects become latent failures. Because the voltage breakdown window is very narrow, latent defects like this are an unlikely occurrence; but even a rare event might be a concern for high reliability devices.

Electrostatic fields, from insulated surfaces, can induce voltages across gate-oxides in devices. The induced voltage level depends many factors. It can depend on the size and amount of charge on the object. The closeness of the object to the devices and orientation with respect to the electrostatic field, also determines the coupling that results in the induced voltage. Large charged surfaces can and are capable of inducing hundreds of volts across a dielectric when the device has a very low gate capacitance. The greater the gate capacitance, the more difficult it is to raise the induced voltage to the breakdown point (See Appendix Charge Equation). A highly charged surface may arc to a device or may produce a corona discharge that cannot be seen or heard. Damage to VS devices can happen without any discharge from the charged surface.

### Protection of Voltage Susceptible Devices

"On-chip" protection circuits are designed to dissipate ESD energy and prevent a dielectric breakdown of the gate-oxide in VS devices. Figure 6A shows an IC protection circuit and a pictorial of the MOS transistor. The current versus voltage (I/V) curves for both devices are shown in Figure 6B. The P/N junction's I/V trace lies within the MOS gate-oxide breakdown voltages. The P/N diode is forward biased when the voltage is in the positive quadrant and is reversed biased when the voltage is in the negative quadrant of the curve. When the reverse bias voltage is increased, the P/N junction is said to reach avalanche breakdown. This breakdown is not destructive if the rate of energy dissipation in the P/N junction's structure is sufficiently limited and dissipated. When an HBM type of discharge or an ESD event occurs, the P/N junction is designed to protect the gate-oxide by clamping the voltage to a level that prevents gate-oxide damage. The protection circuits are very effective in protecting the VS devices from induced voltages. Most MOS devices are protected by these "on-chip" protection circuits. Some designs are as robust as 10,000 volts HBM [5 & 6].

MOS power transistors are unprotected and have large gate areas in comparison to IC gates. A large gate area has a high capacitance, which helps protect the device by keeping the voltage low for any given applied or induced charge. In contrast to MOS power transistors, a discrete field effect transistor (FET) with a low breakdown voltage and low input capacitance is more difficult to handle and protect.

The P/N and the G/D curves (Fig. 6B) show why a charged device model (CDM) type of discharge can cause ESD damage to the gate-oxide. The discharge is so rapid that the current/voltage (I/V) curve follows the dotted line. Because the P/N junction does not start conducting soon enough, the voltage reaches the gate-oxide breakdown point (the vertical dashed I/V trace). Therefore, CDM events may result in damaging interior VS devices because the protection circuits will not suppress the fast voltage pulse. The protection circuit normally dissipates the energy during an HBM event, until either or both the protection circuit and/or the protected device is damaged.

Discrete FETs with low breakdown voltages and low gate capacitances are very difficult to protect, even with the best ESD protection plan. This is why devices need to be identified in data sheets by an ES or VS designator. These VS transistors have given the impression that all devices are extremely vulnerable to electrostatic fields. This has resulted in the false impressions that maximum ESD protection efforts are always needed for all devices. Fortunately, unprotected voltage susceptible ICs are not very prevalent, and are not used in most circuit designs. Most unprotected MOS transistors are discrete devices used in special applications and may have other components on the circuit board that protect them from damage in good circuit designs. However, there is an increasing use of VS ICs in some very high-speed