

ESDA/JEDEC JTR002-01-22

ESDA/JEDEC Joint Technical Report

ESDA/JEDEC JTR002-01-22



*For the User Guide of
ANSI/ESDA/JEDEC JS-002*

*Charged Device Model Testing of
Integrated Circuits*

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FOREWORD

This technical report¹ is intended to be a complimentary document to ANSI/ESDA/JEDEC JS-002. The intention of this document is to act as a user guide for JS-002 and give the user a wealth of additional information to help them execute CDM testing within their company. This document covers some basic practical considerations such as cleaning and cable replacement and digs into more detailed discussions regarding the oscilloscope and handling charging delays. It also gives a detailed discussion on waveform verification that gives the user a clear/concise approach to completing waveform verification with waveform examples included. This is followed by guidance on the impacts of package size on the peak current, the ability to calculate the charge associated with a waveform discharge, and some practical guidance and ways to handle difficult-to-test packaging that should prove to be very helpful to the user. The final sections address some of the challenges with no-connects, the first pin tested risks, and wraps up with a discussion on reporting CDM data to the customer. The intent is to update this technical report in the future as the joint CDM WG finds new learnings, and each time ANSI/ESDA/JEDEC JS-002 is updated.

This technical report was published on July 29, 2022 and was designated ESDA/JEDEC JTR002-01-22.

¹ **Technical Report (TR):** A collection of technical data or test results published as an informational reference on a specific material, product, system or process.

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ESDA/JEDEC Joint Technical Report for the User Guide of ANSI/ESDA/JEDEC JS-002 – Charged Device Model Testing of Integrated Circuits

1.0 PURPOSE AND SCOPE**1.1 Purpose**

The information and procedures defined in this technical report are intended to help users better understand the procedures and requirements specified in ANSI/ESDA/JEDEC JS-002.

1.2 Scope

This report only covers the procedures and requirements specified in ANSI/ESDA/JEDEC JS-002.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms²

ANSI/ESDA/JEDEC JS-002, For Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM) Device Level^{2,3}

3.0 PERSONNEL SAFETY

THE EQUIPMENT SHALL NOT BE INSTALLED OR OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.

3.1 Training

ALL PERSONNEL SHOULD RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING BEFORE USING THE EQUIPMENT.

3.2 Personnel Safety

THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES, AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.

GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.

ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED, AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.

NOTE: CDM TESTERS HAVE MOVING PARTS WHEN IN OPERATION AND CARE SHOULD BE TAKEN TO AVOID PERSONNEL CONTACT WITH MOVING PARTS WHEN IN OPERATION.

² EOS/ESD Association, Inc., 218 West Court Street, Rome, NY 13440; +1 315-339-6937; www.esda.org

³ JEDEC Solid State Technology Association, 3103 North 10th Street, Arlington, VA 22201, www.jedec.org

4.0 CDM TESTER OPERATIONAL CONSIDERATIONS

4.1 Cleaning

4.1.1 Tester Cleaning

Waveform performance can be affected by contamination on any part of the test system, including the field plate dielectric, calibration targets, ground plane pogo pin, and the device under test.

Use isopropanol (isopropyl alcohol, IPA) to clean each item listed below using a procedure approved by the local safety organization and avoiding leaving any residue:

- The calibration targets should be properly stored when not in use. These should be cleaned before being used for waveform verification, using either a lint-free cloth or swab.
- The field plate dielectric should be cleaned using a lint-free cloth to ensure no fibers are left on the plate. Care should be taken when cleaning around the vacuum holes. It is best to clean this area with a swab.
- The ground plane pogo pin should be cleaned using a swab, and care should be taken to avoid damaging the pogo pin with excessive force or using too much alcohol as this may remove the lubricant within the pogo pin body.

4.1.2 Device Cleaning

Care should be taken when handling all components of the system and devices to be tested. To avoid depositing oils from your fingers on the package pins, use ESD handling practices consistent with the company's ESD handling procedures such as dissipative tweezers or vacuum wands. Direct contact between the package pins and skin should be avoided, if possible, to minimize contamination.

Devices should be cleaned with IPA and allowed to dry prior to being placed in the tester. Cleaning of the device improves waveform repeatability during CDM testing by minimizing contaminants. Use a procedure approved by the local safety organization and following internal ESD procedures. A soft brush can be used to gently clean the device terminals paying attention to avoid bending pins or removing balls. Devices should then be handled in a way that maintains cleanliness (vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers, which have been neutralized by holding in an ionized air stream). Cleaning with isopropyl alcohol may leave the surface moist for some time after the cleaning. The moisture may provide an unintended leakage path if present during the stress. It is important to dry all surfaces after cleaning, either by allowing the surfaces to dry naturally or using forced air to evaporate the moisture.

Packages with an open cavity (for example, microphones) should be cleaned with particular attention to avoid IPA leaking into the package cavity. If this cannot be done, let the package dry longer after cleaning.

NOTE: The cleaning process may be verified by stressing and measuring the peak current on several cleaned parts, comparing the same pins for peak current consistency.

4.2 Routine Versus Quarterly Checks

ANSI/ESDA/JEDEC JS-002 specifies that waveforms should be verified at least once per shift when CDM testing is performed. This does not require a full waveform verification but typically uses one verification module at the most common Test Condition planned. The verification module which most closely matches the packaged device's capacitance to the field plate should be used. However, determining the package capacitance can be time-consuming. For routine waveform verification of one Test Condition, choosing the verification module most closely aligned to the package size is reasonable. As shown in Section 7.0, if one verification module is aligned to the center of the I_{peak} range, likely, the other verification module is aligned. If there is any doubt, complete the routine verification using both verification modules. This ensures the tester and waveforms meet the required specifications, and the tester is operating within tolerances between full waveform verifications. Longer periods between routine waveform verifications are allowed. It is important to note that the longer the time between waveform verifications, the more CDM results to be in question should an issue be found during routine waveform verification.

In addition to the daily routine checks, waveform verifications should be performed quarterly or when changes are made to the system hardware or portions of the measurement chain (for example, replacing the pogo pin).

Quarterly waveform verifications are similar to routine verifications but include all Test Conditions, both polarities, and both verification modules as a requirement. It is important to record the data when performing these measurements to prove the system is within specifications.

4.2.1 Tracking Factor/Offset Settings

As current waveform amplitudes are based on the voltage factor and offset settings, it is recommended that these values be captured when performing the routine or quarterly verifications. These factor/offset settings should be reviewed. If these settings are increasing or decreasing over time, it may indicate an issue with the system.

4.2.2 Hardware Changes Requiring Waveform Verification

Many CDM test systems offer configurations to meet multiple CDM test standards. Waveforms must be verified when switching between these configurations, ensuring the tester hardware meets the given standard requirements. For example, the legacy ESDA and AEC standards used a thin insulator between the field plate and the device under test (DUT). In contrast, ANSI/ESDA/JEDEC JS-002 uses a 0.381 mm $\pm$ 0.025 mm (15 mil) thick FR4 field plate dielectric between the field plate and the DUT.

Other hardware changes, such as replacing the discharge pogo pin, require that a complete verification be performed. Pogo pins have a limited life, which may be as little as six months, depending on usage. Routine daily waveform verification may show changes in the waveforms as the pogo pin deteriorates. Changes in the shape of the waveform can be a good indication that the pogo pin needs to be replaced.

NOTE: Manufacturers' recommendations should be followed when removing and replacing a pogo pin. It is important to measure the length of the exposed portion of the pogo pin before removing it from the socket to ensure the same length can be set when installing the new pogo pin.

4.3 Holding a Package in Place, Z Height Caution

Field induced CDM testing requires the device to be in a dead bug position (upside down) on the field plate dielectric. Vacuum holes in the field plate/dielectric are used to hold the device in place during testing. However, in some cases, the device may have to be held in place or supported by a fixturing material similar to the FR4 epoxy board used for the field plate dielectric. Section 14.0, Small Package Parts and CDM, discusses the use of FR4 to hold very small devices in place during testing.

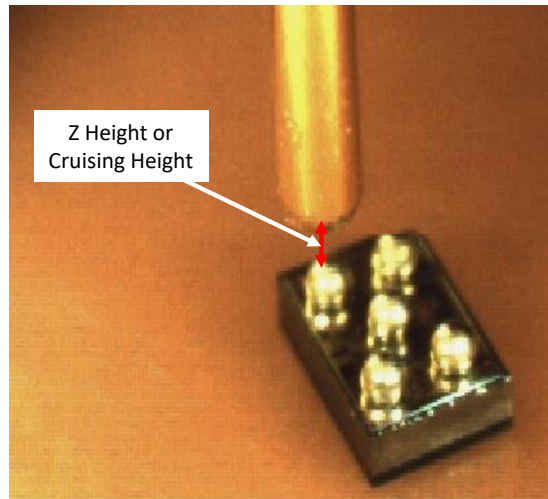


Figure 1: Relative Position (Z Height or “Cruising Height”) of the Pogo Pin to the DUT During the Movement from Pin to Pin During Testing

CDM test systems use X and Y mechanisms to position the ground (discharge) pogo pin over the pin to be tested and a Z mechanism to contact the pogo pin and the pin under test. When moving from pin to pin on the device, the pogo pin is moved away from the device, and the X and Y mechanisms position the pogo pin over the next pin to be tested. Enough space must be left between the device pins and the ground pogo pin when the X and Y mechanisms are moving to avoid hitting a pin on the device and possibly damaging the device or simply moving the device, which would require repositioning the device to continue testing.

The picture above in Figure 1 shows an example of the Z height clearance between the pogo pin and a device under test. As the BGA device has only one ball height, it is easy to set an appropriate repositioning Z height, or as it is referred to in some test systems as “cruising height”. When a device has different height pins, it is important to set this “cruising height” high enough that the pogo does not hit any pins or even the device body during the X and Y movements. The photo below in Figure 2 shows an example of a device where it would be important to set the “cruising height” properly to avoid hitting the components in the center of the grid during the X and Y movement from pin to pin.

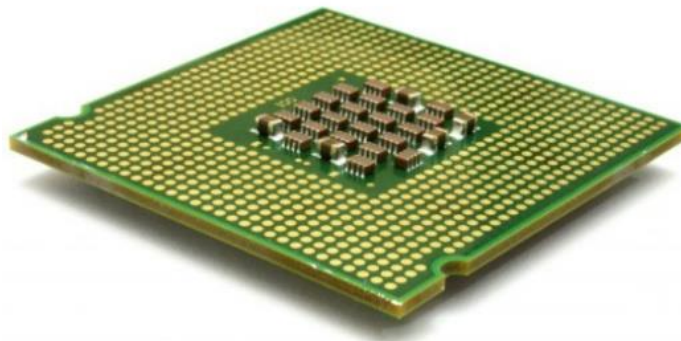


Figure 2: A Device Where the Adjustment of the “Cruising Height” Would be Critical to Avoid Hitting the Components in the Center of the Grid during Movement from Pin to Pin

4.4 Pogo Pin Tips (Round Versus Concave Versus Sharp)

The field induced waveform occurs as an air discharge, small changes in the discharge pogo pin's geometry can cause the waveforms to no longer meet the specification when performing waveform verification on the calibration targets. Although the standard does not specify using a round pogo pin, waveform parameters are based on this pogo shape. Unlike a round pogo tip, a pointed (sharp) tip changes the fields between the tip and the target and can adversely affect the waveform. Like a concave tip that may align better with a certain device pin shape, other shapes may also change the field when contacting pins of a device and subsequently change the waveform parameters.

Although device pins (contacts) have different shapes, the use of a round pogo tip keeps the electric fields more constant than a pointed or even a smaller diameter round tip. A typical standard pogo diameter is ~0.50 mm to 0.56 mm, and smaller diameters are ~0.38 mm to 0.44 mm. Full waveform verification should be done any time the pogo pin is replaced, but this is especially important if the pogo pin shape changes.

4.5 Humidity

Field induced waveforms occur as an air discharge and can be affected by many different factors, like the speed of approach, pogo tip shape, and the environment, or more precisely, the humidity levels within the test area (chamber). As humidity increases, amplitude drops, making testing at high humidity levels less stringent of a test. In addition to amplitudes being affected by humidity, repeatability is also affected by humidity levels, which are known to worsen as voltage levels decrease [1]. Although the standard specifies humidity should be less than 30% during testing and waveform verification, it is advisable to bring this level as low as possible using dry air or nitrogen brought directly into the test chamber. A small humidity meter placed inside the system can help determine the proper soak time for the desired humidity target level.

4.6 Cable Connections

The standard specifies the use of high bandwidth cables and components (connectors and attenuators) to ensure the best waveform performance and measurement integrity. For 6 GHz measurements, attenuators with a bandwidth of at least 12 GHz are recommended. The use of higher bandwidth components during all measurements further ensures measurement integrity.

Each added connector connection can introduce reflections on the discharge waveforms. For this reason, it is important to limit the number of connections and ensure the connections are tight using a torque wrench that uses the necessary force required to ensure the connections are tight without damaging the connectors. Most systems use SMA connectors, and torque wrenches are available for these connector types.

4.7 1-Ohm Current Sensing Resistance Measurements

The 1-ohm current sensing resistor is part of the discharge chain when performing CDM testing. Therefore, the resistance value must be correctly measured and known to compensate for peak current offset or to detect resistor degradation, which leads to changes in the shape of the discharge pulse.

Two-probe digital multimeters are not accurate enough to measure the 1-ohm current sensing resistor with an accuracy of 0.01 ohm (ANSI/ESDA/JEDEC JS-002, per Section 5.5 standard); therefore, Kelvin 4-wire connections should be used. Using Kelvin 4-wire connections, the current is supplied via a pair of force connections (Force High (FH) and Force Low (FL)) while the sensing pair (Sense High (SH) and Sense Low (SL)) connections measure the voltage across the resistor. The advantage of using the Kelvin 4-wire approach is that the voltage drop in the sense pair is negligible compared to the force pair, making a low ohmic resistance measurement. Figures 3a and 3b show the set-up for the 1-ohm current sensing resistance measurement using a Kelvin 4-wire approach. The 1-ohm current sensing resistor should either be terminated by the 50-ohm input of an oscilloscope or by a 50-ohm termination.

The following items should be taken into consideration to maximize the accuracy of the 1-ohm current sensing resistor measurement:

- Use of the maximum number of digits
- Slowest AC filter to increase accuracy
- The highest range for the number of power line cycles to increase accuracy
- Offset compensation to reduce or eliminates thermal electromotive force
- Warm-up time according to the resistance meter manual
- Measurement range (lower current ranges minimize self-heating of the 1-ohm current sensing resistor, but higher current ranges improve the accuracy of the measurement)

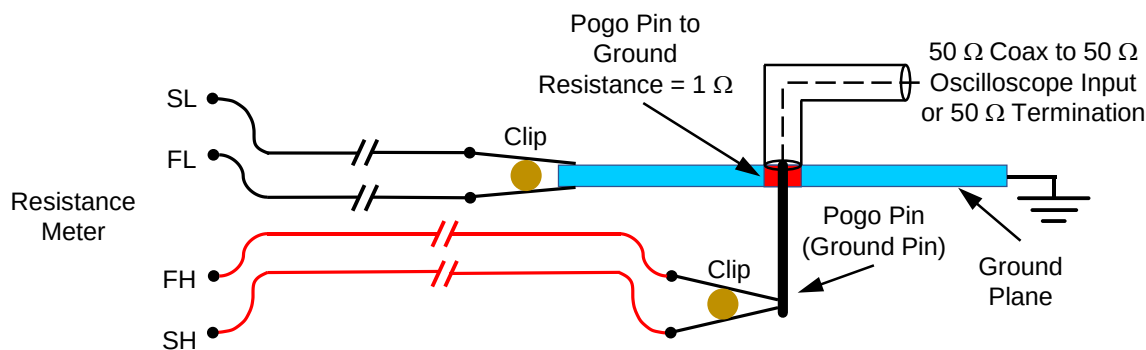


Figure 3a: Kelvin 4-Wire Resistance Measurement 1-Ohm Current Sensing Resistor Setup

NOTE: SL – Sense Low connection, SH – Sense High connection, FL – Force Low connection, FH – Force High connection



Figure 3b: Connection of the Kelvin 4-Wire Clips to the 1-Ohm Current Sensing Resistor Setup

Figure 4 shows the measurement accuracy influence for different types of ohmmeters versus applied current for two types of source measurement units (SMU, Keithley 2400 and 2450 – note equivalents are acceptable), a 6½ digit bench multimeter (Keysight 33401A or equivalent), and two handheld multimeters (Metra Hit/27M and Fluke 289 or equivalent). For the calculation, the specified measurement accuracy ($\pm$ (% of reading + % of full scale) expressed in ohms) for each type of ohmmeter has been calculated for the 1-ohm resistor measurement. Using a Keysight 33401A bench multimeter, the best accuracy is obtained with the lowest applied measurement current and minimizing the risk of self-heating of the 1-ohm current sensing resistor during the measurement, see Figure 4. The same accuracy can also be obtained with one of the SMU's when the current is increased by a factor of 100 compared to the Keysight 33401A bench multimeter with the risk of self-heating.

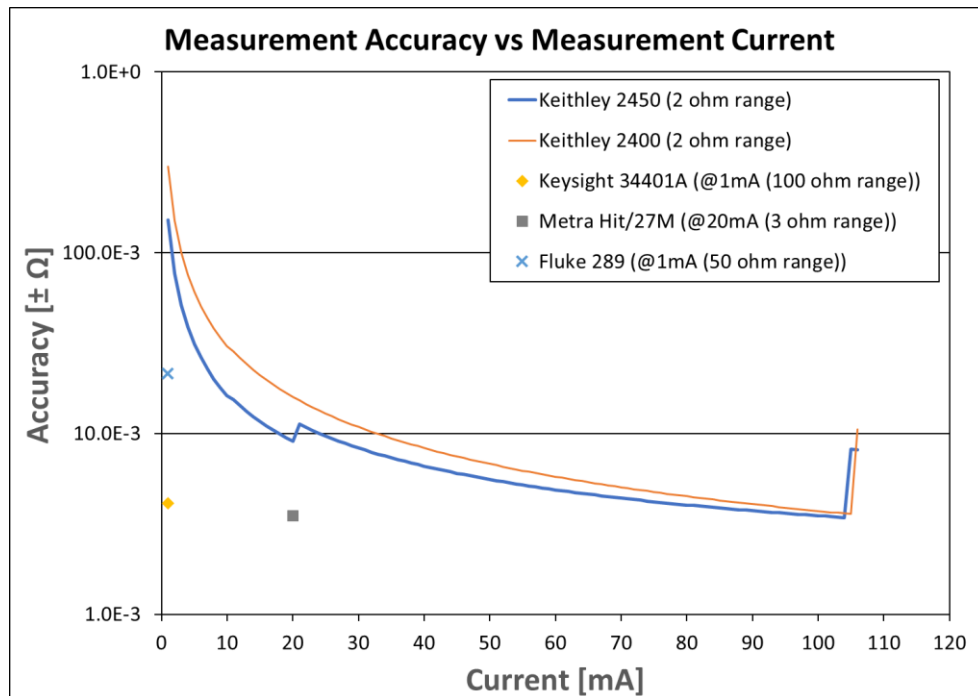


Figure 4: Calculated Measurement Accuracy Versus Measurement Current for Different Types of Ohmmeters when Measuring a 1-Ohm Current Sensing Resistor

NOTE: The Keysight 34401A, Metra Hit/27M, and Fluke 289 have a fixed range measuring a 1-ohm resistor.

NOTE: Accuracy is improved with lower readings on the above Y-axis – ideally, the measurement accuracy of less than 10^{-3} ohm is desired.

NOTE: Measurement accuracy = $\pm$ (% of reading + % of full scale) expressed in ohms.

5.0 OSCILLOSCOPE EFFECTS - SETTINGS

5.1 Metrology Concerns

Four metrology considerations need to be understood when setting up to capture and analyze CDM waveforms.

- Proper cabling and attenuator selection
- Proper oscilloscope selection
- Oscilloscope variation concerns
- Proper data capture and analysis

5.2 Proper Cabling and Attenuator Selection

Due to the nature of the CDM waveforms, with very fast rise times and short durations, all the items within the metrology chain must be of good quality and have the proper bandwidth to minimize questions or concerns during waveform verification or actual device testing.

Cables, attenuators, and bandwidth filters should be chosen to meet the calibration requirements of ANSI/ESDA/JEDEC JS-002, which means they should have a minimum bandwidth of at least 12 GHz. However, it is advisable to have even higher bandwidths to provide the best accuracy. Many of today's SMA coax cables and attenuators are available with a bandwidth of 18 GHz.

An important item within the metrology chain is the coax connectors and adapters being used. High quality, high bandwidth connectors/adapters, preferably SMA style, should be used. It is also very important that "all" connections be tight to avoid any noise or reflection issues caused by a bad connection.

5.3 Proper Oscilloscope Selection

Although the standard allows the use of a 1-GHz oscilloscope for daily waveform verification, it is best to use a higher bandwidth oscilloscope for these measurements.

If a 1-GHz oscilloscope is to be used for daily verification, it is important to capture reference data on the intended 1-GHz oscilloscope after the system has been calibrated using an oscilloscope with a 6 GHz or higher bandwidth. Waveforms captured during the daily 1-GHz verification can then be compared to the reference data to see if waveforms have changed. See ANSI/ESDA/JEDEC JS-002.

Another issue to be aware of is that some modern oscilloscopes specify a minimum bandwidth. In other words, an oscilloscope specified at 1-GHz may have a bandwidth of 1.1 GHz or 1.2 GHz. The bandwidth can change depending on the vertical setting of the oscilloscope or the number of channels used, complicating matters even more. The same models may have different bandwidths but meet the 1-GHz minimum specification. This small change in bandwidth can be enough to put the waveforms out of specification levels, as discussed in [2]. The simple guidance is that if a 1-GHz oscilloscope is used for routine waveform verification, the same oscilloscope and the same oscilloscope channel should always be used.

5.4 Oscilloscope Variation Concerns

Oscilloscopes available today offer two different types of frequency response, either a Gaussian or maximally-flat response. Most oscilloscopes with bandwidth specifications of 1 GHz and below typically have a Gaussian response, while oscilloscopes with bandwidth specifications greater than 1 GHz typically have a maximally-flat frequency response. When measuring near the bandwidth limits, where most CDM measurements are made, maximally-flat response oscilloscopes always provide a higher amplitude waveform than an oscilloscope using a Gaussian response, resulting in faster rise times and shorter pulse widths. These differences can cause a waveform to be in spec on one oscilloscope and out on another.

Figure 5 shows the difference in the frequency magnitude response for an oscilloscope with a Gaussian response and one with a maximally-flat response.

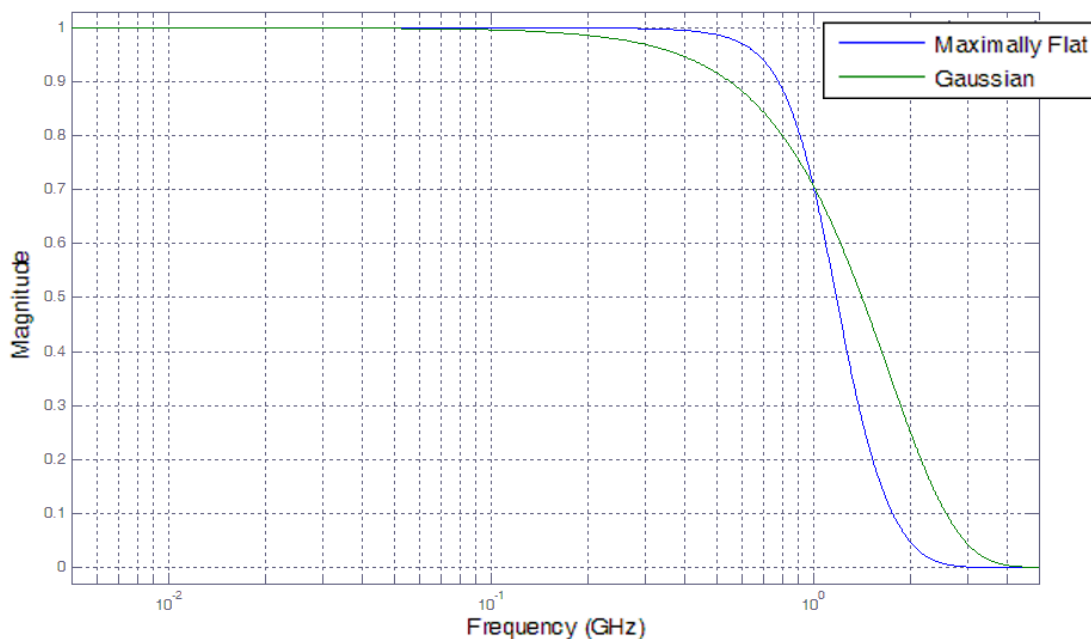


Figure 5: Magnitude Response for Gaussian and Maximally-Flat Filters

Another concern with oscilloscopes is the way the oscilloscope internally limits bandwidth. If an oscilloscope's bandwidth must be limited to meet the requirements of a 1-GHz waveform, it is best to use a low pass filter in front of the oscilloscope in addition to any attenuators being used. This would be important when a 2- to 4-GHz oscilloscope is being used and must be reduced to 1-GHz capability to meet specifications. The filter should be a Gaussian non-reflective type. However, as is recommended in ANSI/ESDA/JEDEC JS-002, an oscilloscope with a bandwidth of ≥ 6 GHz should be used whenever possible to minimize any clipping of the peak current (I_p).

5.5 Proper Data Capture and Analysis

The current sensor is a 1-ohm resistor in parallel with a 50-ohm cable connected to the oscilloscope. The resistor itself is allowed to be 10% higher or lower than the target value. Therefore, it is important to consider the actual resistor value when determining the waveform's true peak current from the oscilloscope readings. The oscilloscope capture points should be corrected by dividing them by the parallel between 50 ohms and the real resistance value measured as suggested in Section 4.7.

Oscilloscope sample rate plays a fundamental role in data analysis; commercially available 6-GHz oscilloscope sample rates range from 20 Gs/s to 60 Gs/s. A 20-Gs/s sample rate describes a 200-ps rise time waveform with a maximum of four points; this reduced rise time resolution may affect the minimum value of the acquired rise time, making the waveform parameter analysis more difficult.

Another consideration should be done on vertical scale settings. High-speed digital oscilloscopes usually have a limited resolution, typically eight bits in the single-shot mode used during CDM waveform capture. It is important to adjust the measurement range and offset of the oscilloscope to best use the available resolution. The gain and offset controls should be chosen to obtain close to a full-scale waveform without clipping the waveform. However, the use of "fine vertical scale" should be avoided because this adjustment may create a better-looking waveform on the screen but does not improve the measurement resolution.

Correct attenuator choice is also fundamental for low voltage stress and tiny ICs: a small vertical scale is generally noisier than the others and should be used only when needed. Attenuator choice should consider the maximum input voltage to avoid damage on the first input stage.

6.0 DETERMINING IF A CHARGE TIME (DELAY) IS NEEDED

With larger packaged units, it may be necessary to add additional charge time (delay) into the CDM tester to ensure the product under test received a full charge before discharge. This typically starts to become an issue when the package size exceeds 500 mm² when a charging resistor of approximately 100 megohms is installed but can also occur at lower package sizes if this charging resistor is larger. It is recommended that each new large package (> 500 mm²) tested on a CDM tester for the first time go through this procedure to ensure the delay has been set properly.

NOTE: Charge time (delay) is the amount of time the device is allowed to charge – any added time is added to the default in most cases

NOTE: Discharge time (delay) is the amount of time that the pogo pin remains in contact with the pin under test – any added time is added to the default in most cases

6.1 Procedure for Determining if a Charge Time (Delay) is Needed

The procedure below can be used to determine if a charging delay is needed. It is recommended to run this evaluation using a primary GND or VSS pin on the package.

1. Set the field plate voltage at +250 volts. Any voltage can be used as the objective is to monitor the peak current (I_p). However, voltages lower than 250 volts should be avoided due to I_p stability, and higher voltages should only be used if the product can tolerate it without being damaged.
2. With the charge time (delay) set to 0 ms, collect ten waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

3. With the charge time set to 500 ms, collect ten waveforms, record the I_p from each. Calculate the average I_p of the waveforms.
4. Compare the average I_p value from the charge time of 0 ms and the charge time measurement at 500 ms. If the average I_p for the charge time of 0 ms is at least 95% of the average I_p for the charge time of 500 ms, then the package to be tested has a capacitance small enough not to require an added delay. If the average I_p for the charge time of 0 ms is less than 95% of the average I_p for the charge time of 500 ms, refer to the procedure below to determine the appropriate charge time to ensure the device receives a full charge.

The procedure below can be used for characterizing the charge time on the CDM tester and determining the appropriate charge time (delay) for full charging. The below procedure is used if step 4 above determines that the I_p value does not align between the 0 ms and 500 ms comparison.

6.2 Procedure for Setting Charge Time (Delay)

Typically, the primary GND or VSS bus of a product is reasonably robust when zapped at + 250 volts and can be used as a good reference point when setting up for this procedure. However, any pin can be used that the user believes would not be damaged by the discharge at the set voltage. The below procedure's objective is to characterize the I_p at various charge time points, focusing on looking for a point where the I_p saturates (no longer increases in value). The charge time setting corresponding to the point at which the I_p saturates would be the minimum delay that should be set. It is recommended to be conservative and add 50 ms to 100 ms to the determined delay value.

Follow the procedure below, using the identified pin on the package under consideration, to determine an appropriate charge time (delay):

1. Set the field plate voltage at + 250 volts (any voltage can be used as the objective is to monitor I_p).
2. With the charge time (delay) set to 0 ms, collect ten waveforms and record the I_p from each. Calculate the average I_p of the waveforms.
3. Increase the charge time (delay) by 50 ms, collect ten waveforms, record the I_p from each, and calculate the average I_p .
4. Continue incrementing the charge time by 50 ms (a larger or smaller step can be chosen) and record the average I_p until a minimum of 500 ms charge delay.
5. Plot the results, as shown below in Figure 6.
6. The appropriate charge time (delay) results in a "saturation point" for the I_p . As shown below in Figure 6, the I_p for this example saturates at just over 5.4 amperes at 300 ms. Adding some guardband to this example would set a charge time (delay) of 350 ms – 400 ms as the required charge time (delay) on this example package device.
7. It is expected that 500 ms or less is sufficient to reach a saturation point for most large devices. However, if after 500 ms, a saturation point has not been reached, repeat steps 4 & 5 until this occurs.
8. It is important to note that longer charge times do not "overcharge" the device but would only increase test time, so balancing charge time (delay) is important to minimize the overall test time.

NOTE: To avoid the risk of not fully discharging the device, it is a good practice to set the discharge time (delay) to align with whatever charge time (delay) was determined in the above procedure.

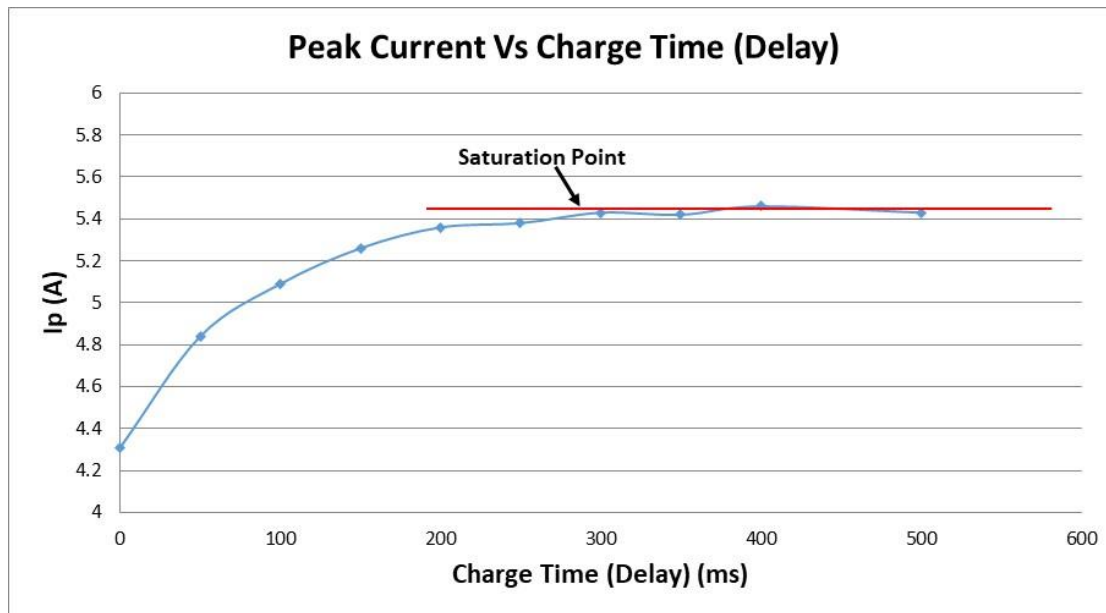


Figure 6: Example Characterization of Charge Time (Delay) Versus I_p

7.0 WAVEFORM VERIFICATION PROCEDURE – FACTOR/OFFSET

7.1 Factor/Offset Adjustment Method

This procedure aligns the tester for direct software voltage input of the Test Condition (TC) for the full alignment range. This method may not allow for alignment of each Test Condition with the target mid-range of I_p , as shown in Tables 1 or 2 of ANSI/ESDA/JEDEC JS-002. However, it is the easiest to use in a lab environment with multiple testers because the software voltage entered matches the Test Condition target level. It also does not require linear interpolation/extrapolation for Test Conditions other than the five levels listed in Tables 1 or 2 of ANSI/ESDA/JEDEC JS-002.

Though Table 1 (1-GHz target levels) of ANSI/ESDA/JEDEC JS-002 could be used for this, it is highly recommended to use the Table 2 values (> 6-GHz values) of ANSI/ESDA/JEDEC JS-002. It is well documented [2] that the variation in 1-GHz oscilloscopes can create another error source in verifying and setting the waveform targets. High bandwidth oscilloscopes eliminate this source of I_p clipping and are the recommended method for completing all waveform verifications. This approach of using the high bandwidth oscilloscope is used throughout this user guide.

Using the factor/offset feature available on many CDM testers adjusts the field plate voltage based on the software's target voltage (software voltage). This adjustment allows a user to always enter the Test Condition target with the system adjusting the field plate voltage to hit the target I_p .

The requirements/details of this factor/offset adjustment method are as follows:

- A single factor/offset is used across the entire Test Condition range. In other words, the user must determine a single factor/offset value that can be used across the full set of TCs, which typically means there is some compromise with trying to hit the mid-point of the range across all 5 TCs.
- A different factor/offset can be used for each polarity. Most CDM test systems allow a separate adjustment for positive and negative voltages, typically the same value for factor/offset can be used for both polarities, but both polarities must be checked.
- The same factor/offset must be used for both large and small verification modules.

The pros/cons of this approach are listed below:

- Pros
 - Easiest to use in a lab with many testers as the target TC voltage is entered in the user's software. Therefore, the system user can avoid determining unique field plate voltages values to enter for each TC but can enter the target voltage aligned with each TC (for example, entering a software voltage of 250 volts for TC 250).
- Cons
 - Ip may not align to the center of the Ip range for each Test Condition. Since a fixed factor/offset must be used across all 5 TCs, it is typically expected that the user does not achieve the mid-point of the target range for every TC. This could be done, but the effort required would not make the use of this approach very practical.

Figure 7 shows the full qualification or quarterly flow check required to follow the requirements specified in ANSI/ESDA/JEDEC JS-002. This section of the user guide steps the user through this flow, step by step, to help better understand what is expected of the user. Note that while the flow in Figure 7 shows completing the large or small verification module first, then completing the other, any combination of checking the large and small verification module is acceptable as long as all TCs are completed for both verification modules and the requirements listed previously for this adjustment method are met.

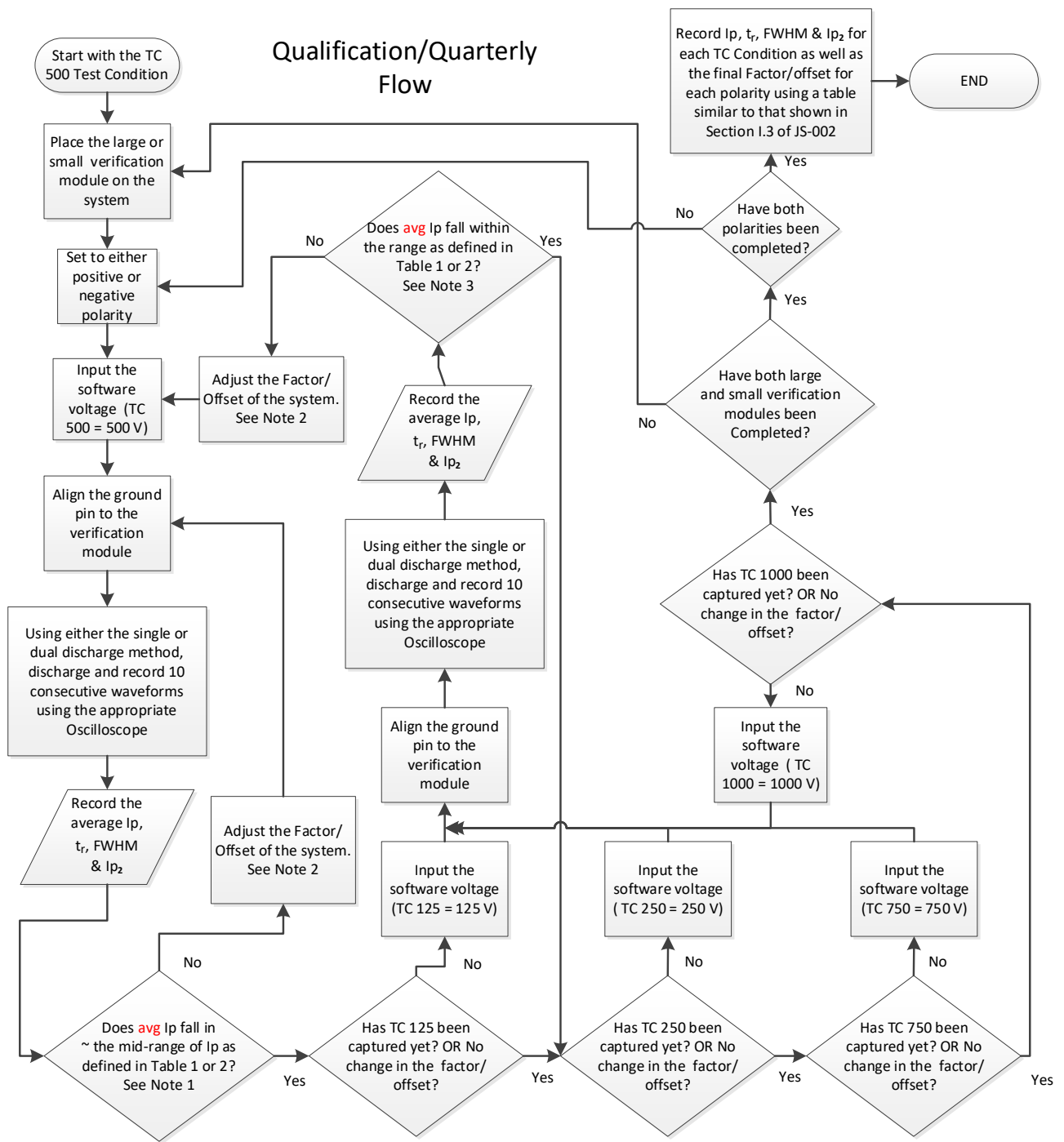


Figure 7: Example Waveform Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

NOTE 1: Targeting the mid-range of TC 500 is a starting point for adjusting the field plate voltage. Based on the results of the other Test Conditions (TC 125/250/750/1000), the I_p may end up higher or lower than the mid-range value on TC 500. Adjustments in the factor/offset may shift the I_p higher or lower, as shown in Figures 8 and 9.

NOTE 2: To properly calibrate systems, tester manufacturers have implemented a secondary “adjustment” parameter as an offset from the software voltage setting, either represented as a voltage “multiplier” value or a percentage “offset” value, which modifies the field plate voltage. Consult the tester manufacturer for more detail.

NOTE 3: After several iterations through this loop, if the user finds they cannot meet the I_p range as defined in Tables 1 or 2 of ANSI/ESDA/JEDEC JS-002, or the factor/offset is outside the typical documented range, re-clean the verification modules and pogo pin and check that all connections are tight. If this still does not work, check the system vacuum, or replace the pogo pin. Consult the tester manufacturer for more information.

7.2 Factor/Offset Adjustment Impacts

Before proceeding into the verification process detail, it is necessary to review some background on how the factor or offset impacts the shape of the I_p curve as a function of the voltage setting. The actual field plate voltage is modified by multiplying the factor by the software voltage setting by adjusting the factor. For example, a software voltage setting of 500 volts would result in a field plate voltage of 450 volts with a factor of 0.9. As shown in Figure 8, the center curve (in red) depicts a typical I_p versus software voltage setting. If we assume the center curve depicts a situation in which the factor equals one, as the factor is adjusted lower, the actual slope of the I_p versus software voltage curve becomes shallower.

Consequently, as the factor is adjusted higher, the slope of the I_p versus software voltage curve becomes steeper. Adjusting the factor is the most typical way to ensure meeting the target levels.

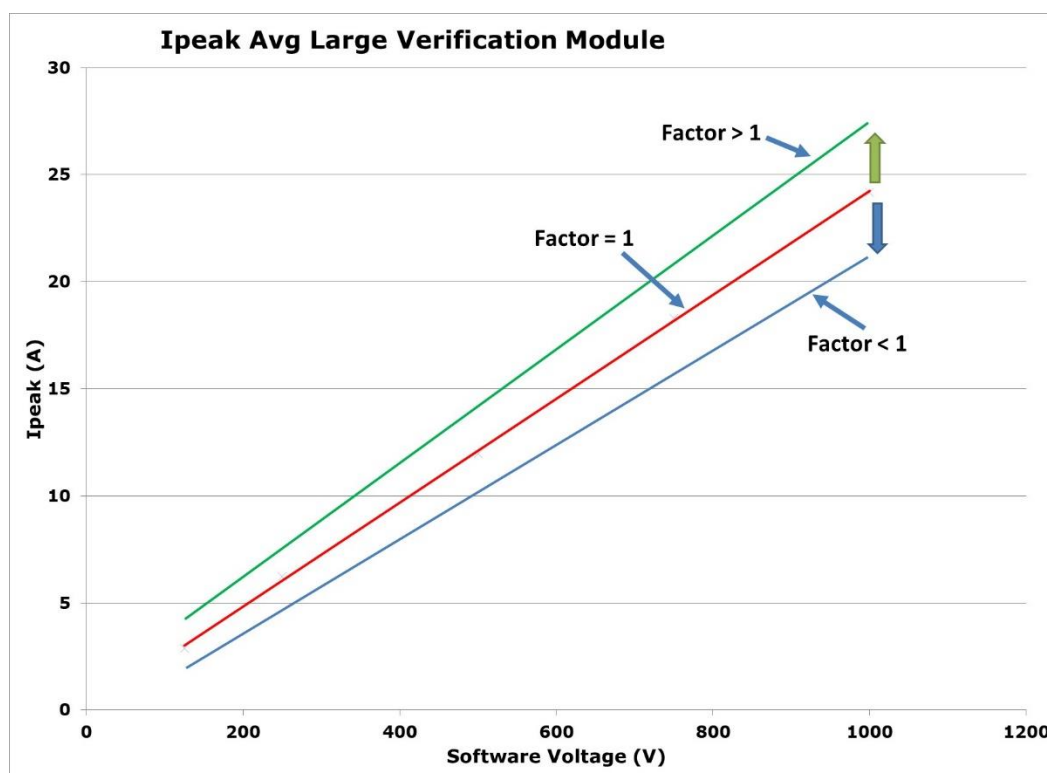


Figure 8: Example of the Impact of Factor Adjustment on the Average I_p for the Large Verification Module – High Bandwidth Oscilloscope

Additionally, some CDM ESD testers offer a second way to adjust the I_p versus voltage curve. This is known as the offset. By adjusting the offset, the actual field plate voltage is modified by adding the offset to the software voltage setting. For example, a software voltage setting of 500 volts would result in a field plate voltage of 450 volts with an offset of -50 volts. Note that the offset can be

either a positive or negative value. As shown in Figure 9, the center curve (in red) depicts a typical I_p versus software voltage setting. If we assume the center curve depicts a situation in which the offset equals zero, as the offset is set below zero, the actual curve of the I_p versus software voltage curve is lowered with no change in the slope. Consequently, as the offset is increased above zero, the I_p versus software voltage curve is raised with no change in the slope. Adjusting the offset can be used for finer adjustments and can help meet the TC 125 condition's tighter range. Note that if offset is used to make adjustments at higher Test Conditions, it does pose a risk of creating too large an adjustment for TC 125 and lower Test Condition settings.

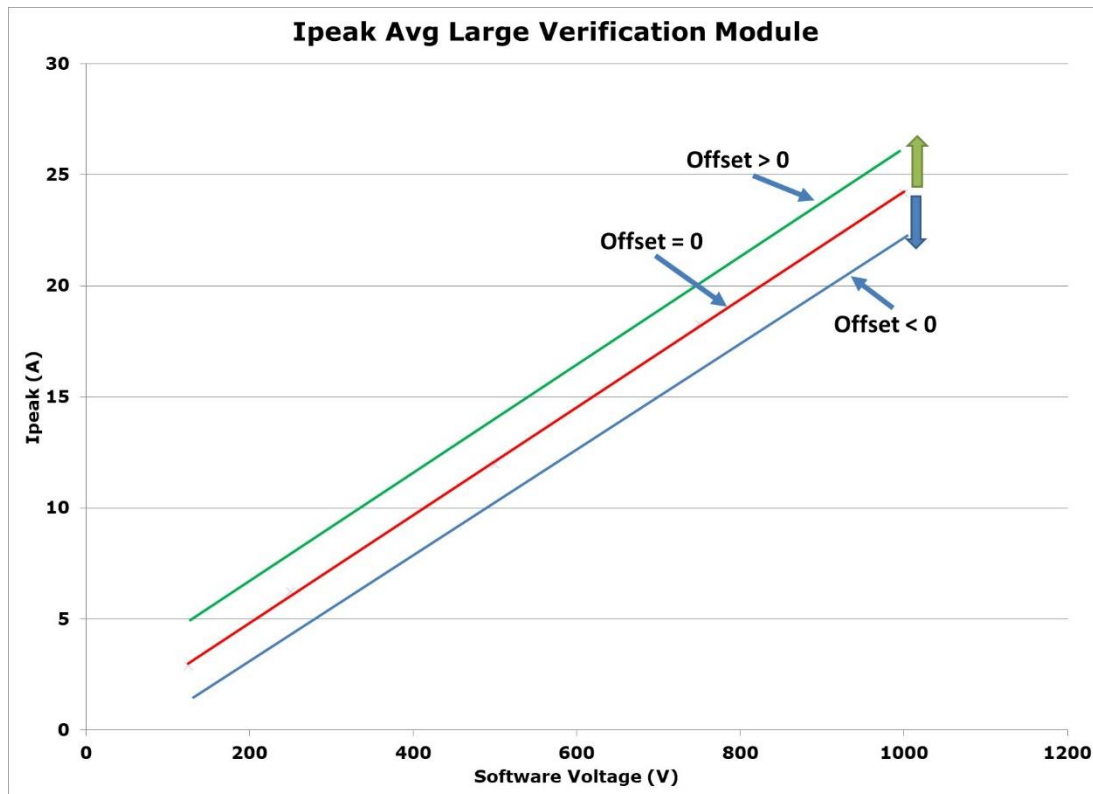


Figure 9: Example of the Impact of Offset Adjustment on the Average I_p for the Large Verification Module – High Bandwidth Oscilloscope

7.3 Factor/Offset Adjustment Method Details

7.3.1 Positive Polarity Waveform Verification

Figure 10 breaks out the first leg of the flow chart shown in Figure 7 and focuses on just the first check at TC 500. The check can start with any TC, and experience on a CDM tester may find that a different TC is best to start with (for example, starting with the TCs most often used for product qualifications and ensuring these are best aligned to the center of the target range). However, for this example, the user guide follows the flow shown in Figure 7 and starts with TC 500.