



## **Global A CGI/TSI Physical Layer Device Test Specification**

### **1 Introduction**

**Note:** Nothing in this standard supercedes applicable laws and regulations.

**Note:** In the event of conflict between the English and domestic language, the English language shall take precedence.

**1.1 Scope.** This specification leads testing of the Physical Layer (PL) of Controller Area Network (CAN) Graphic Interface (CGI) Touch Screen Serial Interface (TSI), i.e., CGI/TSI, Bus devices.

**1.1.1** Electro Magnetic Compatibility (EMC) and Electro Magnetic Interference (EMI) testing is not described in this document, except crank pulse and Electro Static Discharge (ESD).

**1.1.2** The measurement results shall be documented in the separate available CG3704 Global A CGI/TSI Physical Layer Test Result Template, all plots included.

**1.1.3** Parameters are given as nominal values unless otherwise noted.

**1.1.4** All tests and test methods shall be executed if not otherwise stated.

**1.2 Mission/Theme.** This specification applies to only GM vehicles using CGI/TSI Bus devices.

**1.3 Classification.** Not applicable.

### **2 References**

**Note:** Only the latest approved standards are applicable unless otherwise specified.

#### **2.1 External Standards/Specifications.**

ISO 11898

#### **2.2 GM Standards/Specifications.**

GMW3059

GMW3097

GMW3122

#### **2.3 Additional References.**

- CG3704 Global A CGI/TSI Physical Layer Device Test Specification Test Result Template

### **3 Test Preparation and Evaluation**

#### **3.1 Resources.**

**3.1.1 Calibration.** The test facilities and equipment shall be in good working order and shall have a valid calibration label.

**3.1.2 Alternatives.** Alternative test facilities and equipment may also be used. However, all measuring variables as specified in this standard shall be determined correctly with respect to their physical definition.

**3.1.3 Facilities.** A room with controlled temperature and humidity and a hot/cold chamber.

**3.1.4 Equipment.** The test equipment must fulfill GMW3122 requirements for High Speed testing.

**3.1.5 Test Vehicle/Test Piece.** As specified by the required tests.

**3.1.6 Test Time.**

Calendar time: 20 days  
Test hours: 120 hours  
Coordination hours: 40 hours

**3.1.7 Test Required Information.** As specified by the required tests.

**3.1.8 Personnel/Skills.** Skilled in using electrical measurement equipment, e.g., voltage and resistance meters and digital storage oscilloscopes (DSO). Familiarity with hot/cold chambers.

**3.2 Preparation.** As specified by the required tests.

**3.3 Conditions.**

**3.3.1 Environmental Conditions.** Unless otherwise specified in the test description the following environmental parameters shall be used for the tests:

- Room Ambient Temperature 23 °C
- Room Ambient Humidity 50% ± 20%

**3.3.2 Test Conditions.** Deviations from the requirements of this standard shall have been agreed upon. Such requirements shall be specified on component drawings, test certificates, reports, etc.

**3.3.2.1 Supply Voltage.** Unless otherwise specified in the test description the supply voltage shall be 14 V ± 0.1 V.

**3.3.2.2 R<sub>1</sub> and R<sub>2</sub> Values.** The nominal values R<sub>1</sub> and R<sub>2</sub> of the Dual Wire CAN bus termination resistors for the test setups shall be as follows:

- Regular Bus termination: 60 Ω to 62 Ω
- Central Bus Termination: 30 Ω to 32 Ω

**3.4 Instructions.** As recorded in Section 4.

**3.5 Data.** As required in Sections 3.7.1 and 4.

**3.6 Safety.** This standard may involve hazardous materials, operations, and equipment. This standard does not propose to address all the safety problems associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

**3.7 Documentation.** Samples of components or material released to this standard shall be tested for conformity with the requirements of this standard and approved by the responsible GM Department prior to the start of delivery of production level components or materials.

Any change to the component or material, e.g., design, function, properties, manufacturing process and/or location of manufacture requires a new release of the product. It is the sole responsibility of the supplier to provide the customer, unsolicited, with documentation of any change or modification to the product/process, and to apply for a new release.

If not otherwise agreed to, the entire verification test shall be repeated and documented by the supplier prior to start of delivery of the modified or changed product. In some cases, a shorter test can be agreed to between the responsible GM department and the supplier.

**3.7.1 Test Results.** The measurement results shall be documented in the separately available CG3704 CGI/TSI Physical Layer Device Test Specification Test Result Template, all plots included.

**3.7.1.1 General Guidelines for Completing the CGI/TSI Physical Layer Device Test Specification Test Result Template.**

**3.7.1.1.1** Read the Global A CGI/TSI Physical Layer Device Test Specification before performing the tests. This test results template does not include any test descriptions.

**3.7.1.1.2** The supplier shall use CG3704 Test Result Template and not a different format.

**3.7.1.1.3** The test results shall be entered using the same word processing tools as General Motors (GM).

**3.7.1.1.4** The Supplier shall not change the acceptance criteria.

**3.7.1.1.5** All tests shall be performed. If a test is not possible or not applicable, the Supplier shall name the reason why the test was not performed.

**3.7.1.1.6** The Supplier shall enter the actual result of the test in the "Test Result" column, e.g.,  $V_{\text{Resume}} = 6.2 \text{ V}$ , and not simply OK, NOK or even nothing.

**3.7.1.1.7** Plots of the signal waveforms and delay measurements shall be added to the test report for all test cases.

**3.7.1.1.8** Additions to the test results, e.g., plots and CAN traces, shall be inserted directly after the respective paragraph.

## 4 Requirements and Procedure

### 4.1 Physical Layer (Dual Wire High Speed CAN Bus).

#### 4.1.1 CGI/TSI Bus Output Voltage Levels.

**Note:** Refer to Figure A3 in Appendix A for an example of CGI/TSI Bus Output Voltage Levels.

##### 4.1.1.1 Recessive Output Voltage Levels.

**Scope** Measure the CGI/TSI bus output voltage levels in recessive state and check whether they meet the requirements of the General Motors Local Area Network (GMLAN) Physical Layer specification GMW3122.

**Conditions** The test circuit according to Figure 1 shall be used.

**Test Method** Measure the absolute and differential voltage levels of the  $\text{CAN}_\text{H}$  and  $\text{CAN}_\text{L}$  line. In addition, measure the common mode bus voltage  $V_{\text{CM}}$ .  
Add oscilloscope plots to the test report showing  $V_{\text{CAN}_\text{H}}$ ,  $V_{\text{CAN}_\text{L}}$  and  $V_{\text{diff}}$ .

$$V_{\text{diff}} = V_{\text{CAN}_\text{H}} - V_{\text{CAN}_\text{L}}$$

$$V_{\text{CM}} = 0.5 (V_{\text{CAN}_\text{H}} + V_{\text{CAN}_\text{L}})$$

**Acceptance Criteria** See Table 1.

**Table 1: Recessive Output Levels of the Electronic Controller Unit (ECU) according to GMW3122**

| RECESSIVE STATE                 |                           |         |         |         |
|---------------------------------|---------------------------|---------|---------|---------|
| Parameter                       | Notation                  | Value   |         |         |
|                                 |                           | Minimum | Nominal | Maximum |
| Output bus voltage              | $V_{\text{CAN}_\text{H}}$ | 2.0 V   | 2.5 V   | 3.0 V   |
| Output bus voltage              | $V_{\text{CAN}_\text{L}}$ | 2.0 V   | 2.5 V   | 3.0 V   |
| Differential output bus voltage | $V_{\text{diff}}$         | -120 mV | 0 V     | 12 mV   |
| Common mode bus voltage         | $V_{\text{CM}}$           | 2.25 V  | 2.5 V   | 2.75 V  |

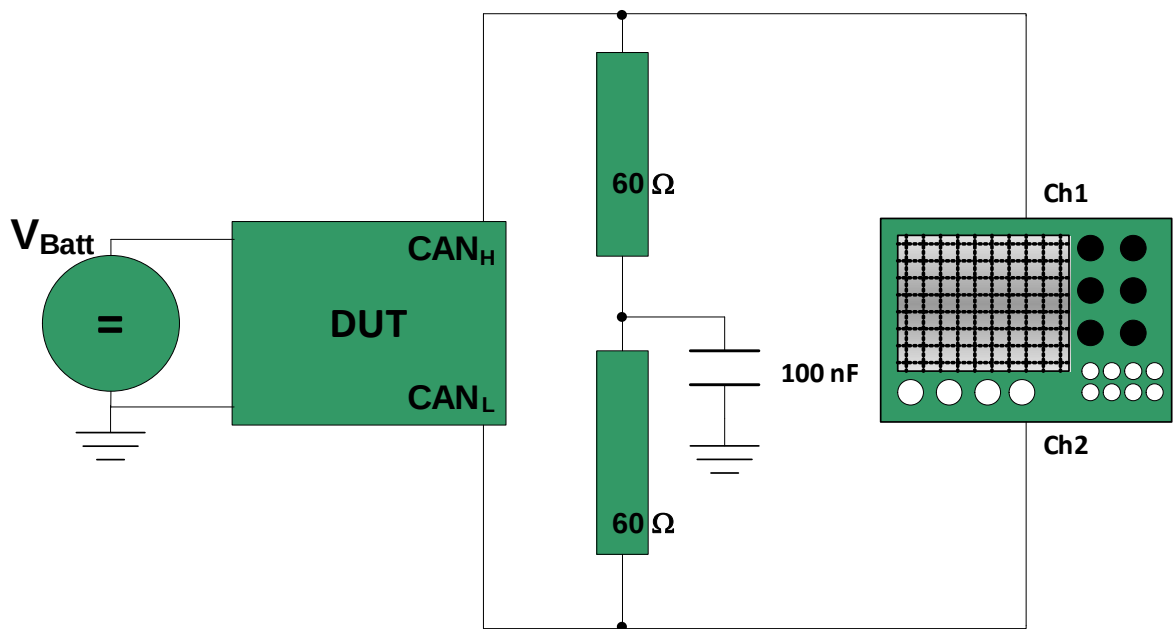


Figure 1: CGI/TSI Bus Test Setup

#### 4.1.1.2 Dominant Output Voltage Levels.

|                     |                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope               | Measure the CGI/TSI bus output voltage levels in dominant state and check whether they meet the requirements of the GMLAN Physical layer specification GMW3122.                                                                                                                                                                                                                 |
| Conditions          | The test circuit according to Figure 1 shall be used.                                                                                                                                                                                                                                                                                                                           |
| Test Method         | <p>Measure the absolute and differential voltage levels of the CAN<sub>H</sub> and CAN<sub>L</sub> line. In addition, measure the common mode bus voltage V<sub>CM</sub>.</p> <p>Add oscilloscope plots to the test report showing V<sub>CAN_H</sub>, V<sub>CAN_L</sub> and V<sub>diff</sub>.</p> $V_{diff} = V_{CAN\_H} - V_{CAN\_L}$ $V_{CM} = 0.5 (V_{CAN\_H} + V_{CAN\_L})$ |
| Acceptance Criteria | See Table 2.                                                                                                                                                                                                                                                                                                                                                                    |

Table 2: Dominant Output Levels of the ECU according to GMW3122

| DOMINANT STATE              |              |                              |         |                              |
|-----------------------------|--------------|------------------------------|---------|------------------------------|
| Parameter                   | Notation     | Value                        |         |                              |
|                             |              | Minimum                      | Nominal | Maximum                      |
| Output bus voltage          | $V_{CAN\_H}$ | 2.75 V<br>(preferred: 3.0 V) | 3.5 V   | 4.5 V<br>(preferred: 4.25 V) |
| Output bus voltage          | $V_{CAN\_L}$ | 0.5 V<br>(preferred: 0.8 V)  | 1.5 V   | 2.25 V<br>(preferred: 2.0 V) |
| Differential output voltage | $V_{diff}$   | 1.5 V                        | 2.0 V   | 3.0 V                        |
| Common mode bus voltage     | $V_{CM}$     | 2.1 V                        | 2.5 V   | 2.9 V                        |

#### 4.1.2 Recessive Input Threshold.

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope               | Measure the recessive input threshold of the Device Under Test (DUT).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Conditions          | The test circuit according to Figure 2 shall be used.<br>$R_{Test} = 120 \Omega$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Test Method         | <p>Set the current <math>I</math> to a value which induces the upper threshold <math>V_{diff} = 0.5 \text{ V}</math>.<br/> <b>Note:</b> Refer to Figure A1 in Appendix A for a schematic of the current source <math>I</math>.<br/> Then set <math>U</math> to a value that generates:</p> <ol style="list-style-type: none"> <li><math>V = -2.0 \text{ V}</math> and</li> <li><math>V = 6.5 \text{ V}</math>.</li> </ol> <p>Monitor the CAN lines, the RxD and TxD lines of the DUT and check at which level the DUT still detects a recessive bit and, therefore, tries to transmit its messages.<br/> Add oscilloscope plots to the test report showing the bus activity at:</p> <ol style="list-style-type: none"> <li><math>V = -2.0 \text{ V}</math> and <math>V_{diff} = 0.5 \text{ V}</math> and</li> <li><math>V = 6.5 \text{ V}</math> and <math>V_{diff} = 0.5 \text{ V}</math>.</li> </ol> |
| Acceptance Criteria | Under both conditions the DUT is not allowed to stop the transmission of its frames.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

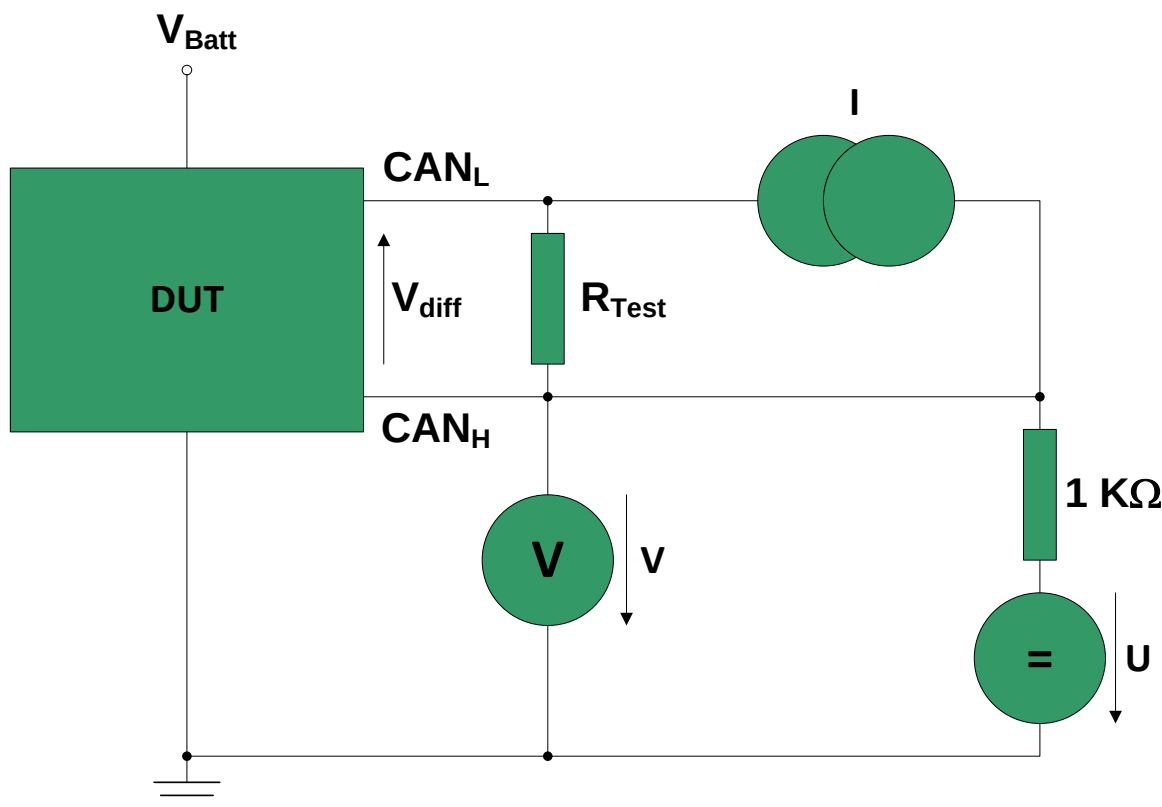


Figure 2: Recessive Input Threshold Test Circuit

#### 4.1.3 Dominant Input Threshold.

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope               | Measure the dominant input threshold of the DUT.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Conditions          | The test circuit according to Figure 3 shall be used.<br>$R_{\text{Test}} = 120 \, \Omega$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Test Method         | <p>Set the current <math>I</math> to a value which induces the upper threshold <math>V_{\text{diff}} = 0.5 \, \text{V}</math> to <math>0.9 \, \text{V}</math>, in steps of <math>0.1 \, \text{V}</math>.</p> <p><b>Note:</b> Refer to Figure A1 in Appendix A for a schematic of the current source <math>I</math>.</p> <p>Then set <math>U</math> to a value that generates:</p> <ol style="list-style-type: none"> <li><math>V = -2.0 \, \text{V}</math> and</li> <li><math>V = 6.5 \, \text{V}</math>.</li> </ol> <p>Monitor the CAN lines, the RxD and TxD lines of the DUT and check at which level the DUT still detects a recessive bit and, therefore, tries to transmit its messages.</p> <p>Add oscilloscope plots to the test report showing the bus activity at:</p> <ol style="list-style-type: none"> <li><math>V = -2.0 \, \text{V}</math> and <math>V_{\text{diff}} = 0.5 \, \text{V}</math> to <math>0.9 \, \text{V}</math>, increase in steps of <math>0.1 \, \text{V}</math> and</li> <li><math>V = 6.5 \, \text{V}</math> and <math>V_{\text{diff}} = 0.5 \, \text{V}</math> to <math>0.9 \, \text{V}</math>, increase in steps of <math>0.1 \, \text{V}</math>.</li> </ol> |
| Acceptance Criteria | <p>Under both conditions, the DUT shall stop the transmission of its frames at the latest when a dominant input threshold of <math>0.9 \, \text{V}</math> is reached.</p> <p><b>Note:</b> The DUT shall try to transmit its message at a dominant input threshold of <math>0.5 \, \text{V}</math>, but it is possible that the communication is disturbed.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

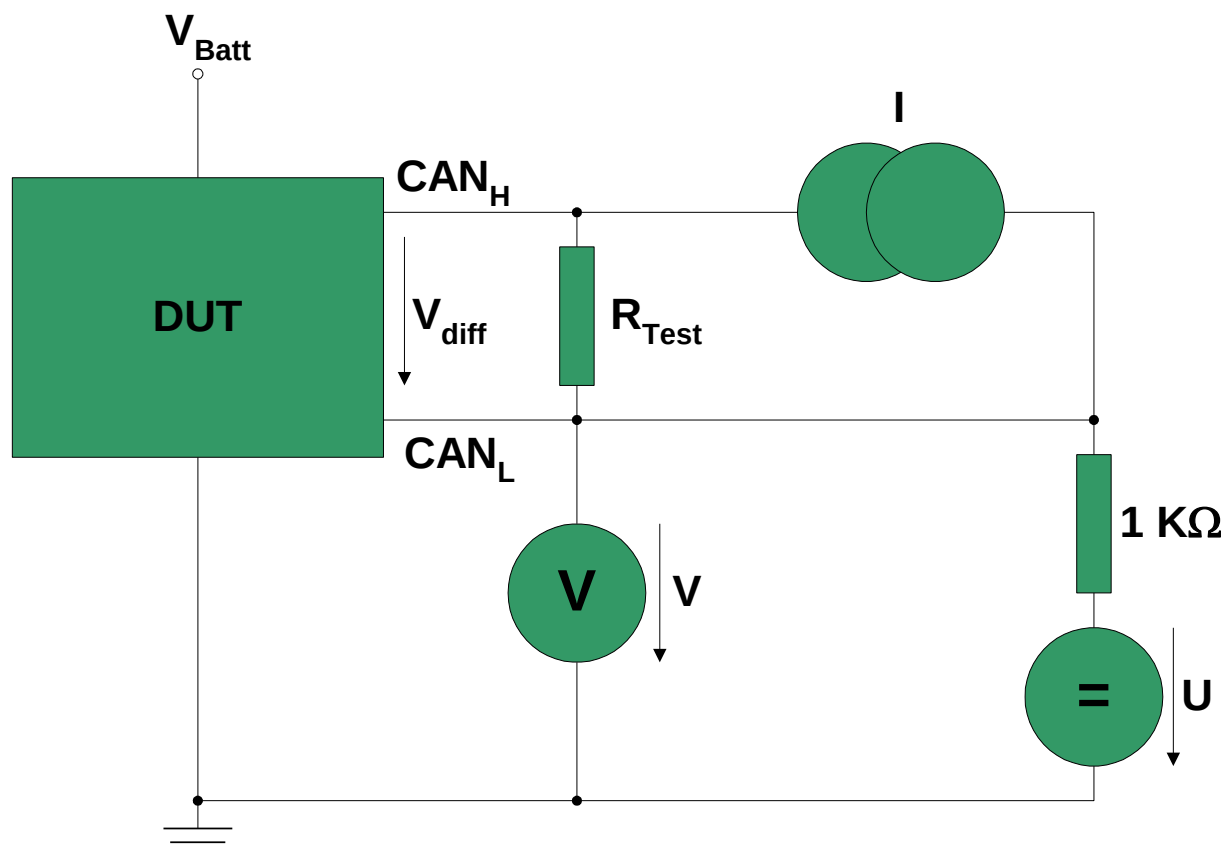


Figure 3: Dominant Input Threshold Test Circuit

#### 4.1.4 Device Resistance.

##### 4.1.4.1 Internal Resistance of CAN<sub>H</sub> and CAN<sub>L</sub>.

##### 4.1.4.1.1 DUT is connected to supply and ground.

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope               | Measure the internal resistance of CAN <sub>H</sub> and CAN <sub>L</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Conditions          | <p>The test circuit according to Figure 4 shall be used. An oscilloscope shall be used for measuring the recessive voltage level on the CAN line.</p> <p>The CAN<sub>H</sub> and CAN<sub>L</sub> shall be shorted. <math>R_{Test} = 5\text{ k}\Omega</math>.</p> <p><b>Note:</b> All Input(s)/Outputs(s) (I/O(s)), e.g., external sensors, shall be connected.</p>                                                                                                                                                                                |
| Test Method         | <p>Measure V and calculate <math>R_{in}</math> with the following formula:</p> <p><b>Note:</b> Measured value of <math>R_{in}</math> represents the <math>R_{in\_H}</math> and <math>R_{in\_L}</math> in parallel.</p> $R_{in} = 2 \cdot R_{Test} \frac{V_{CAN} - V}{V - U}$ <p>Where <math>V_{CAN}</math> is the recessive output voltage level according paragraph 4.1.1.1.</p> <p>Determine <math>R_{in\_CAN\_H}</math> and <math>R_{in\_CAN\_L}</math> for <math>U = -2.0\text{ V}</math> and <math>U = 7.0\text{ V}</math> respectively.</p> |
| Acceptance Criteria | See Table 3.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

Table 3 Internal Resistance of CAN<sub>H</sub> and CAN<sub>L</sub>

| Parameters                       | Minimum | Maximum | Condition |
|----------------------------------|---------|---------|-----------|
| R <sub>in</sub> CAN <sub>H</sub> | 5 kΩ    | 50 kΩ   | No Load   |
| R <sub>in</sub> CAN <sub>L</sub> | 5 kΩ    | 50 kΩ   | No Load   |

**4.1.4.1.2 DUT is not connected to supply.**

**Scope** If the supply voltage is interrupted, e.g., fuse open, the CAN<sub>H</sub> and CAN<sub>L</sub> line shall have a high resistance to supply or ground (GND) in order to prevent damage in the connected ECU.

**Conditions** No peripherals are connected.  
The test circuit according to Figure 4 shall be used.  
The CAN<sub>H</sub> and CAN<sub>L</sub> shall be shorted.  
Disconnect the DUT from the supply line.

**Test Method** Measured value of R<sub>in</sub> represents the R<sub>in,H</sub> and R<sub>in,L</sub> in parallel and R<sub>in</sub> is calculated with the following formula:

$$R_{in} = 2 \cdot R_{test} \frac{V}{U - V}$$

Determine R<sub>in,CAN,H</sub> and R<sub>in,CAN,L</sub> at U = -2.0 V and U = 7.0 V respectively.

**Acceptance Criteria** R<sub>in,CAN,H</sub> ≥ 5 kΩ and R<sub>in,CAN,L</sub> ≥ 5 kΩ.

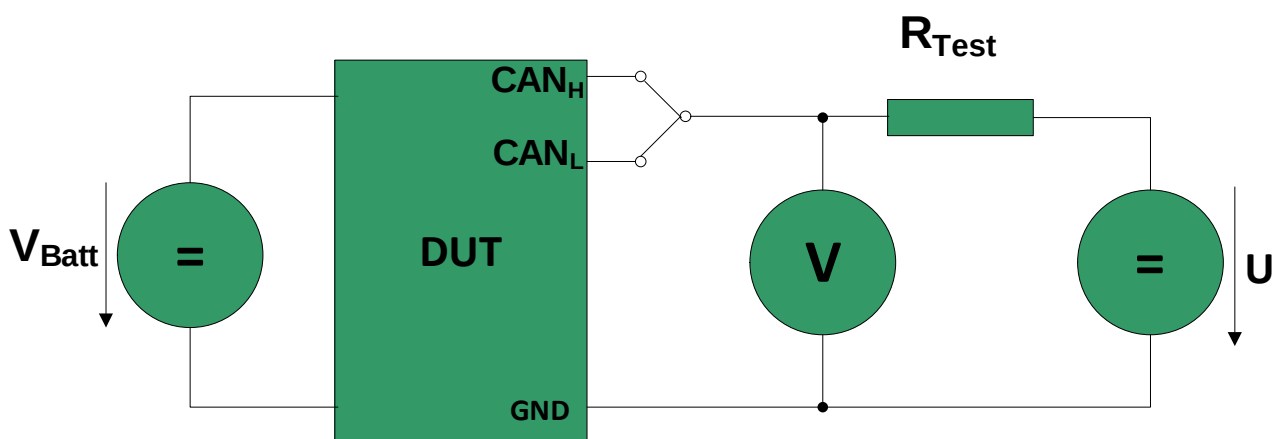


Figure 4: Measurement of Internal Resistance

4.1.4.1.3 DUT is not connected to ground.

|             |                                                                                                                                                                                                      |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope       | If the ground connection of the DUT is interrupted, the CAN <sub>H</sub> and CAN <sub>L</sub> line shall have a high resistance to supply or ground in order to prevent damage in the connected ECU. |
| Conditions  | The test circuit according to Figure 5 shall be used. Disconnect the DUT from the ground line.<br><b>Note:</b> All I/O(s), e.g., external sensors, shall be connected.                               |
| Test Method | Measure the output leakage current of the DUT between CAN <sub>H</sub> and ground and CAN <sub>L</sub> and ground. Calculate $R_{in\_CAN\_H}$ and $R_{in\_CAN\_L}$ as follows:                       |

$$R_{in} = \frac{U_{Batt}}{I_{leak}}$$

Acceptance Criteria  $R_{in\_CAN\_H} \geq 5 \text{ k}\Omega$  and  $R_{in\_CAN\_L} \geq 5 \text{ k}\Omega$ .

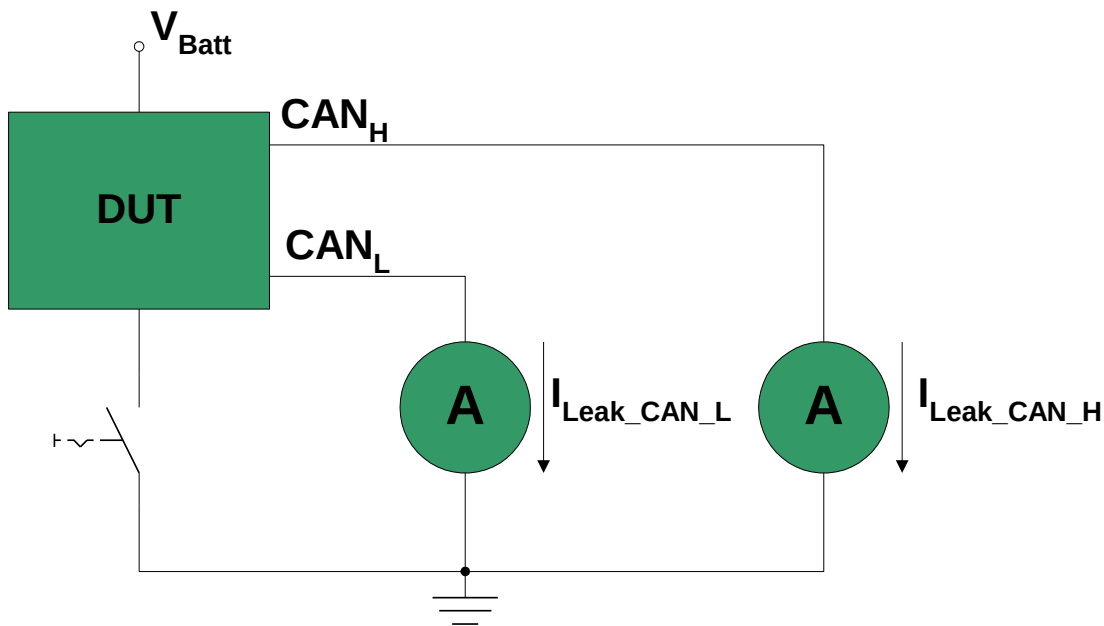


Figure 5: Measurement of Internal Resistance in Case of Loss Of Ground (LOG)

#### 4.1.4.2 Internal Differential Resistor.

Scope Measure the internal differential resistance of the DUT

Conditions The test circuit according to Figure 6 shall be used.

$$U = 5 \text{ V.}$$

$$R_{\text{Test}} = 120 \text{ } \Omega.$$

Test Method Measure V and calculate  $R_{\text{diff}}$  with the following formula:

**Note:**  $V_{\text{diff}}$  is the recessive differential open circuit voltage according to paragraph 4.1.1.1.

$$R_{\text{diff}} = R_{\text{Test}} \frac{V_{\text{diff}} - V}{V - U}$$

Acceptance Criteria See Table 4.

Table 4: Internal Differential Resistor

| Parameters        | Minimum      | Nominal      | Maximum      | Condition                        |
|-------------------|--------------|--------------|--------------|----------------------------------|
| $R_{\text{diff}}$ | 116 $\Omega$ | 120 $\Omega$ | 128 $\Omega$ | DUT with regular bus termination |

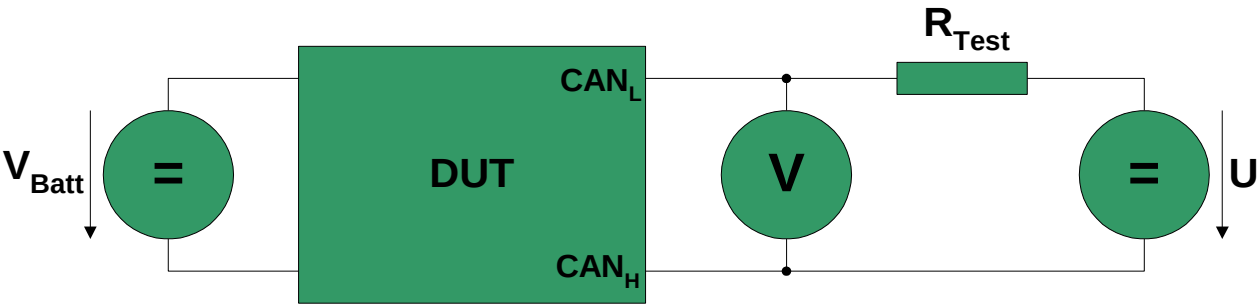


Figure 6: Internal Differential Resistor Measurement

# 4.1.5 Device Capacitance.

## 4.1.5.1 Input Capacitance.

|            |                                                                                                                                                                                                       |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope      | Measure and calculate the input capacitance of the DUT.                                                                                                                                               |
| Conditions | The test circuits according to Figure 7 shall be used. The DUT will fail this test if it has a built in termination network. To perform this test properly, the termination network shall be removed. |

$$R_{Test} = 5 \text{ k}\Omega.$$

|             |                                                                                            |
|-------------|--------------------------------------------------------------------------------------------|
| Test Method | Measure $\tau_a$ as shown in Figure 8 and calculate $C_{Fig8}$ with the following formula: |
|-------------|--------------------------------------------------------------------------------------------|

$$\tau = 0.721 \cdot (t_2 - t_1)$$

$$C_{Fig8} = \frac{\tau_a}{R_{Test}}$$

$$C_{in} = \frac{C_{Fig8}}{2}$$

Add oscilloscope plots to the test report showing  $\tau_a$  measurement.

|                     |                                                                                                                                    |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------|
| Acceptance Criteria | $40 \text{ pF} \leq C_{in \text{ CAN\_H}} \leq 150 \text{ pF}.$<br>$40 \text{ pF} \leq C_{in \text{ CAN\_L}} \leq 150 \text{ pF}.$ |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------|

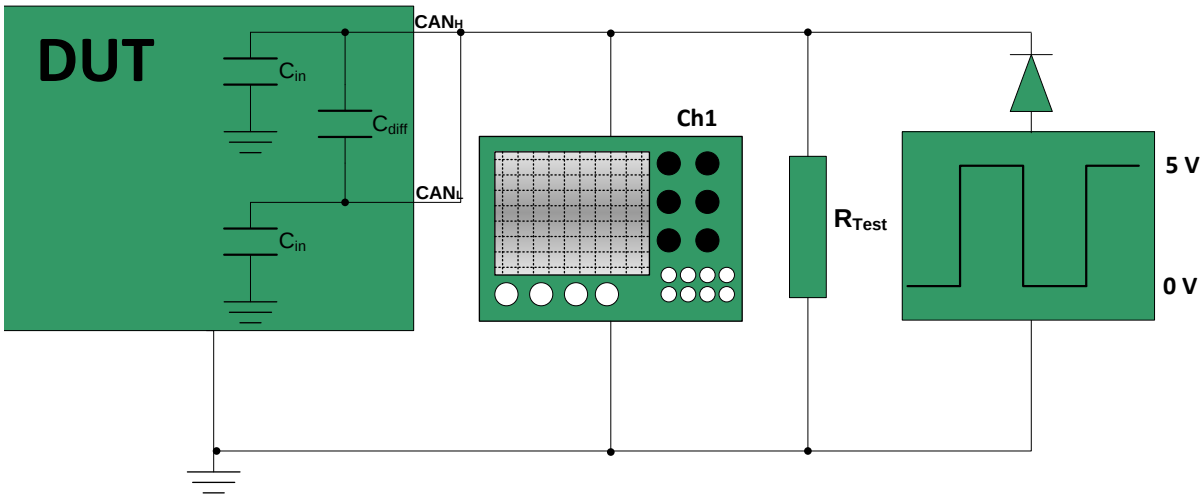


Figure 7: Measurement of  $\tau_a$

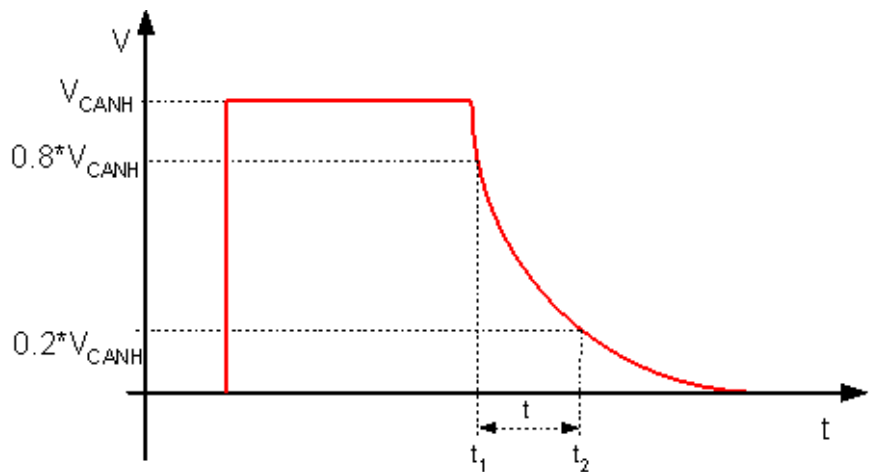
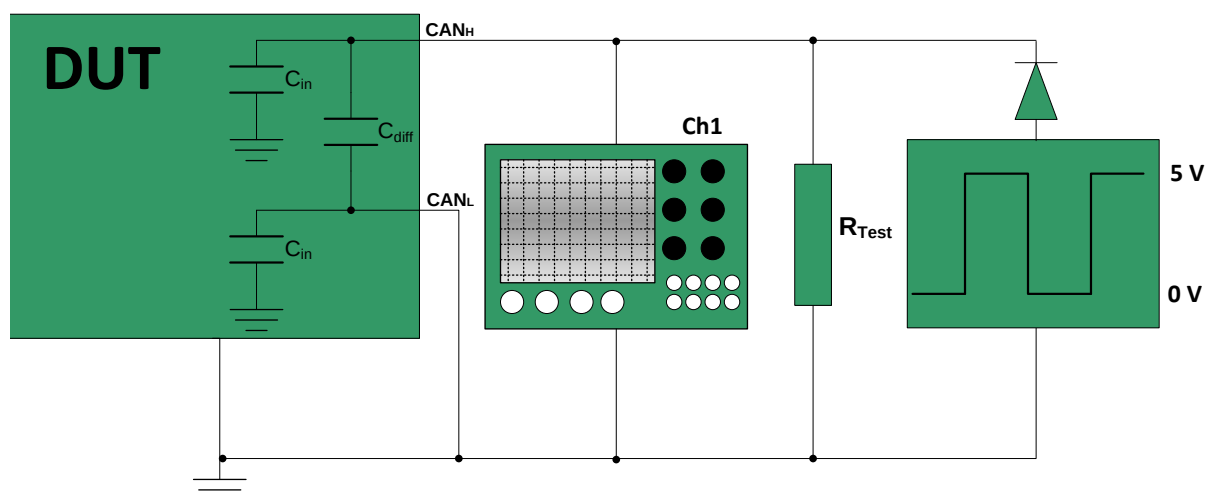


Figure 8:  $\tau$  Definition

#### 4.1.5.2 Input Differential Capacitance.

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope               | Measure and calculate the differential capacitance of the DUT.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Conditions          | The test circuits according to Figure 9 shall be used. The DUT will fail this test if it has a built in termination network. To perform this test properly, the termination network shall be removed.                                                                                                                                                                                                                                                                                                                                                                   |
|                     | $R_{Test} = 5 \text{ k}\Omega$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Test Method         | Measure $\tau_b$ as shown in Figure 9 and calculate $C_{Fig9}$ with the following formula: <div style="border: 1px solid black; padding: 5px; margin: 10px auto; width: fit-content;"> <math display="block">C_{Fig9} = \frac{\tau_b}{R_{Test}}</math> </div> <div style="border: 1px solid black; padding: 5px; margin: 10px auto; width: fit-content;"> <math display="block">C_{diff} = C_{Fig9} - C_{in}</math> </div> <p>Use <math>C_{in}</math> from paragraph 4.1.5.1.</p> <p>Add oscilloscope plots to the test report for <math>\tau_b</math> measurement.</p> |
| Acceptance Criteria | $0 \text{ pF} \leq C_{diff} \leq 90 \text{ pF}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

Figure 9: Measurement of  $\tau_b$

**4.1.6 Minimum and Maximum Supply Voltage Level for Bus Communication.****4.1.6.1 Minimum Supply Voltage Level and Resume Time Measurement.**

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Scope               | Determine the minimum supply voltage level threshold for a correct bus communication.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Conditions          | Set up a physical network consisting of the DUT and a test tool. The test tool must be able to simulate all nodes that are necessary for normal bus communication of the DUT.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Test Method         | <p>Set the supply voltage to 0 V initially.</p> <p>Increase the supply voltage in steps of 0.1 V with a speed of 1 minute per step.</p> <p>Check at which voltage level the bus communication starts with no communication problems, i.e., no error frames on the bus and no corrupted or delayed transmission of messages. Document the voltage level <math>V_{TH\_Resume}</math>.</p> <p>Decrease the supply voltage of the DUT in steps of 0.1 V with a speed of 1 minute per step and check the minimum voltage level till which the bus communication is proper. Document the voltage level <math>V_{TH\_Minimum}</math>.</p> <p>Then decrease the voltage to further 1 V lower than the minimum voltage level where ECU enters the sleep mode.</p> <p>Instantly increase the supply voltage greater than <math>V_{TH\_Resume}</math> and measure the time difference between the voltage reaching <math>V_{TH\_Resume}</math> and the transmission of first message from DUT.</p> <p>Document the time <math>T_{Resume}</math>.</p> <p>Add the following oscilloscope plots to the test report:</p> <ol style="list-style-type: none"> <li>1. Oscilloscope plots displaying CGI/TSI bus activity and message trace at minimum supply voltage.</li> <li>2. Oscilloscope plots displaying CGI/TSI bus activity and message trace at the resume voltage showing resume time period also where communication starts again.</li> </ol> |
| Acceptance Criteria | <p>The DUT shall support error-free bus communication down to a supply voltage level of 6.0 V (unless otherwise specified in the applicable Subsystem Technical Specification (SSTS) or Component Technical Specification (CTS)).</p> <p>The DUT shall resume bus communication within 300 ms.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |