



General Motors Local Area Network (GMLAN) Single Wire Controller Area Network (SWCAN) Physical and Data Link Layers Specification

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1 Introduction

Note: Nothing in this standard supercedes applicable laws and regulations.

Note: In the event of conflict between the English and domestic language, the English language shall take precedence.

1.1 Purpose. This document specifies the physical layer requirements for a Carrier Sense Multiple Access/Collision Resolution (CSMA/CR) data link which operates on a single wire medium to communicate among Electronic Control Units (ECU) on road vehicles at normal transmission rates of 33.333 kbits/s and at a special high speed assembly or service transmission bit rate of 83.333 kbits/s.

This document is to be referenced by the particular Component Technical Specification (CTS) which describes any given ECU in which the single wire data link controller and physical layer interface is located. Only the performance of the data link physical layer is specified in this document. ECU environmental and other requirements shall be provided in the ECU CTS.

The intended audience includes, but is not limited to ECU suppliers, Controller Area Network (CAN) controller suppliers, CAN transceiver suppliers, component release engineers and platform system engineers.

1.2 Applicability. This specification describes the physical layer requirements for a single wire data link capable of operating with various CSMA/CR protocols such as the CAN version 2.0. This serial data link network is intended for use in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor (μ P) and/or dedicated logic devices which use the network.

The network shall be able to operate in either the normal data rate mode or a high speed data download mode for assembly line and service data transfer operations. The high speed mode is only intended to be operational when the bus is attached to an off-board service node. This node shall provide temporary bus electrical loads which facilitate higher speed operation. Such temporary loads shall be removed when not performing download operations.

This physical layer specification includes such transceiver requirements as are necessary to ensure that the bus voltage signals and that a common Integrated Circuit (IC) footprint can be achieved across all applications. The transceiver requirements are specified in Appendix A.

1.3 Remarks. This specification is not restricted.

2 References

Note: Only the latest approved standards are applicable unless otherwise specified.

2.1 External Standards/Specifications.

ISO 11898	ISO 16845	SAE 970295
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2.2 GM Standards/Specifications.

GMW3059	GMW3103	GMW3173	GMW14241
GMW3097	GMW3172		

2.3 Additional References.

(ID) = This standard/material is limited to internal distribution within General Motors and shall not be distributed outside this company. Contact the GM Lead Engineer for further instructions.

- A description of GM-J1962 On-Board Diagnostic (OBD) interface is available from the Global General Assembly Service and Electrical site at Uniform Resource Locator (URL): <http://avg.me.gm.com/standard/global/ggse.asp> (ID)
- A list of known CAN controller and transceiver issues is available in Global Document Management (GDM): Cabinets/Global Product Development/Global Engineering/Vehicle Systems & Technology (by VPPS)/Electrical Systems Controls Software/8_Electrical Function/87_Electrical Architecture/87_ECU Hardware & Network Infrastructure/ECU HW (ID)
- A list of preferred devices and their suppliers is available in GDM: Cabinets/Global Product Development/Global Engineering/Vehicle Systems & Technology (by VPPS)/Electrical

Systems_Controls_Software/8_Electrical Function/87_Electrical Architecture/87_ECU Hardware & Network Infrastructure/CAN/Information for sourcing (ID)

- Applicable CTS, Subsystem Technical Specification (SSTS), or other Platform Specific Technical Specification (PSTS)
- CAN version 2.0 specification (only with recessive to dominant bit synchronization)
- Electrostatic Discharge (ESD) Protection Equivalent Series Resistance (ESR) EPCOS B82432-A1473-K size 1812, or equivalent, available at electronic component suppliers, e.g., EPCOS, URL: <http://www.epcos.com/>
- General Motors Network Management (GMNM) software: URL: <https://share.gm.com/sites/SSPR/IVLAN/IVLAN/Forms/Specifications.aspx> (ID)
- Intel 82527 data sheet available at URL: <http://www.datasheetcatalog.com/>
- Melexis application note: Application_Note_390118056023_RxD glitch at mode change from sleep.pdf
- Philips SJA1000 data sheet available at URL: <http://www.datasheetcatalog.com/>

3 Requirements

The physical layer is responsible for providing a method of transferring digital data symbols (1's and 0's) to the communication medium. The physical layer interface is a single wire, ground referenced bus with high side voltage drive. Requirements in this document generally apply over the specified operating conditions and lifetime unless otherwise noted.

3.1 Physical and Data Link Layer Characteristics.

3.1.1 CSMA/CR bus access and arbitration with dominant high and recessive low signal voltages.

3.1.2 Only performs bit resynchronization on recessive to dominant bit transitions.

3.1.3 The CAN controller shall be capable of transmitting and receiving messages with both standard frame format, i.e., 11-bit CAN identifiers, and extended frame format, i.e., 29-bit CAN identifiers (CAN 2.0B active). The CAN controller shall support mixed mode operation with CAN identifiers of both 29-bit and 11-bit in length. Alternatively tolerant of messages with extended frame format (CAN 2.0B passive) if explicitly called out per the CTS, SSTS or PSTS bus implementation specifications. The CAN controller shall be fully compatible to ISO 11898. For example, the enhanced protocol for higher clock tolerance must be supported, e.g., tolerate 2-bit message intermission.

3.1.4 Compliance to ISO 11898 shall be verified through CAN conformance testing according to the ISO 16845 test plan. Successful passing of the complete conformance test shall be documented through provision of a written statement of the semiconductor manufacturer. The test plan conformance declaration shall indicate which product version was tested and which version of the CAN conformance test plan was used as reference.

3.1.5 The controller must support the complete range of resynchronization jump width settings specified in ISO 11898. In particular, a bit timing parameter setting of Synchronization Jump Width (SJW) = 2 time quanta = PHASE_SEG2 must be supported. Also, the resynchronization function must be operational when a synchronization edge is detected outside the range set by the SJW parameter, i.e., when the phase error is greater than the SJW, the CAN controller shall adjust the timing of the current bit by SJW time quanta.

3.1.6 The controller must perform at most one hard and/or resynchronization action per CAN bit time, the time between any two sample points. The earliest point in time when the next resynchronization is permitted is after the sample point of the current bit as determined by the most recent bit resynchronization action. This means after any bit resynchronization action (hard and/or resynchronization), the resynchronization function must be disabled until the currently pending bit sampling has been concluded. This would allow the next resynchronization (at the earliest) in t_{SEG2} of this bit if the sample result was "recessive". This case might occur due to a glitch on the bus. **Note:** This requirement applies to both the hard synchronization function at the start of a frame as well as to the resynchronization function while frame transmission/reception is ongoing.

3.1.7 When the bus is idle and a recessive to dominant signal edge has occurred, then the controller shall behave in the following manner:

- The controller must sample the bit value at the specified time after this signal edge and must disregard any consecutive edges until sampling of the current bit has been concluded, e.g., hard synchronization function must be disabled immediately upon receipt of the first Recessive to Dominant (R-D) edge after an idle period.
- If the sampling result is "dominant", then this event shall be taken as a valid start of frame bit.
- Otherwise, if the sampling result is "recessive", then the edge shall be considered as a glitch and shall be disregarded. In particular, there must not be any error frame transmission due to a glitch while the bus is idle.

3.1.8 It is *not* recommended to feed CAN controllers with a Phase Locked Loop (PLL) generated clock signal. If a CAN controller is operated with a PLL clock, then careful analysis of the implications of the additional clock jitter is required. As a preventive measure extra accuracy requirements on the oscillator clock apply in this case. See 3.2.4 CAN Controller Clock Tolerance.

3.1.9 The information processing time of the protocol controller must be equal to 2 time quanta or less.

3.1.10 The CAN controller may employ a message buffer concept with or without Dual Ported Random Access Memory (DPRAM).

3.1.11 The CAN protocol controller shall provide at least two (2) transmit message buffers and two (2) receive message buffers. This is to ensure that higher priority messages are not blocked by lower priority messages and that new messages are not "dropped" while the Central Processing Unit (CPU) is still reading the current message.

3.1.12 Any time when more than one transmit buffer is armed for transmission, then the protocol controller shall automatically, e.g., without any CPU support, transmit the message with the lowest CAN identifier first.

3.1.13 When two or more messages with the same CAN identifier are armed for transmission, then the protocol controller shall transmit these messages in a First-In, First-Out (FIFO) fashion, i.e., in the sequence how they were armed.

3.2 Bus Operation.

3.2.1 Normal Communication. Transmission bit rate in normal communication is 33.333 kbits/s. Table 1 defines all compliant bit timing settings for operation at 33.333 kbits/s including the recommended controller settings for TSEG1 and TSEG2. See Appendix D for information on how these values were calculated. Normal transmission mode shall use transmitters with controlled waveform rise and overshoot times. Waveform trailing edge control is required to assure that high frequency components are minimized at the beginning of the downward voltage slope. The remaining fall time occurs after the bus is inactive with drivers off and is determined by the Resistor Capacitor (RC) time constant of the total bus load.

Table 1: 33.333 kbits/s Compliant Bit Timing Settings

t_q	t_{sjw}	$t_{SEG2min}$	SJW	TSEG1	TSEG2
1.5 μ s	4.5 μ s	4.5 μ s	2 (3 t_q)	15 (16 t_q)	2 (3 t_q)
1.58 μ s	3.16 μ s	3.16 μ s	1 (2 t_q)	15 (16 t_q)	1 (2 t_q)
1.67 μ s	3.33 μ s	3.33 μ s	1 (2 t_q)	14 (15 t_q)	1 (2 t_q)
1.76 μ s	3.52 μ s	3.52 μ s	1 (2 t_q)	13 (14 t_q)	1 (2 t_q)
1.88 μ s	3.76 μ s	3.76 μ s	1 (2 t_q)	12 (13 t_q)	1 (2 t_q)
2.0 μ s	4.0 μ s	4.0 μ s	1 (2 t_q)	11 (12 t_q)	1 (2 t_q)

3.2.2 High Speed Communication. Transmission bit rate in high speed communication is 83.333 kbits/s. Table 2 defines all compliant bit timing settings for operation at 83.333 kbits/s. This mode is used for assembly line and service data download when the on-board network is attached to an off-board ECU. High speed transmission mode allows shortened bit time and shortened waveform rise and fall times. Electromagnetic Compatibility (EMC) requirements in 3.5 Radiated Electromagnetic Interference (EMI) Protection are waived while in this mode. Bus transmitter drive circuits for those nodes which are required to communicate in high

speed mode shall be able to drive reduced bus resistance when in this mode. See Table 3 and Appendix C. High speed communications shall utilize the normal mode signal voltage levels as specified in Table 3.

The test tool must connect R_{tool} to the bus before transmitting any high speed messages. R_{tool} shall be connected directly to ground on the ECU via an appropriate switch, e.g., transistor or relay. R_{tool} shall never be connected to the Load pin of the transceiver. The Load pin is not designed to handle the high level of current through R_{tool} .

All nodes shall be able to operate at the High Speed mode frame timing and shall enter this mode when they have been commanded by the download system manager. The normal sequence of entering and leaving high speed mode is as follows, commanded by the download system manager (additional steps may be inserted by the download system manager as needed):

- All nodes are awakened at normal bus speed.
- The download tool switches the bus circuit to the lower tool bus resistance.
- All nodes are commanded to go to high speed mode.
- High speed traffic is completed.
- All nodes are commanded to go to normal speed mode.
- The download tool switches the tool bus resistance out of the bus circuit.

Nodes shall not be allowed to go to sleep during high speed mode. If they are asleep and then get an input which would require them to send a message, they will corrupt the service activity.

Nodes shall initialize in the normal speed mode after a power up, running reset or CAN bus off condition.

Table 2: 83.333 kbits/s Compliant Bit Timing Settings

t_q	t_{SJWmin}	$t_{SEG2min}$	SJW	TSEG1	TSEG2
0.6 μs	1.8 μs	1.8 μs	2 (3 t_q)	15 (16 t_q)	2 (3 t_q)
0.632 μs	1.896 μs	1.896 μs	2 (3 t_q)	14 (15 t_q)	2 (3 t_q)
0.667 μs	2.0	2.0 μs	2 (3 t_q)	13 (14 t_q)	2 (3 t_q)
0.706 μs	2.118 μs	2.118 μs	2 (3 t_q)	12 (13 t_q)	2 (3 t_q)
0.75 μs	1.5 μs	2.25 μs	2 (3 t_q)	11 (12 t_q)	2 (3 t_q)
0.8 μs	1.6 μs	1.6 μs	2 (3 t_q)	10 (11 t_q)	2 (3 t_q)
0.857 μs	1.714 μs	1.714 μs	2 (3 t_q)	9 (10 t_q)	2 (3 t_q)
0.923 μs	1.846 μs	1.846 μs	1 (2 t_q)	9 (10 t_q)	1 (2 t_q)
1.0 μs	2.0 μs	2.0 μs	1 (2 t_q)	8 (9 t_q)	1 (2 t_q)

3.2.3 ECU Selective Awake. This bus includes a selective node awake capability, which allows normal communication to take place among some nodes while leaving the other nodes in an undisturbed sleep state. This is accomplished by controlling the signal voltages such that all nodes must wake up when they receive a higher voltage message signal waveform. The communication system communicates to the nodes information as to which nodes are to stay operational (awake) and which nodes are to put themselves into a non-communicating low power "sleep" state. Communication at the lower, normal voltage levels shall not disturb the sleeping nodes.

The transceiver's loss of ground protection circuit connection to ground shall not be interrupted when in the sleep mode. To accomplish this, all nodes shall maintain V_{batt} on the transceiver at all times when any serial communication can take place. This is to ensure that the unit resistive loads shall not be removed from the network timing circuit. The recommended method of power moding serial communications nodes shall be by use of the network sleep mode.

The High Speed and High Voltage wake up features shall not be active at the same time. This requires that the bus be awakened only when in the normal speed mode.

Methods and connections for host wake up circuits:

- CAN controller in the "wake up on bus activity" sleep mode. Upon receipt of a wake up bus signal, the transceiver Receive Input (RxD) output shall pass received bus signals to the controller's RxD input, which will awaken the controller, and the controller will then issue a wake up signal or interrupt to the local microprocessor to begin CAN operations.

In this case, the controller is typically in an intermediate sleep state, which is not the lowest sleep power consumption state.

- Microprocessor connects the transceiver's RxD pin to a latched port as a wake up input.

Upon receipt of a wake up bus signal, the transceiver RxD output shall pass received bus signals to the microprocessors latched wake up input. The latched RxD signal shall wake up the microprocessor which then initializes the CAN controller and enables CAN operation. The latch is reset after the microprocessor has put the transceiver into another sleep mode before the microprocessor puts the ECU to sleep.

In this case, the controller is typically in the lowest power consumption sleep state.

- ECU with transceiver implementing $V_{reg\ cntrl}$ pin.

Devices, which implement a transceiver with a $V_{reg\ cntrl}$ pin will wake up when Positive Supply Voltage (V_{cc}) is applied due to a serial data wake-up event occurring. In order to remain awake, the mode control inputs of the transceiver must be changed to any mode other than Sleep, e.g., by the microcontroller (μC).

Note: Some of the devices can create an RxD glitch when transitioning out of Sleep mode. See Appendix K for information on how to deal with this glitch.

3.2.4 CAN Controller Clock Tolerance. All nodes which operate on the Single Wire Controller Area Network (SWCAN) bus shall utilize a CAN controller with a bit timing clock tolerance of less than or equal to $\pm 0.35\%$ (alternatively $\pm 0.5\%$ if called out per CTS, SSTS, or PSTS bus implementation specifications) to ensure that the CAN bit timing synchronization shall not be affected by the waveform rise and fall times. See Appendices B and J.

Note: Careful analysis of the bit time tolerance is recommended when PLL clocks are considered. The permitted tolerance of the oscillator circuit is reduced when a PLL clock is used for the CAN data link layer controller. For example, the suitable oscillator tolerance would be 0.05% in the case where the PLL circuit exhibits an add-on tolerance of 0.3%.

When a ceramic resonator with a maximum tolerance of 0.3% is used with a PLL, the add-on clock tolerance of the PLL is limited to 0.05% over a single bit time. In normal speed mode, this is equivalent to 0.05% of 30 μs , or 15 ns maximum jitter over 30 μs . In high speed mode, this is equivalent to 0.05% of 12 μs , or 6 ns maximum jitter over 12 μs .

3.2.5 Bus Electrical Parameters. There are two possible modes of the bus electrical voltage level parameters required by devices which drive and receive signals on the single wire bus. They are the normal and the wake up communications signal levels. See Table 3. The high level signals (V_{oh} , V_{ih} , V_{ohWu} , and V_{ihWu}) of Table 3 are considered to be the dominant or driven-to-high-voltage bus states.

The High Speed and High Voltage wake up bus signals shall not be active at the same time.

3.2.5.1 Normal Mode Transmit and Receive Voltage Thresholds for Data Communication. Serial communication shall operate with normal signal voltage levels indicated in Table 3 without generating a wake up signal or interrupt to the ECU controller when the battery voltage is sufficient to prevent this. See Table 3.

3.2.5.2 High Speed Mode Transmit and Receive Signal Voltages. The high speed input threshold and output signal voltages are the same as the normal mode signals. See Table 3.

High speed operation dominant bus symbols shall not exceed the transceiver duty cycles, operating voltage, and temperature requirements as specified in A9 and A10 in Appendix A.

3.2.5.3 Wake Up Signal Voltage Levels. A special higher voltage communication waveform using higher signal voltages shall be used to transmit wake up message frames. Transceivers which detect that the signal voltage has exceeded the wake up threshold for the minimum wakeup filter time shall provide a wakeup signal to its ECU. See Table A1 in Appendix A. The CAN wakeup frame shall provide at least three consecutive normal speed dominant bit times either in the Identifier or in the data fields. The wakeup frame shall not be sent when in the high speed mode. See 3.2.2 High Speed Communication. For $V_{batt} > 12.7$ V, messages which are transmitted at the normal voltage levels shall not wake up any receiving ECU.

Messages which are transmitted at the higher wake up voltage levels shall meet normal bit timing rules at the normal input threshold voltage V_{ih} ; so as to be interpreted as normal data as well as wake up commands. See Table 3.

3.2.6 SWCAN Bus Signals and Loading Requirements. Table 3, Part B Parameter Limits shall be met over Table 3, Part A Operating Conditions including the specified bus loading range. Testing shall be performed using the particular application circuit. See 3.12 Recommended Transceiver Application Circuits.

Table 3: SWCAN Bus Signals Loading Requirements
Part A: Operating Conditions

Operating Condition Parameter	Symbol	Minimum	Typical	Maximum	Unit
ECU and test tool operational battery voltage input except high speed mode ^{Note 1}	V_{batt}	7.0	12	18	V
Low battery ECU operating supply voltage except in high speed mode and sleep mode	$V_{batt\ low}$	6.0	---	7.0	V
Short duration high battery ECU operating supply voltage ($t < 1$ minute, $t_{amb} < 85$ °C) except in high speed mode	$V_{batt\ high}$	18	24	26.5	V
ECU battery voltage input in high speed mode ^{Note 1}	V_{batt}	9	12	16	V
Test tool battery voltage input in high speed mode ^{Note 1}	V_{batt}	9	12	14	V
Ground offset voltage	$V_{g\ off}$	---	---	1.3	V
Low battery ground offset voltage	$V_{g\ off\ low\ batt}$	0.0	0.1 (V_{batt})	0.7 (V_{batt}) - 3.6	V
Battery ECU offset voltage when sleeping devices shall be activated	$V_{b\ off}$	---	---	1.0	V
Network total resistance except in high speed mode ^{Notes 2, 3}	R_{tl}	200	---	3332	Ω
High speed mode network resistance to ground (GND)	R_{load}	75	---	135	Ω
Network total capacitance in networks with 0.35% CAN clock tolerance ^{Notes 2, 4, 5}	C_{tl}	396	---	19 000	pF
Network total capacitance in networks with 0.5% CAN clock tolerance ^{Notes 2, 4, 5}	$C_{tl\ 0.5\%}$	396	---	17 000	pF
Network time constant in networks with 0.35% CAN clock tolerance ^{Notes 2, 5}	$\tau_{network}$	1.0	---	4.0	μs
Network time constant in networks with 0.5% CAN clock tolerance ^{Notes 2, 5}	$\tau_{network\ 0.5\%}$	1.0	---	3.6	μs
Network time constant in High Speed mode ^{Note 6}	τ_{hs}	---	---	1.5	μs
Number of system nodes including off vehicle test tool	---	2	---	32	---

Table 3: SWCAN Bus Signals Loading Requirements

Part B: Parameter Limits

(To be met over the specified Operating Conditions (Table 3, Part A) and component lifetime)

Device Behavioral Parameter ^{Note 7}	Symbol	Minimum	Typical	Maximum	Unit
Offset wakeup input high voltage threshold ^{Notes 8, 9}	$V_{ihWuOffset}$	$V_{batt} - 5.3$	---	$V_{batt} - 3.65$	V
Offset wakeup output high voltage ^{Note 10}	$V_{ohWuOffset}$	$V_{batt} - 2.7$	---	V_{batt}	V
Fixed wakeup input high voltage threshold ^{Notes 8, 9}	$V_{ihWuFixed}$	6.6	---	7.9	V
Fixed wakeup output high voltage ^{Note 11}	$V_{ohWuFixed}$	9.5	---	13 (12.5 preferred)	V
High speed and normal mode output high voltage ^{Note 10}	V_{oh}	4.2 normal, 3.9 high speed	4.65	5.1	V
Low battery output high voltage ($6.0 < V_{batt} < 7.0$)	$V_{oh \text{ lot Batt}}$	$V_{batt} - 2.8$	---	5.1	V
High speed and normal mode input high voltage input threshold	V_{ih}	2.0	2.1	2.2	V
Normal Bus recessive or passive state low voltage ^{Note 12}	$V_{leaknorm}$	-0.2	0	0.2	V
Loss of Ground (LOG) condition: Bus recessive or passive state low voltage ^{Note 12}	$V_{leakLOG}$	-0.2	---	0.5	V
Device resistance (unit load including LOG switch resistance)	R_{ul}	6435	6490	6665	Ω
Device resistance (primary load)	R_{pl}	2949	3010	3170	Ω
Device resistance (minimum load)	R_{min}	2000	---	---	Ω
Device capacitance (includes unit load and Printed Circuit Board (PCB) and connector capacitance and ESD protection, if required)	C_{ul}	135	150	300	pF
High speed mode tool resistance to GND (including tool's switch resistance to ground)	R_{tool}	120	130	140	Ω
Normal mode signal delay added to transition time: Bus rising edge ^{Notes 3, 13}	$t_{t \text{ norm}}$	2.0	---	6.3	μs
Normal mode signal delay added to transition time: Bus falling edge ^{Notes 3, 13}	$t_{t \text{ norm}}$	1.8	---	10.0	μs
High speed mode signal delay added to transition time: Bus rising edge ^{Note 14}	$t_{t \text{ hs}}$	0.1	---	1.7	μs
High speed mode signal delay added to transition time: Bus falling edge ^{Note 14}	$t_{t \text{ hs}}$	0.04	---	3.0	μs

Device Behavioral Parameter ^{Note 7}	Symbol	Minimum	Typical	Maximum	Unit
High Voltage Wake Up (HVWU) mode signal delay added to transition time: Bus rising edge ^{Notes 3, 13}	t_{f-wu}	2.0	---	6.3	μs
HVWU Mode signal delay added to transition time: Bus falling edge in networks with 0.35% CAN clock tolerance ^{Notes 3, 13}	t_{f-wu}	1.8	---	14.0 at 4.0 μs τ	μs
HVWU Mode signal delay added to transition time: Bus falling edge in networks with 0.5% CAN clock tolerance ^{Notes 3, 13}	$t_{f-wu} 0.5\%$	1.8	---	12.7 at 3.6 μs τ	μs
Normal mode, HVWU mode and high speed mode receive delay time	$t_{RxDelay}$	0.2	---	1.0	μs
Device leakage current to bus with no loss of ground	I_{leak}	---	---	10	μA
Total device leakage current to bus with loss of ground	$I_{leak} LOG$	---	---	100	μA
Network distance between any two ECU nodes	bus length	---	---	determined by network time constant	m

Notes:

- V_{batt} is measured at the ECU input power pins. All voltages are referenced to the local ECU ground pin.
- The minimum Network Time Constant and Signal Transition Time are determined by the EMC requirements. If these values are set too low, the ECU will not pass the required EMC tests.
- The signal transition time must be maintained regardless of bus RC distribution.
- The network total capacitance includes the capacitors placed on the ECUs as well as the capacitance of the bus wires, connectors, splices, PCB traces, etc.
- The network time constant incorporates the bus wiring capacitance. The minimum value is selected to limit radiated emissions. The maximum value is selected to ensure proper communication under all communication modes and is the absolute maximum allowed under normal and error operating conditions. This should be considered when determining the fusing for the vehicle. Not all combinations of Resistance (R) and Capacitance (C) are possible. Only those combinations of R and C, bus length, and PCB trace capacitance, etc., are possible that meet the specified network time constant.
- The high speed mode network time constant (τ_{hs}) is the product of (R_{tool} in parallel with R_{tl}) and C_{tool} . This time constant only applies when operating in the high speed mode with the tool resistor connected.
- ECUs shall not transmit unless all parameters in Table 3 are fully operational.
- The maximum transceiver input wake up voltage level shall be the smaller of $V_{ihWuFixed}$ maximum or $V_{ihWuOffset}$ maximum.
- The minimum transceiver input wake up voltage level shall be the smaller of $V_{ihWuFixed}$ minimum or $V_{ihWuOffset}$ minimum.
- The V_{ohWu} value is measured at the ECU bus pin. It includes an allowance for the voltage drop across the inductor Direct Current (DC) resistance. See 3.6.2 Line Inductor.
- The minimum transceiver output wake up voltage level shall be the smaller of $V_{ohWuFixed}$ minimum or $V_{ohWuOffset}$ minimum.
- The bus recessive state low voltage is the offset due to the ECU high side driver leakage current (I_{leak}) and does not include the ground offset voltage ($V_{g off}$). This leakage current limitation shall be in effect over the $6.0 V < V_{batt} < 26.5 V$. See 3.10 Operating Battery Power Voltage Range and 3.2.6.1 Bus Passive State Voltage Offset (V_{leak}).
- Signal delay time is measured from $V_{cmos il}$ on the Transmit Input (TxD) input pin to the $V_{ihMax} + V_{g off}$ level on the Bus Input/Output (I/O) pin for a recessive to dominant edge and is measured from $V_{cmos ih}$ on the TxD input pin to the $V_{ihMin} - V_{g off}$ level on the Bus I/O pin for a dominant to recessive edge. It includes both the internal transceiver propagation delay and the waveform rise time. The minimum value should be measured with the minimum network time constant and the maximum value should be measured with the maximum normal network time constant.
- High speed mode signal delay time is measured from $V_{cmos il}$ on the TxD input pin to the $V_{ihMax} + V_{g off}$ level on the Bus I/O pin with R_{tool} present for a recessive to dominant edge and is measured from $V_{cmos ih}$ on the TxD input pin to the $V_{ihMin} - V_{g off}$ level on the Bus I/O pin with R_{tool} present for a dominant to recessive edge. It includes both the internal transceiver propagation delay and the waveform rise time. The minimum value should be measured with the minimum network time constant and the maximum value should be measured with the maximum normal network time constant.

3.2.6.1 Bus Passive State Voltage Offset (V_{leak}). The Bus I/O circuit shall operate under the following limitations:

- When a node is awake and the bus is in the recessive state, the absolute maximum value of V_{leak} , which may be provided by the node output current, shall be as shown in Table 3 over the bus load resistance range $75 \Omega < R_{\text{il}} < 6.49 \Omega + 1\% \text{ k}\Omega$.
- In the sleep mode without a loss of ground, the node leakage current shall be as shown in Table 3.
- In any node or bus state, the contribution to bus leakage current by any node, which has a loss of ground condition, shall be as specified in Table 3.

Note: This circuit shall only source current to the bus.

3.3 Network Topology. The number of nodes, the total wire length of the system, the number and type of primary loads and the clock tolerance are all interrelated. Table E1 in Appendix E, is used in designing a SWCAN system to ensure that there are no errors due to the chosen system topology. An interactive Excel spreadsheet is available to System Architecture Engineers to determine the best system topology for each vehicle.

3.3.1 Network Wiring. Vehicle bus wiring shall conform to GMW3173 ISO Cable Selection and Physical Harness Requirements for Vehicle Bus Data Transmission.

3.3.2 Bus Electrical Load.

3.3.2.1 Distribution. The vehicle single wire communications bus may be configured with any combination and location of load circuits which meet the following criteria:

- Each ECU shall contain at least one unit device capacitance load and the series inductance. See 3.6.1 Capacitor.
- Bus Resistor unit loads (R_{ul}) may be uniformly distributed as unit loads among all ECUs or there may be one or more unit loads grouped together at a single physical location. Capacitive unit loads (C_{ul}) are a part of the ECU EMC/ESD protection and may not be grouped at a single physical location.
- The total network equivalent minimum resistance (R_{tl}) and maximum capacitance (C_{tl}) shall comply with the totals specified in Table 3.
- Primary loads may be implemented in some ECUs in a vehicle network to lower the overall network time constant and enable longer wire lengths. A primary load is equivalent to $2.1(R_{\text{ul}})$, i.e., 3.01 k Ω or 3.00 k Ω , 1%.

3.3.2.2 Power Dissipation.

3.3.2.2.1 The standard unit load resistor of 6.49 k Ω shall be able to dissipate a minimum of 0.12 W at 70 °C.

3.3.2.2.2 The standard primary load resistor of 3.01 k Ω shall be able to dissipate a minimum of 0.25 W at 70 °C.

3.3.2.2.3 The tool resistor load for high speed mode shall be able to dissipate a minimum of 2.0 W at 70 °C.

3.3.3 Bus Wire Length. There shall be no more than 60 m between any two network system ECU nodes (including off-vehicle service test tools) to accommodate 7 ns/m time delay effects on CAN bit synchronization timing requirements.

Bus wire length is also limited by the wire capacitance when routed close to body ground planes and/or harness ground wires. See Table 3, Note 4, for the limits for this effect on network time constant.

3.3.4 Loss of Ground Protection. The loss of ground by any single ECU, with or without an accompanying loss of V_{batt} , shall not cause any bus voltage offset that will disable normal communications. See Table 3. This shall be accomplished by including a loss of ground protection circuit in each ECU which shall disconnect the path from the bus to V_{batt} when a loss of ground occurs.

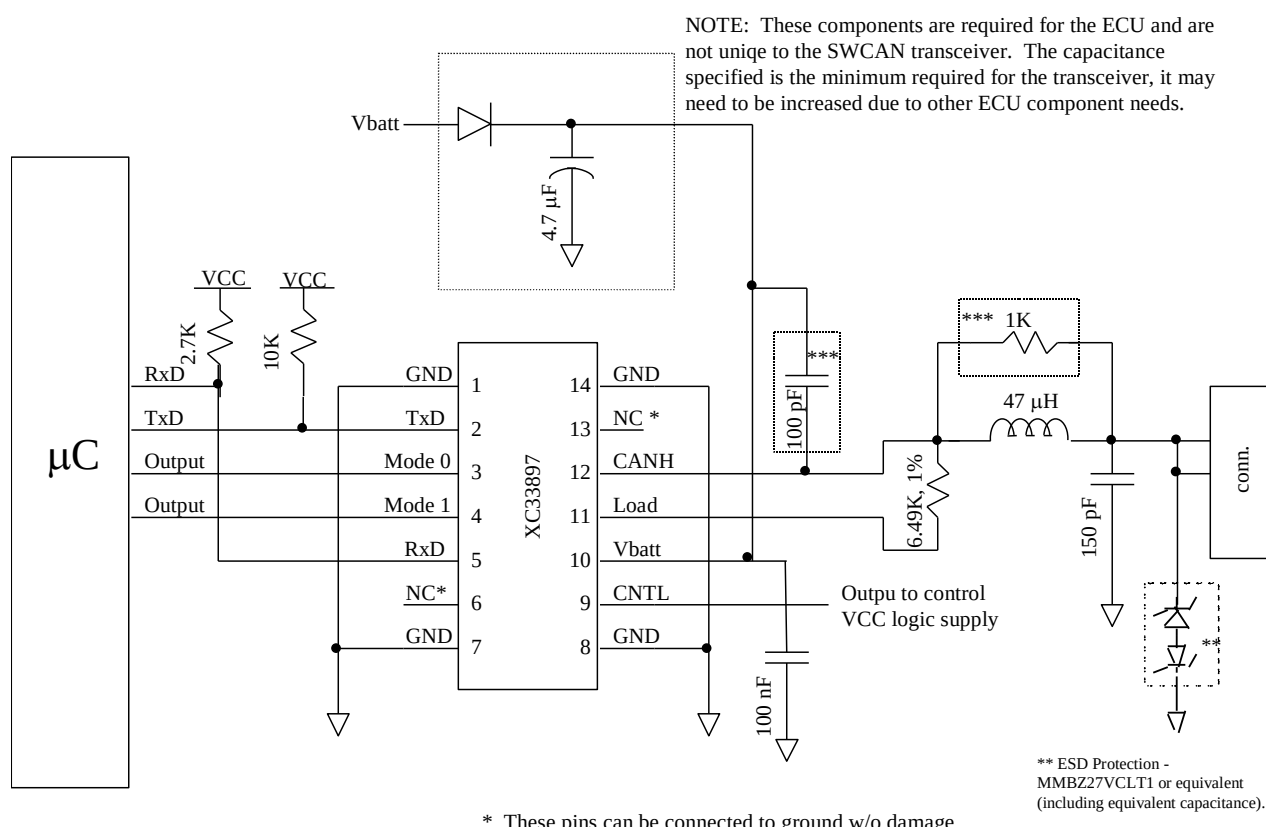
3.4 ESD Protection. The ECU CAN High (CANH) I/O pin shall withstand the following ESD without any damage to the ECU when subjected to the GMW3097 ESD, Remote Inputs/Outputs and ESD, Handling of Devices. See Table 4.

Depending on the network architecture being in a particular platform application, a reduced ESD severity level may be sufficient in certain cases. See GMW3097, General Specification for Electrical/Electronic Components and Subsystems, Electromagnetic Compatibility, and the CTS, SSTs or PSTs.

Table 4: Electrostatic Discharges

ECU Condition	Contact	Air (Non-Contact)	Test Required
Unpowered	± 6 kV	± 8 kV	GMW3097 ESD, Handling of Devices
Powered	± 8 kV	± 15 kV	GMW3097 ESD, Remote Inputs/Outputs

3.4.1 ESD Transient Suppressor. If needed to provide ECU ESD immunity, circuit element such as a transorb, back-to-back zener or a varistor device may be added to the network in one or more places to provide ESD protection. See Figure 1. The preferred method is that a central ESD suppressor be located in or near the Data Link Connector (DLC) if the individual ECUs are able to meet the unpowered ESD requirement. See GM-J1962 OBD interface for more information on the DLC on the Global General Assembly Service and Electrical site at URL: <http://avg.me.gm.com/standard/global/ggse.asp>. This central ESD suppression system shall be designed such that the suppressor cannot be disconnected while the DLC connector remains exposed and connected to any vehicle ECUs. See Figure 1 for the ESD component electrical location on the data link bus.



Note: CNTL = Control, conn. = Connector, NC = Not Connected, w/o = without.

Figure 1: Recommended Application Circuit for ECUs Utilizing the Freescale Transceiver

When ESD suppressor devices are used, they may add capacitance or introduce voltage and/or temperature variability to the network time constant and/or the bus maximum network capacitance. See Table 3. When central ESD protection is used, the maximum wire length allowed is reduced so the total network time constant is not affected. When ESD protection is implemented in an individual ECU, the local load capacitor must be reduced by the amount added by the ESD protection to keep the device time constant correct.

3.5 Radiated EMI Protection. ECUs shall conform to the electromagnetic interference requirements as indicated in the following GM EMC test specifications:

- GMW3097 General Specification for Electrical/Electronic Components and Subsystems, Electromagnetic Compatibility.
- GMW3103 General Specification for Electrical/Electronic Components and Subsystems, Electromagnetic Compatibility, Global EMC Component/Subsystem Validation Acceptance Process.

3.6 Bus Protection and Transient Suppression. The following devices may need to be added or, if already specified, shall meet these additional requirements to prevent damage to the bus components in the event of ESD and voltage transients, or to help in the meeting of the EMC requirements. See Figure 1.

3.6.1 Capacitor. The load capacitor shall have a minimum Direct Current Working Voltage (WVDC) of 100 V. **Note:** Capacitors smaller than 0805 may not be suitable. Typically type NPO and X7R types are suitable.

3.6.2 Line Inductor. An inductor, typical $L = 47 \mu\text{H}$, ESR as in Table 5, e.g., EPCOS B82432-A1473-K size 1812, or equivalent, available at electronic component suppliers, e.g., EPCOS, URL: <http://www.epcos.com/>, if required by the ECU to meet EMI susceptibility requirements, shall be placed between the SWCAN device and the load capacitor. The DC series resistance of this inductor shall be less than 3.5Ω . The line inductor needs to support a current of at least 70 mA DC and a transient current of up to 350 mA for $t < 20 \text{ ms}$. The power dissipation rating of the inductor shall be appropriate to a maximum loaded network under worst case environmental and electrical conditions. The inductor shall also be capable of withstanding the specified ESD conditions and fault tolerant modes, e.g., short-circuit of the bus line to ground.

If the inductor is not needed in a particular application, it is required that a zero ohm resistor be installed in the circuit at the inductor pc board location as a means of later installing the inductor for those vehicles and transceivers that may need the inductor. The PCB layout shall accommodate the inductor package sizes of 1210 and 1812 Surface Mount Device (SMD).

Table 5: Line Inductor Characteristics

Line Inductor Characteristic	Symbol	Minimum	Typical	Maximum	Units
Nominal inductance	L_{ind}	---	---	47	μH
EMC ESR if required	R_{ind}	---	---	3.5	Ω
DC capability of EMC inductor	$I_{\text{ind DC}}$	70	---	---	mA
Transient current capability of EMC inductor and reverse battery diode for $t < 100 \text{ ms}$	$I_{\text{ind 100ms}}$	350	---	---	mA

3.7 Fault Tolerant Modes. The network shall meet the requirements as defined per the following failure modes:

- **ECU Power Loss:** When up to 20% of the vehicle ECUs lose connection to power or experience a low-power condition, then they shall not interfere with normal communication among the remaining bus ECUs. The effective ECU bus load resistance shall be within $\pm 20\%$ of the nominal value in the ECUs. Upon return of power, normal operation shall resume without any operator intervention within a time period specified by the ECU CTS.
- **Bus Short to Ground:** Network data communications may be interrupted, but there shall be no damage to any ECU when the bus is shorted to ground. A network impedance of less than 50Ω between the bus and ground shall be considered a short to ground and continued communications are not guaranteed or required. Upon removal of the fault, normal operation shall resume without any operator intervention within a time period specified by the ECU CTS.

- **Bus Short to Battery:** Network data communications may be interrupted, but there shall be no damage to any device when the bus is shorted to positive battery less than 26.5 V ($V_{\text{batt}} < 26.5 \text{ V}$). A network impedance of less than 50 Ω between the bus and battery shall be considered a short and continued communications are not guaranteed or required. Upon removal of the fault, normal operation shall resume without any operator intervention within a time period specified by the ECU CTS.
- **Loss of ECU Connection to Ground:** When up to 10% of the vehicle ECUs lose their ground connection, this shall not prevent the remaining ECUs from normal communication. The ECU(s) shall implement this protection by interrupting the ground path to the bus load resistor when a loss of ground occurs. Upon removal of the fault, normal operation shall resume without any operator intervention within a time period specified by the ECU CTS.
- **A short or open in any single circuit of an ECU:** Except for power, ground, or serial data, a short or open shall not preclude the ability to communicate with that ECU for diagnostic purposes.

3.8 Transceiver Pin Out and Footprint. The transceiver shall have the printed circuit board pin assignments and footprint as shown in Appendix A (A1 through A9 and Figure A1).

3.9 Ground Offset Voltage. Ground offset voltage limits at the ECU, as specified in Table 3, must be maintained over the entire range of $6.0 \text{ V} < V_{\text{batt}} < 26.5 \text{ V}$.

3.10 Operating Battery Power Voltage Range.

3.10.1 Normal Battery Voltage Power Operation. Unless otherwise specified by the CTS, SSTs or PSTs, ECUs shall be capable of meeting all requirements specified in this document when the $V_{\text{batt ECU}}$ voltage, as measured at the ECU power input pin, is within the range of 7.0 V to 18 V, except for the High Speed mode which shall operate within the range of 8 V to 16 V. The ECU shall provide $V_{\text{batt IC}}$ to the bus transceiver within the range of 6.0 V to 18 V. See A8 in Appendix A.

3.10.2 Battery Power Over-Voltage Operation. For message frames which must occur at higher battery voltage conditions, some means of clamping V_{batt} may be required to allow communications to operate in the $18 \text{ V} < V_{\text{batt ECU}} < 26.5 \text{ V}$ range. The transceivers shall operate normally over the specified network loading between -40°C and $+85^\circ\text{C}$ up to 26.5 V as follows:

- Recessive state transceiver leakage current limits shall be maintained over this range.
- Communication shall not be disturbed by any node over this range.
- ECUs shall not sustain permanent damage when subjected to V_{batt} up to 26.5 V for $t < 1$ minimum.
- ECU must limit V_{batt} transients of greater than 40 V and/or duration greater than 10 ms.

Note: The transceivers may turn off due to internal IC over temperature above 85°C ambient.

3.10.3 Low Battery Voltage Operation.

3.10.3.1 For $V_{\text{batt ECU}} < 2.5 \text{ V}$. The bus shall be passive (not be driven dominant) and RxD shall be undriven (high).

3.10.3.2 For $2.5 \text{ V} < V_{\text{batt ECU}} < 6.0 \text{ V}$. The bus may operate in either the reduced output voltage mode or the passive mode as defined in 3.10.3.1.

3.10.3.3 For $6.0 \text{ V} < V_{\text{batt ECU}} < 7.0 \text{ V}$. The bus should operate in normal mode with a reduced dominant output voltage as specified in Table 3. This allows continued operation with reduced ground offset margin. In high speed mode, the bus shall operate in the reduced output voltage mode or the passive mode.

3.10.4 Battery Offset Voltage. The battery offset voltage between the battery input pins of any ECU limits specified in Table 3 must be maintained over the entire range of $7.0 \text{ V} < V_{\text{batt ECU}} < 26.5 \text{ V}$. If the battery offset requirements cannot be met, the network software must ensure that all devices remain awake until the vehicle returns to a sleep state. The battery offset requirements must be met at any time when the vehicle is in a sleep state.

3.10.5 Reverse Battery Blocking Diode. The reverse battery blocking diode voltage drop between the ECU's $V_{\text{batt ECU}}$ input pin and the transceiver's $V_{\text{batt IC}}$ input pin shall be in the range $0.4 \text{ V} < V_{\text{diode}} < 1.0 \text{ V}$. The diode function shall pass the reverse polarity test as specified in GMW3172 Reverse Polarity. See Table 6.