GM	WORLDWIDE ENGINEERING STANDARDS	General Specification	GMW3122

Dual Wire Controller Area Network (DWCAN) Physical Layer and Data Link Layer Specification

Contents

1 Introduction 4
1.1 Purpose. 4
1.2 Applicability. 4
1.3 Remarks. 4
2 References 4
2.1 External Standards/Specifications. 4
2.2 GM Standards/Specifications. 4
2.3 Additional References. 4
3 Requirements 5
3.1 Physical and Data Link Layer Characteristics. 5
3.1.1 Data link layer and two-wire physical layer according to ISO 11898 (High Speed CAN Physical Layer). 5
3.1.2 Capable of operating with CAN 2.0A protocol 5
3.1.3 Supports the enhanced protocol for extended clock tolerance. 5
3.1.4 Only performs bit resynchronization on recessive to dominant bus signal edges. 5
3.1.5 Meets GMW3173 5
3.1.6 Complies with GMW3097 and GMW3091 Electromagnetic Compatibility (EMC) requirements. 5
3.1.7 Intended to operate at ground offset voltages of up to 2.0 V temporarily. 5
3.2 Bus Operation. 5
3.2.1 General Requirements on Bus Operation for 12 V-Powered Devices. 5
3.2.2 General Requirements on Bus Operation for 42 V Powered Devices. 6
3.2.3 Bus Operation During Crank. 6
3.2.4 Tolerance of the CAN Bit Time. 7
3.3 Wake Up Techniques. 7
3.3.1 ECU Selective Awake Using a Wake Up Wire. 8
3.3.2 Wake Up on Bus Activity. 10
3.3.3 Wake Up on Continuous High Level Discrete Input. 11
3.4 ECU Requirements. 12
3.5 Bus Termination.. 13
3.5.1 Regular Bus Termination. 14

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3.5.2 Secondary Bus Termination. 14
3.5.3 Central Bus Termination Concept. 14
3.5.4 No Bus Termination. 14
3.5.5 Bus Termination in the Wiring Harness. 15
3.6 Bus Wiring Requirements. 15
3.6.1 Bus Wiring Configurations. 15
3.6.2 Connector Parameters. 15
3.7 ESD Protection of CAN Bus Pins. 15
3.7.1 General Requirements for Every ECU. 15
3.7.2 Specific Requirements for ECUs with Central ESD Protection Function. 15
3.8 Radiated Emission and Immunity.. 15
3.9 Bus Protection and Transient Suppression. 15
3.9.1 Line Common Mode Choke. 15
3.10 Fault Tolerant Modes. 16
3.10.1 ECU Loses Power. 16
3.10.2 ECU Loses Ground. 16
3.10.3 Any ECU that is Attached to the Network by Means of a Stub Connection and Does Not Provide Bus Termination Becomes Disconnected from the Bus Wires. 17
3.10.4 An ECU that Provides Bus Termination Becomes Disconnected from the Bus Wires. 17
3.10.5 Interruption of CANH and/or CANL Wire at Any Location. 17
3.10.6 CANH and/or CANL Wire Shorted to Ground. 17
3.10.7 CANH and/or CANL Wire Shorted to Battery Voltage. 17
3.10.8 CANH Wire Shorted to CANL Wire. 17
3.10.9 Presence of Proceeding Wiring Fault Conditions Should Not Prevent an ECU from Entering Low Power Standby Mode. 17
3.11 Requirements on the CAN Transceiver and CAN Protocol Controller. 17
3.11.1 CAN Transceiver Requirements. 17
3.11.2 CAN Controller Requirements. 20
3.11.3 CAN Controller Set-up. 22
3.12 High Speed Bus Requirements. 23
3.12.1 ECU Parameter Specifications. 23
3.12.2 Wiring and Network Topology. 24
3.13 Medium Speed Bus Requirements. 24
3.13.1 ECU Parameter Specifications.. 24
3.13.2 Wiring and Network Topology. 26
4 Validation. 26
4.1 General. 26
4.1.1 ECUs shall pass the tests in GMW14241. 26
4.1.2 Production Testing at Supplier's End of Line. 27

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4.2 Validation Cross Reference Index. Not applicable. ... 27
4.3 Supporting Paragraphs. ... 27
4.3.1 Development Testing. ... 27
4.3.2 Change Management. ... 27
5 Provisions for Shipping ... 27
6 Notes ... 27
6.1 Glossary. ... 27
6.2 Acronyms, Abbreviations, and Symbols. ... 27
6.2.1 Acronyms. ... 27
6.2.2 Abbreviations. ... 29
6.2.3 Symbols. Not applicable. ... 31
7 Additional Paragraphs ... 31
7.1 All parts or systems supplied to this standard must comply with the requirements of GMW3059 ... 31
8 Coding System ... 31
9 Release and Revisions ... 32
Appendix A: Reported Component Problems ... 33
Appendix B: Implementation Guidelines - Wake Up Wire ... 34
Appendix C ... 35
C1 High Speed Bit Timing Example ... 35
C1.1 Propagation Delay (t_{PROP}). ... 35
C1.2 CAN Bit Timing Requirements. ... 35
C1.3 All Acceptable Bit Timing Settings. ... 35
C1.4 Calculation of Bit Settings from Time Quanta. ... 36
C1.4.1 Implementation Example for CAN Bit Timing Parameters on a High Speed Bus. ... 36
Appendix D ... 38
D1 Medium Speed (125 kbits/s) Bit Timing Example ... 38
D1.1 Propagation Delay (t_{PROP}). ... 38
D1.2 Bit Timing Requirements. ... 38
D1.3 Compliant Bit Timing Settings for 125 kbits/s Medium Speed CAN. ... 38
D1.4 Calculation of Bit Settings from Time Quanta. ... 39
D1.4.1 Implementation Example for CAN Bit Timing Parameters on an Infotainment Bus. ... 40
D2 Medium Speed (95.238 kbits/s) Bit Timing Example ... 41
D2.1 Propagation Delay (t_{PROP}). ... 41
D2.2 Bit Timing Requirements. ... 41
D2.3 Compliant Bit Timing Requirements. ... 41
D2.4 Calculation of Bit Settings from Time Quanta. ... 42
D2.4.1 Implementation Example for CAN Bit Timing Parameters on an Infotainment Bus. ... 43

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1 Introduction

Note: Nothing in this standard supercedes applicable laws and regulations.

Note: In the event of conflict between the English and domestic language, the English language shall take precedence.

1.1 Purpose. This document specifies the physical layer requirements for a Carrier Sense Multiple Access/Collision Resolution (CSMA/CR) data link which operates on a dual wire medium to communicate among Electronic Control Units (ECU) on road vehicles at normal transmission rates of:

- High Speed Bus 500 kbits/s
- Medium Speed Bus 95.24 kbits/s and 125 kbits/s

This document is to be referenced by the particular Component Technical Specification (CTS) which describes any given ECU in which the dual wire data link controller and physical layer interface is located. The performance of the data link layer and physical layer is specified in this document. ECU environmental and other requirements shall be provided in the CTS. Functional as well as parameter requirements in this document generally apply over the applicable operating conditions and aging. This includes, for example, operating ambient temperature, operating supply voltage and age drift over component lifetime unless otherwise noted.

The intended audience includes, but is not limited to, ECU suppliers, component release engineers, platform system engineers and semiconductor manufacturers of Controller Area Network (CAN) controller and CAN transceiver Integrated Circuits (IC).

1.2 Applicability. This specification describes the data link and physical layer requirements for a dual wire data link capable of operating with CSMA/CR protocols such as CAN version 2.0A (standard frame format). All ECUs shall tolerate CAN version 2.0B (29-bit identifier extended frame format) messages, i.e., ECUs may not disturb such messages unless bit errors were detected. This serial data link network is intended for use in applications where a high data rate is required.

1.3 Remarks. Within this document the following conventions are applied:

The word "**Shall**" shall be used in the following ways:

a. To state a binding requirement on the network or the nodes which comprise the network, which is verifiable by external manipulation and/or observation of a node or the network.

b. To state a binding requirement upon a node's requirements document that is verifiable through a review of the document.

The word "**Must**" shall be used to state a binding requirement upon nodes on the network components which will have a corresponding ECU or component requirements document. These requirements will be verified as part of the component verification.

The word "**Should**" denotes a preference or desired conformance.

2 References

Note: Only the latest approved standards are applicable unless otherwise specified.

2.1 External Standards/Specifications.

ISO 7637-1	ISO 11898-1	ISO 16845	SAE J2284-1
ISO 7637-3	ISO 11898-2	ISO 21848	SAE J2284-3
ISO 11898	ISO 11898-5	SAE J2284	

2.2 GM Standards/Specifications.

GMW3110	GMW3091	GMW3172	GMW3191
GMW3059	GMW3097	GMW3173	GMW14241

2.3 Additional References.

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- A list of known CAN controller and transceiver issues is available in Global Document Management (GDM): Cabinets/Global Product Development/Global Engineering/Vehicle Systems & Technology (by

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VPPS)/Electrical Systems_Controls_Software/8_Electrical Function/87_Electrical Architecture/87_ECU Hardware & Network Infrastructure/ECU HW (ID)

- Applicable CTS, Subsystem Technical Specification (SSTS), or other Platform Specific Technical Specification (PSTS)
- CAN version 2.0A specification (standard frame format)
- CAN version 2.0B specification (29 bit identifier extended frame format)
- CG2223 Platform to Powertrain Electrical Interface (PPEI) Power and Ground Test Procedure (ID)

3 Requirements

3.1 Physical and Data Link Layer Characteristics.

3.1.1 Data link layer and two-wire physical layer according to ISO 11898 (High Speed CAN Physical Layer).

3.1.2 Capable of operating with CAN 2.0A protocol messages and tolerates CAN 2.0B protocol messages. If CTS, SSTS, or PSTS require conformance to CAN 2.0B, then the applicable interfaces shall be capable to transmit and receive standard, as well as extended frame format messages at any time during operation, that is support the protocol CAN 2.0B running in mixed-mode operation.

3.1.3 Supports the enhanced protocol for extended clock tolerance.

3.1.4 Only performs bit resynchronization on recessive to dominant bus signal edges.

3.1.5 Meets GMW3173 General Motors Local Area Network (GMLAN) architecture and bus wiring requirements.

3.1.6 Complies with GMW3097 and GMW3091 Electromagnetic Compatibility (EMC) requirements.

3.1.7 Intended to operate at ground offset voltages of up to 2.0 V temporarily.

3.2 Bus Operation.

3.2.1 General Requirements on Bus Operation for 12 V-Powered Devices. Per default the bus network when awake shall be fully functional, i.e., nodes shall be able to transmit and receive data, when the supply voltage at the ECU power input pins is within a range as specified in GMW3172 and/or the applicable CTS, SSTS or PSTS.

Note: In any case, bus communication shall be supported down to (at least) 9.0 V as measured at the ECU power/ground input pins.

Note: The requirement "shall support communication" does not imply that valid sensor data or actuator function must be supported at this voltage.

Note: Those devices which are involved in the vehicle immobilization function in some fashion typically need to support bus communication down to a supply voltage of 6.0 V.

If local ECU supply voltage had decreased below the specified minimum value, then the ECU shall resume bus receive and transmit capability within a time as specified in the ECU CTS. The time is measured from the point in time when the voltage increases to a level of 0.5 V higher than the specified minimum supply voltage until bus receive and transmit capability is resumed. If no time is specified in the CTS, then the ECU shall resume bus receive and transmit capability within t_{rsm}. See 3.10. In addition, if local ECU supply voltage decreases below the specified minimum value, then the ECU shall continue to support bus receive and transmit capability for a time of t > 2 ms.

Note: Operation at battery voltages of less than approximately 6.5 V typically implies usage of a low dropout voltage regulator.

The bus network shall support communication between powered nodes even when only two of the nodes on each network are sufficiently powered and the rest of the nodes are non-powered or under powered. Under powered is when battery voltage at the ECU power input pins is within the range of 0 V to 6.0 V unless otherwise specified. See applicable CTS, SSTS, or PSTS.

Nodes that are not able to communicate without disturbing the communication between other nodes, e.g., due to non-powered or under powered conditions, shall not be allowed to communicate. Nodes shall, under these conditions, close down communication circuits in a controlled manner.

Nodes that are in sleep condition shall not disturb communication between other nodes.

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In addition, ECUs that transmit and receive message frames which are required to support engine start, such as immobilizer data or Crank command, shall support communication in the range of 16 V to 18 V for 1 h and 18 V to 26.5 V for 1 minute (jump start condition) unless otherwise specified. See, e.g., GMW3172.

3.2.2 General Requirements on Bus Operation for 42 V Powered Devices. If an ECU is supplied exclusively by 42 V nominal power as main supply, then it shall comply with the following requirements on bus operation:

- The bus network when awake shall be fully functional, i.e., device shall be able to transmit and receive data, when the battery voltage at the ECU power input pins is within the range of 21.0 V to 50.0 V.
- Devices that are relevant for vehicle functions at Crank and/or which are not permitted to perform a reset or re-initialization during an engine Start and Stop cycle, shall be fully functional, i.e., devices shall be able to transmit and receive data, when a supply voltage starting profile according to ISO 21848 is applied. The ECU shall support error-free bus communication during and after the complete ISO 21848 starting profile.
- Devices, that are not relevant to vehicle functions during Crank and/or that are allowed to perform reset or re-initialization during an engine Start and Stop cycle, shall not cause error conditions to occur on the bus, i.e., there shall be no error frames during and after the application of the Crank pulse. The device shall resume bus communication within $t \leq t_{rsm}$ after the supply voltage has reached a level of 21.0 V unless otherwise specified in the applicable CTS, SSTS to PSTS.
- High Speed Bus networks shall operate if only two of the nodes on each network are sufficiently powered and the rest of the nodes are not powered, or are in a low supply voltage condition. Low supply voltage in this context means the battery voltage at the ECU power input pins is less than 21.0 V.
- High Speed Bus Nodes that are not able to communicate without disturbing the communication of other nodes while in low supply voltage condition shall automatically disable communication under that condition. Such nodes shall close down their communication function in a controlled manner while in low supply voltage condition.
- Nodes that are in sleep condition shall not disturb communication of other nodes.
- Physical interface drivers, which are not powered or under-powered, shall not disturb the communication on the network.

3.2.3 Bus Operation During Crank. Table 1 describes the bus network functionality during Crank. Refer to the applicable CTS, SSTS or PSTS to determine which devices are required to support this function during Crank.

Note: Each ECU that is supposed to contribute data for engine start purposes, e.g., immobilizer data, needs to support bus transmission function during Crank, depending on PSTS requirements.

Voltage levels and timing of the Crank pulse are specified in GMW3097 and CG2223.

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Table 1: ECU Functional Status at Crank

Period	Description
Run/Crank Transition	The bus network shall be fully functional, nodes shall be able to transmit and receive data.
$Crank_1$	Bus functionality during this period shall be stated in the CTS, SSTS or PSTS. Under no circumstances shall any node disturb ongoing bus communication. Ongoing message transmissions should be concluded normally, e.g., without causing error conditions on the bus.
$Crank_2$	See $Crank_1$.
$Crank_3$	Upon return of power nodes shall resume data receive and transmit function within a time period being specified in the CTS, SSTS or PSTS. If such time is not specified in the CTS, SSTS or PSTS, then the node shall resume receive/transmit function within $t \leq t_{rsm}$. See 3.10. Under no circumstances shall any node disturb ongoing bus communication, e.g., due to startup initiation.
Crank/Run Transition	The bus network shall be fully functional, nodes shall be able to transmit and receive data.

3.2.3.1 Transferred 42 V Crank Pulse to 14 V Side, e.g., Via 42 V/14 V Direct Current (DC) to DC Converter. All designated ECUs shall be fully functional, i.e., device shall be able to transmit and receive data on high speed CAN when a test pulse according to Table 2 is applied. Designated ECUs shall support error-free bus communication and are not allowed to perform reset or re-initialization during and after the complete test pulse.

Note: See the CTS, SSTS, or PSTS to determine which devices shall support operation while a transferred Crank pulse is present.

Table 2: Test Pulse

Nominal Voltage	Minimum Pulse Voltage	Pulse Duration	Rise and Fall Time
13.8 V	7.0 V	1 s	5.0 ms

3.2.4 Tolerance of the CAN Bit Time. Any CAN interface of an ECU must be compliant to an overall tolerance of the CAN bit time length as specified in 3.12 and 3.13, i.e., CAN bits being transmitted by an ECU shall meet this tolerance requirement and each ECU shall be capable to receive messages from other ECUs which meet this requirement. The tolerance value is applicable over operating conditions and aging, e.g., temperature, supply voltage and age drift over specified vehicle temperature including component life time. This is to ensure proper operation of the network, e.g., with respect to the CAN bus resynchronization function.

Careful analysis of the bit time tolerance is recommended when ceramic resonators and/or Phase Locked Loop (PLL) clocks are considered. The permitted tolerance of the oscillator circuit is reduced when a PLL clock is used for the CAN data link layer controller. For example, the suitable oscillator tolerance would be 0.1%, for the case where the PLL circuit would exhibit an add-on tolerance of 0.35% (or 0.4% at 125 kbits/s or 95.2 kbits/s).

When a ceramic resonator with a maximum tolerance of 0.3% is used with a PLL, the add-on clock tolerance of the PLL is limited to 0.15% (or 0.2% at 125 kbits/s or 95.2 kbits/s) over a single bit time. At a bus speed of 500 bit/s, this is equivalent to 0.15% of 2 µs, or 3 ns maximum jitter over 2 µs. At a bus speed of 125 kbits/s, this is equivalent to 0.2% of 8 µs, or 16 ns maximum jitter over 8 µs. At a bus speed of 95.2 kbits/s, this is equivalent to 0.2% of 10.5 µs, or 21 ns maximum jitter over 10.5 µs.

3.3 Wake Up Techniques. Dual Wire Controller Area Network (DWCAN) allows three (3) types of ECU awake/sleep techniques as follows. If a wake up technique is used, then it must conform to GMW3097 EMC requirements.

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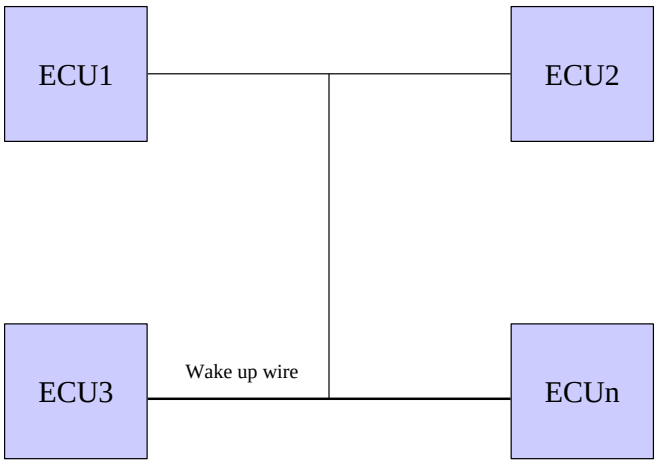
1. Selective awake by an awake pulse. When used, it will be possible to communicate on the DWCAN network without forcing nodes that are not needed to stay awake. See 3.3.1.
2. Non-selective wake up on presence of CAN bus communication. When used, it will force nodes to stay awake as long as ongoing communication occurs. This is the **recommended concept for new designs**. See 3.3.2.

Note: This concept requires employing CAN transceiver products which support node wake up upon bus traffic. See 3.11.1.2.11.

3. Non-selective awake by a continuous high level discrete signal, typically called "Communication Enable". When used, it will force nodes to stay awake as long as the discrete signal is at a high level, e.g., Ignition signal. See 3.3.3.

Usage of awake/sleep techniques are optional. Whether and how the proceeding approaches shall be used is to be defined in the applicable PSTS data bus implementation document. **Note:** More than one of the proceeding concepts can apply to a particular ECU or network, e.g., it may be necessary in a subnet for an ECU to be present which supports wake up on bus traffic (see 3.3.2) and in addition to control the discrete wake up line (see 3.3.1).

3.3.1 ECU Selective Awake Using a Wake Up Wire. ECU selective awake is accomplished by a dedicated wire, a wake up wire. See Figure 1.



n <= 22

Figure 1: Wake Up Wire

The wake up wire is a common wire for all ECUs connected on the same bus. Each ECU needs one pin assigned for this function. The following parameter specifications of the wake up wire concept support connection of up to 22 ECUs. The wake up wire signal is an input/output interface, i.e., the ECU can send and receive the wake up signal on the same wire.

3.3.1.1 Concept Description.

3.3.1.1.1 The wake up output requirements are:

- The wake up voltage V_{twu} shall be applied on the wake up wire for a time t_{wuo}.
- Wake up is generated as a hardware signal on the wake up wire. The ECU generating this signal shall wake up or notify all ECUs connected on the same bus.

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3.3.1.1.2 The wake up input requirements are:

- An ECU currently in sleep mode, that detects a voltage in excess of $V_{r\,wu}$ for a time longer than $t_{r\,wui}$ applied on the wake up wire, shall switch to active mode.
- The wake up pulse shall also affect an ECU in active mode, not only an ECU that is in sleep mode, i.e., an ECU that is in active mode shall be able to detect the wake up pulse.
- Each ECU shall be able to generate wake up pulses and detect wake up pulses on the wake up wire.

3.3.1.2 Wake Up Wire Basic Requirements.

3.3.1.2.1 An ECU should not change power modes when subjected to GMW3097 EMC conditions. For example, the ECU shall not take conducted/coupled immunity test conditions as valid wake up or go to sleep events.

3.3.1.2.2 Fault Tolerant Modes.

3.3.1.2.2.1 ECU Power Loss. An ECU shall not interfere with wake up function among other ECUs during a loss of power or low supply voltage condition. Upon return of power, normal wake up operation shall resume without any operator intervention within a time period being specified by the ECU CTS. If a time period is not specified in the CTS, then the ECU shall resume operation within $t \leq t_{rsm}$. See 3.10.

3.3.1.2.2.2 Wake Up Wire Short to Ground. Wake up function may be interrupted, but there shall be no damage to any ECU when the wake up wire is shorted to ground or to a negative voltage down to V_{wu} = -5 V. Upon removal of the wiring fault, normal wake up operation shall resume without any operator intervention within a time period being specified by the ECU CTS. If a time period is not specified in the CTS, then the ECU shall resume normal operation within $t \leq t_{rsm}$.

3.3.1.2.2.3 Wake Up Wire Shorted to Battery Voltage. Wake up function may be interrupted, but there shall be no damage to any ECU when the wake up wire is shorted to a positive battery voltage of V_{wu} = 16 V without time limit, 18 V for 1 h and 26.5 V for 1 minute. Upon removal of the wiring fault, normal wake up operation shall resume without any operator intervention within a time period being specified by the ECU CTS. If a time period is not specified in the CTS, then the ECU shall resume normal operation within $t \leq t_{rsm}$.

3.3.1.2.3 The ECU´s wake up input/output function shall be fully functional when the ECU is powered with a supply voltage of V_s = 6.5 V to 16.0 V. When the ECU supply voltage has decreased below V_s = 6.5 V, then the wake up function shall resume operation when the supply voltage reaches a level of V_s = 7 V or higher.

Note: This operating supply voltage range for the wake up wire function only applies if not otherwise specified in the applicable CTS, SSTS, or PSTS.

3.3.1.3 Wake Up Output Requirements. The parameter specifications apply over operating conditions and aging, e.g., temperature, supply voltage and age drift over specified vehicle temperature and component life time unless otherwise noted. See Table 3.

Table 3: Wake Up Wire Output Parameter Specifications

Parameter	Conditions	Symbol	Minimum	Nominal	Maximum	Unit
Low level output voltage	R_L > 100 kΩ	V_{wuol}	-0.3	0	+0.3	V
High level output voltage	R_L = 240 Ω	V_{wuoh}	Minimum [9, (V_s - 1.7)]	V_s	Maximum [16,(V_s + 0.3)]	V
Short circuit output current	V_{wu} = 0 V	V_{wuohsc}	25	---	250	mA
Transmit wake up pulse length	See Section 4, Validation	t_{wuo}	400	500	600	ms
Input capacitance	---	C_{wuin}	---	---	20	nF

Conditions: 6.0 V ≤ V_s ≤ 18 V, -40 °C < T_{amb} < T_{ambMax} unless otherwise noted. T_{ambMax} shall be specified in the CTS.

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3.3.1.4 Wake Up Input Requirements. See Table 4.

Table 4: Wake Up Wire Input Parameter Specifications

Parameter	Conditions	Symbol	Minimum	Nominal	Maximum	Unit
Low level wake up input voltage	---	V_{wuil}	-2.0	0	+2.0	V
High level wake up input voltage	---	V_{wuih}	4.5	V_s	16	V
Wake up input filter time	See Section 4, Validation	t_{wui}	0.1	---	2.0	ms
Low level input current	$V_{wu} = V_{wuilMax} = 2.0$ V	I_{il}	0.1	0.24	0.35	mA
High level input current	$V_{wu} = V_{battNom} = 12$ V Note 1	I_{ih}	1.2	1.4	2.0	mA
Input capacitance	---	C_{in}	0	---	1	nF

Note 1: This requirement can be implemented, for example, using a pull down resistance to ECU ground potential. See Appendix B.

Conditions: 6.0 V ≤ V_s ≤ 18 V, -40 °C < T_{amb} < T_{ambMax} unless otherwise noted. T_{ambMax} shall be specified in the CTS.

3.3.2 Wake Up on Bus Activity. DWCAN transceivers which support this wake up method have to provide a low power standby/power down mode. The microcontroller (µC) sets the transceiver to standby before it enters standby/power down mode. Wake up shall be performed by an ECU upon detection of any activity on the bus. In standby mode the transceivers of the involved ECUs detect recessive to dominant transitions and generate a wake up signal to the µC. **Note:** It is necessary to apply appropriate bus input signal filtering against inadvertent wake ups. Specifically, devices shall:

- Devices shall ***not*** wake up when transient bus dominant conditions occur with a duration of less or equal to t_{fwu_min} = 0.75 µs. This means the device shall continue to meet the quiescent current limit for sleep mode.
- Devices shall wake up if a valid bus traffic detection condition is present, that is the bus has been in "dominant" condition for a duration of at least t_{fwu_max} = 5 µs. It is acceptable to utilize devices that require multiple transitions from recessive to dominant to recognize a valid wake up event within a single bus frame; however, the device shall not require more than two recessive to dominant or dominant to recessive transitions.
- When the bus is in dominant state at the point in time when the ECU attempts to enter a low power mode, then the ECU shall enter the low power mode and shall remain in the low power mode until there is a valid wake up condition. In this case, a valid wake up condition requires at least one recessive to dominant transition on the bus, unless otherwise explicitly specified for a particular ECU.

3.3.2.1 Requirements on Valid Wake Up Request Messages. It is important to note a bus frame must meet certain characteristics in order to enable reliable wake up request functionality. The frame that is used for the purpose of bus wake up request must contain the pattern:

- The frame must contain at least two (2) instances consisting of at least three (3) consecutive dominant bits separated by a pattern that includes at least one phase consisting of at least three (3) consecutive recessive bits. At data rates higher than 500 kbits/s, the specified phases have to contain more than the proceeding described number of consecutive bits.
- The frame must not contain any data bytes.

Exception: If an ECU-specific frame header is utilized for the purpose to facilitate bus wake up requests, then presence of data bytes is permitted.

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Note: The described pattern may be located anywhere in the transmitted bus frame, e.g., including Identifier (ID) field, Data Length Code (DLC), fixed form bits, Cyclic Redundancy Check (CRC), Start of Frame (SOF) and stuff bits.

3.3.3 Wake Up on Continuous High Level Discrete Input. This approach foresees that ECUs shall enable/disable the communication function of the primary High Speed General Motors Local Area Network (HS GMLAN) interface based on the voltage level of a dedicated input. There is (at least) one ECU which controls the voltage on this dedicated wake up line. Devices which provide output control capability for the dedicated wake up line shall also provide the input function specified that follows. **Note:** It is possible that only a subset of ECUs of a subnet is connected to the wake up line. The CTS specifies whether the ECU shall have a wake up output function and/or whether it shall have a wake up detection input function. For ESD protection requirements refer to GMW3097. Wake up outputs and inputs shall be proof against short circuits to any voltage between -3 V and +26.5 V.

ECUs which shall be able to request wake up of the network shall meet the following requirements at the particular output: In principle, the wake up wire output shall provide open collector characteristic. When asserted, the ECU shall typically output battery voltage level. When not asserted, the ECU shall exhibit a weak low state.

Note: Parameter specifications apply over operating conditions and aging, e.g., temperature, supply voltage and age drift over specified vehicle temperature and component life time unless otherwise noted.

ECUs which shall provide wake up input detection capability shall meet Table 5 and Table 6 requirements at the particular input. The ECU shall have a logic input that connects to the continuous high level signal. This input shall be used for detecting presence of a wake up request. In principle, the wake up wire input shall provide weak pull down to ground potential characteristic. For an example circuit, see Figure B1 in Appendix B.

Table 5: Wake Up Line Output Requirements

Parameter	Conditions	Symbol	Minimum	Nominal	Maximum	Unit
Active state output voltage	R_L = 240 Ω	V_{wuoh}	V_s - 1.0	V_s	Maximum [26.5, (V_s + 0.3)]	V
Active state output current	$V_s \geq 9$ V	I_{oh}	50	---	200	mA
Active state short circuit output current	V_{wu} = 0 V and/or V_{wu} = 26.5 V	V_{wuohsc}	---	---	250	mA
Inactive state output leakage current	V_{wu} = +12 V	$I_{LEAKmax}$	-10	0	+10	uA

Conditions: 6.0 V ≤ V_s ≤ 26.5 V, -40 °C < T_{amb} < T_{ambMax} unless otherwise noted. T_{ambMax} shall be specified in the CTS. V_{wu} corresponds to the voltage at the communication enable Input/Output (I/O) pin of the ECU.

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Table 6: Wake Up Line Input Requirements

Parameter	Conditions	Symbol	Minimum	Nominal	Maximum	Unit
High level input current	$V_{wu} = V_{sNom} = 12$ V	I_{ih}	1.2	1.4	2.0	mA
Low level input current	$V_{wu} = 2.0$ V	I_{il}	0.1	0.24	0.35	mA
High level wake up input voltage	---	V_{wuih}	4.0	V_s	26.5	V
Low level wake up input voltage	---	V_{wuil}	-2.0	0	2.0	V
Edge input recognition time	See Section 4, Validation	t_{wui}	1	---	40	ms

Conditions: 6.0 V ≤ V_s ≤ 26.5 V, -40 °C < T_{amb} < T_{ambMax} unless otherwise noted. T_{ambMax} shall be specified in the CTS.

3.4 ECU Requirements. ECU requirements for high speed CAN shall be according to SAE J2284-3. ECU requirements for medium speed CAN shall be according to ISO 11898-1 and ISO 11898-2 (High Speed Medium Access Unit).

In addition, a medium speed ECU designated for operation at 125 kbits/s shall comply with SAE J2284-1 unless otherwise specified in this document.

All ECUs shall be proof against Table 7 conditions being applied to the bus lines, CAN High (CANH) and CAN Low (CANL), unless an explicit exemption was made per applicable PSTS.

Table 7: ECU Absolute Maximum Ratings [Note 1, Note 2]

Parameter	Symbol	Minimum	Maximum	Unit	Conditions/Comment
CANH and CANL voltage	V_{CAN_DC}	-5	+18	V	No deviations allowed after removal of condition. No time limit, all modes, e.g., normal and sleep, recessive, and dominant bus output states. [Note 3]
CANH and CANL voltage for 1 minute	V_{CAN_1m}	---	+26.5	V	No deviations after removal of condition. Time limit of 1 minute, all modes, recessive and dominant bus output states.
Source voltage at coupling of conducted transients to CANH and CANL lines, see GMW3097	V_{CAN_trn}	-150	+100	V	No deviations allowed after removal of condition. No functional deviations allowed during exposure. All operating modes, recessive and dominant bus output states.
ESD protection for CANH and CANL	V_{CAN_ESD}	-4	+4	kV	Human Body Model (HBM) contact discharge, powered and unpowered. Additional requirements may apply, e.g., per GMW3097. [Note 4]

Note 1: The device shall survive the interruption of its connection to ground without time limit at battery voltages up to 16 V, i.e., a (locally) negative voltage is present at the bus pins relative to the locally disconnected ECU ground pin.
Note 2: When the ECU is in low power mode, the bus outputs CANH and CANL shall output a voltage of 0 V nominal to the bus via an output resistance as specified in ISO 11898-2. See parameter internal resistance of CANH and CANL.
Note 3: If the physical bus interface was subjected to an over temperature shutdown condition, then it shall resume regular operation within 10 s unless a component specific exception were made per CTS.
Note 4: For more detailed EMC and ESD requirements and test conditions applicable to the CAN bus interface of an ECU, see GMW3097. There are requirements on ESD for packaging and handling and ESD during operation of the device (power on mode).

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3.5 Bus Termination. Each network needs to be equipped with two bus termination units. For high speed CAN buses crossing the PPEI border per default, one bus termination shall be implemented on the platform side and one termination on the powertrain side unless otherwise specified. Per default, this circuit shall be implemented in every ECM or Powertrain Control Module (PCM) component unless explicitly otherwise specified. Bus termination characteristics shall meet the SAE J2284-3 specification unless otherwise specified in this document. All electronic control units shall package protect for a bus termination circuit on the Printed Circuit Board (PCB) unless otherwise specified per CTS, SSTS or PSTS. Whether the bus termination components (R1, R2, and C1) are to be populated in a certain control unit shall be specified in the applicable SSTS, CTS or PSTS.

When the ECU is in low power mode, the bus termination unit shall not drive a certain common mode voltage onto the bus, i.e., the output V_{split} shall be in high impedance state with an output leakage of less than ± 100 µA for -3 V < $V_{CAN_H/L}$ < +16 V. **Note**: The differential resistance as measured between CANH and CANL shall always be present, also in low power mode.

The bus interface and termination circuit shall be applied as in 3.5.1 through 3.5.5 and Figure 2.

Important Note: If a bus termination shall be placed outside of a control unit, e.g., in the wiring harness, then a different circuit applies.

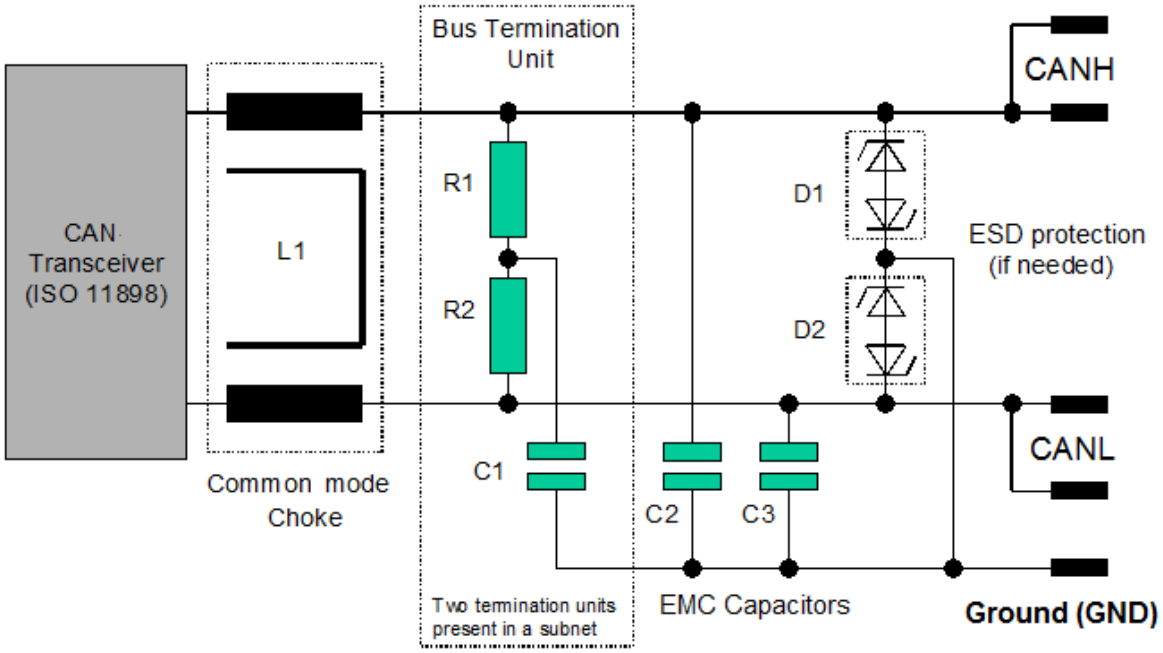

Figure 2: CAN Bus Application Circuit

The requirements on the Common Mode Choke L1 are specified in 3.9.1. The center tap of the termination unit shall be connected to the reference voltage output of the bus transceiver IC if such mechanization is suggested by the semiconductor manufacturer for the particular transceiver product. **Note:** This path may need to be interrupted if the used transceiver product changes.

Capacitors C2 and C3 shall be chosen as follows: 40 pF < C_{i_nom} < 100 pF, tolerance less or equal to 10%, working voltage 100 V or higher. The actual capacitance value of both parts shall be close to each other to optimize EMC behaviors. See 3.12.1. If a special ESD protection circuit is used, see 3.7, then C2 and C3 might have to be chosen with a lower value or be omitted, depending on the capacitance of the protection circuit. Both capacitors shall be placed close to the bus connector with minimum trace length.

If ESD protection elements D1, D2 are needed, acceptable parts are PESD24VS2UAT, PESD1CAN, PESD2CAN or MMBZ27VCLT1G/SZMMBZ27VCLT1G, or equivalent, available at electronic component

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