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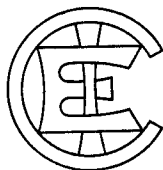
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Diagrams, charts, tables
Part 7: Preparation of logic diagrams

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DIAGRAMS, CHARTS, TABLES

Part 7: Preparation of logic diagrams

FOREWORD

- 1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.
- 2) They have the form of recommendations for international use and they are accepted by the National Committees in that sense.
- 3) In order to promote international unification, the IEC expresses the wish that all National Committees should adopt the text of the IEC recommendation for their national rules in so far as national conditions will permit. Any divergence between the IEC recommendation and the corresponding national rules should, as far as possible, be clearly indicated in the latter.

PREFACE

This standard has been prepared by Sub-Committee 3B: Preparation of Diagrams, Charts and Tables. Item Designation, of IEC Technical Committee No. 3: Graphical Symbols.

Drafts were discussed at the meetings held in Milan in 1975 and in Oslo in 1976. As a result of this latter meeting, a draft, Document 3B(Central Office)19, was submitted to the National Committees for approval under the Six Months' Rule in December 1976.

The National Committees of the following countries voted explicitly in favour of publication:

Australia	France	Spain
Austria	Israel	Sweden
Belgium	Japan	Switzerland
Canada	Korea (Republic of)	Turkey
Denmark	Netherlands	United Kingdom
Egypt	South Africa (Republic of)	Yugoslavia
Finland		

The document was not published at that time, however, as, during the preparatory work, it was realized that additional material would be needed. A first draft for this supplement, comprising Clauses 11, 14, 15 and Appendices A and B, was discussed at the meeting held in Paris in 1978. As a result of this meeting, a combined draft, Document 3B(Central Office)22, which included the contents of Document 3B(Central Office)19 and the text of the draft supplement, was submitted to the National Committees for approval under the Six Months' Rule in May 1979.

The National Committees of the following countries voted explicitly in favour of publication of the draft supplement:

Australia	Germany	Sweden
Austria	Israel	Switzerland
Belgium	Italy	Turkey
Canada	Japan	Union of Soviet
Egypt	Norway	Socialist Republics
Finland	South Africa (Republic of)	United Kingdom

Other IEC publications quoted in this standard:

Publications Nos. 113-3: Diagrams, Charts, Tables, Part 3: General Recommendations for the Preparation of Diagrams.

113-4: Part 4: Recommendations for the Preparation of Circuit Diagrams.

117-15: Recommended Graphical Symbols, Part 15: Binary Logic Elements.

617-12: Graphical Symbols for Diagrams, Part 12: Binary Logic Elements (*in preparation*). Until this standard is published reference should be made to Publication 117-15, quoted above.

DIAGRAMS, CHARTS, TABLES

Part 7: Preparation of logic diagrams

1. Scope

This standard gives additional recommendations for the preparation of diagrams with respect to the use of symbols for logic elements.

2. Related publications

The other parts of IEC Publication 113* are concerned with matters of drawing practice and provide additional guidance.

Graphical symbols for diagrams are given in the relevant parts of IEC Publication 117: Recommended Graphical Symbols, and IEC Publication 617: Graphical Symbols for Diagrams*.

3. Symbols

3.1 General

Symbols for binary logic elements and some rules for the use of the symbols are given in IEC Publication 617-12.

In accordance with Sub-clause 3.4 of IEC Publication 113-3, their size should be governed by the space necessary for internal annotations and the length of the side needed to accommodate input and output lines at an acceptable spacing.

Input and output lines are preferably placed on opposite sides of the symbol and should join the outline of the symbol at right angles. A symbol for a binary logic element may have any number of inputs and outputs provided that the symbol definition requirements as contained in IEC Publication 617-12 are met.

The special rules for complex elements must be observed.

Most logic diagrams will also require the use of symbols drawn from some of the other parts of IEC Publications 117 and 617.

3.2 Combination of symbols

Rules for combining symbols for basic operations are given in IEC Publication 617-12. Symbols representing hardware elements which are contained in one physical package may also be combined providing the interconnections are not accessible to the user and the rules mentioned above are applied.

* See inside back cover.

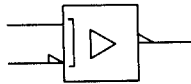
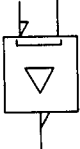
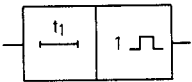
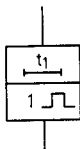
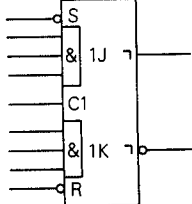
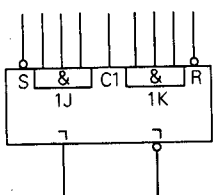
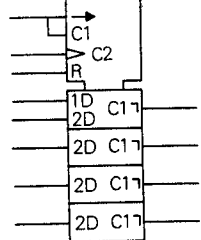
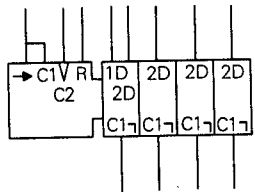
3.3 Symbol orientation

The symbols contained in IEC Publication 617-12 have been designed so that inputs appear on the left and outputs on the right, and this orientation is preferred. However, the other symbol orientation in which inputs appear at the top and outputs at the bottom may also be used, provided the following rules are observed:

- In general, outputs appear on the opposite side of the symbols from the inputs.
- The rules for the placement of the qualifying symbol(s) for the device function given in IEC Publication 617-12 are obeyed.
- Sufficient space is provided to avoid confusion between the qualifying symbol(s) for the function and the input and output labels.
- Strings of characters, forming qualifying symbols or labels, should preferably appear in normal reading order. Each input (output) label is centred with respect to its input (output) line.
- The orientation of qualifying symbols for negation, polarity, grouping dynamic input, inhibit and amplification with respect to the connection lines is unchanged.

Table I gives examples of symbol orientation.

TABLE I

Preferred orientation	Other permitted orientation
	
	
	
	

4. Logic conventions

- 4.1 A logic diagram may be prepared using a single logic convention, either positive or negative, to define the relationship between logic states and the nominal values of corresponding physical quantities. In this case, and in the case where no such relationship needs to be established, the symbol for logic negation is used where necessary; the symbol for logic polarity shall not be used. The convention in use should be clearly shown on the diagram or in referenced documentation (see Figure 2, page 28).

Note. — Different logic conventions may be used for different parts of the same diagram, e.g. on either side of an interface between contrasting technologies—the convention applying to each part being clearly shown and the areas of the diagram to which each applies being clearly delineated.

- 4.2 Alternatively the relationship between the logic state and the nominal value of the corresponding physical quantity at each input and output of every logic element may be given by means of the absence or presence of the symbol for logic polarity (see Figure 3, page 29). In this case the symbol for logic negation shall not be used.
- 4.3 It is sometimes convenient to represent the logic convention by means of idealized waveforms with indications of the logic states and, if necessary, of the nominal value of corresponding physical quantities. Additional information is provided in Appendix B.

5. Contents of a logic diagram

A logic diagram—which may consist of several sheets—should be prepared for each distinct unit, or assembly of units, intended to fulfil a defined purpose. It may thus relate to a single unit or to several units which together form a functional entity.

In cases where the logic diagram cannot be shown on a single sheet the division into separate sheets should be based on the purpose of the diagram.

6. Layout of a diagram

The most important consideration is the adoption of a layout which best aids understanding of the diagram. The layout should be such that the principal flow of information is from left to right of the diagram—otherwise it should be from top to bottom. Where the direction of information flow is not obvious, lines carrying information should be marked with an arrow-head which must not be placed adjacent to any other symbol or label.

Functionally related symbols should be grouped and placed as close to one another as the requirements of annotation and the avoidance of overcrowding will allow.

Lines should be drawn horizontally or vertically except in those isolated cases where oblique lines aid the clarity of the diagram.

For a signal feeding a multiplicity of elements the use of a single straight line with appropriate indications of T-junctions to the elements aids comprehension of the diagram.

The recommendations for grouping and omission of lines given in Clause 4 of IEC Publication 113-3 apply also to lines representing information flow and connecting lines in logic diagrams.

7. Unused elements

Any hardware elements which are not used—e.g. inputs or outputs or complete elements in a multiple element package—may be shown. It is then important to identify the unused elements and the corresponding pin numbers.

8. Distributed connections

The connection of certain logic elements to achieve the effect of an AND or an OR operation without the use of additional logic elements may be depicted as shown in IEC Publication 617-12. All external components required to implement the facility should be shown or referred to in a table.

Any interrupted line should be appropriately cross-referenced in accordance with IEC Publication 113-4.

9. Complex logic units

The correct way to represent a complex logic unit is to use a symbol developed in accordance with the rules given in IEC Publication 617-12. If this is not desirable owing to the complexity of the function, then the symbol used can be a simple rectangle containing a description of the function or a reference to appropriate documentation. Standard labels should be used for inputs and outputs when possible.

If a symbol for a complex function has to be repeated on a diagram, the repetitions may be shown as simple rectangles with appropriate references.

10. Symbols for logic elements

Preferably each logic element should be shown by that symbol which best depicts the logic function actually performed by the element in the system. Thus, in Figure 2, page 28, the same type of hardware element (designated D3) is represented once by the symbol for an OR element with negated inputs and elsewhere by the symbol for an AND element with negated output (NAND).

Additional information is provided in Appendix B.

11. Labelling of lines

11.1 General

Labelling of lines can greatly promote the understanding of a diagram and facilitate the maintenance of a logic system provided that the signals are named intelligently and the name allocation is based on carefully named system functions.

Signal line names should be informative and unambiguous. The space available on the diagram or allocated in the data file usually limits the allowable length of signal names. Identical names shall not be applied to different signal lines, no matter how similar the

function. Every effort should be made to use mnemonic names and standard abbreviations (for examples, see Figures 2 and 3, pages 28 and 29). The mnemonics and abbreviations used should be explained on the diagram or in supporting documentation.

In general, the characters comprising the total signal identification provides three types of information:

the first gives signal cross-reference information;

the second, referred to in this standard as the signal name, gives generally a functional description;

the third (used only on diagrams employing the polarity indicator) gives information which relates the logical truth of a function with its logic level.

Only the second and third types of information are dealt with in this standard.

11.2 Signal names

The signal name is an abbreviation of a statement which can be either true or false. For example: the name ALARM is associated with the statement "ALARM IS ACTIVATED".

True and complement signals of the same function are often required on binary logic diagrams. The preferred method to denote the complement of a signal is by use of a negation bar over the signal name, thus: ALARM, $\overline{\text{ALARM}}$.

If only an in-line notation can be used, the notation adopted to designate the complementary signals shall be explained on the diagram or in supporting documentation, for example ALARM-N.

Convention: The relation between the true value of a statement, represented by a signal name, and the logic state of the binary-digital variable assigned to the signal with that signal name, is given by the following general convention:

True always corresponds to the logic 1-state.

False always corresponds to the logic 0-state.

For example: the signal name ALARM implies that if ALARM is true, the signal is in its 1-state. Conversely, $\overline{\text{ALARM}}$ implies that if ALARM is true, the signal is in its 0-state.

When a *single logic convention* is used for all inputs and outputs (i.e. positive or negative logic), this defines the relationship between logic states and logic levels. Thus, if the positive logic convention is in force, true always corresponds to the logic H-level and, if the negative logic convention is in force, true corresponds to the logic L-level.

When the *logic polarity indicator* is used for each input and output, the signal name should preferably be followed by the logic level (between brackets) for which the statement represented by the signal name is true, e.g. ALARM(L) or ALARM(H).

11.2.1 General rules for signal name allocations

If space permits, easy to understand mnemonics should be used instead of short notations. For example, SELDEV1 rather than SD1 would better convey the meaning (SELECT DEVICE 1).

A signal name must be changed whenever the signal is gated with another, is delayed, chopped, stored, or changes its function in any way; see examples 4 and 7. On the contrary, no signal may change its name as a result of being inverted, amplified, or level shifted (see example 6 in Sub-clause 11.2.11).

Where possible, signals should be named by the function they perform instead of by the signals that generate them. Assume that a signal, PRUN, is gated with a second signal, TP6, to set a bistable element called RUN. If the output signal is called SETRUN, its function is obvious. However, if it is called PRUNTP6 its use is open to speculation (see example 1).

Other signals perform such varied functions that it is not feasible to label them according to their use. For example, the alternative instructions to READ or WRITE may control large blocks of logic. In this event it would be proper to name the signal RD/WR (READ or WRITE); see example 2.

Confusion sometimes occurs in assigning signal names when the true value causes one action and the false value causes a different action. For example, a bistable element may select device A when cleared and device B when set. In this event the signal name should not refer to either device A or B. It should be such as SELDEV with a note on the drawing to explain the selection of device A or B.

Signal names that embody an inherent negative, such as NORUN, sometimes require mental somersaults, and are therefore naturally difficult to understand. If possible, such signal names should be made inherently true; e.g. STOP or HALT can be substituted for NORUN.

11.2.2 *Recommended characters for signal names*

Signal names should be composed from standard character sets, excluding lower-case letters. Also, a single character space may be used where necessary although the use of the dot as a separator often proves advantageous over the space.

Design automation may place certain constraints on the use of characters and the length of signal names.

11.2.3 *Use of serial numbers*

If the same function is generated more than once, each occurrence should have the same signal name and be identified by a different serial number. For example, multiple negators or amplifiers driven by the same signal would have the same signal name, but different serial numbers. Thus, STOP-1 and STOP-2 may be the output signals of two negators which are both driven by the signal STOP (see examples 5, 6, 9 and 10).

11.2.4 *Language requirements*

There is no restriction as to the use of a language for the formation of signal names. The signal names used in this standard may therefore not necessarily be translated literally when using another language.

11.2.5 *Clock pulses*

The basic clock and all clocks derived therefrom may be designated by CP (Clock Pulse) and identified by the clock period. If the basic clock period is, for example, 25 ns, the mnemonic might be CP25N. Clocks derived from the basic clock might then be termed CP50N, CP100N, and so on.