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INTERNATIONAL STANDARD

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Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies

IEC 60194-2:2017-12(en)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARDS DESIGN, MANUFACTURE AND ASSEMBLY – VOCABULARY –

Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies

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International Standard IEC 60194-2 has been prepared by IEC technical committee 91: Electronics assembly technology.

This first edition, together with IEC 60194-1, will cancel and replace IEC 60194:2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to IEC 60194:2015:

a) exclusion of 32 general terms better served by other TCs;
b) exclusion of 47 terms no longer used by the electronics assembly industry;
c) inclusion of 13 new terms related with device embedded substrate technology;
d) removal of identification codes for terms as well as annexes.

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The text of this International Standard is based on the following documents:

CDV	Report on voting
91/1442/CDV	91/1473/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

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PRINTED BOARDS DESIGN, MANUFACTURE AND ASSEMBLY – VOCABULARY –

Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies

1 Scope

This part of IEC 60194 covers terms and definitions related to printed board and electronic assembly technologies as well as other electronic technologies.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of electronics assembly technology, the terms and definitions in 3.1 to 3.24 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1 A

3.1.1
abrasive trimming
adjustment of the value of a film component by notching it with a finely adjusted stream of an abrasive material against the resistor surface

3.1.2
accelerated ageing
accelerated life test
test in which the parameters such as voltage and temperature are increased above normal operating values to obtain observable or measurable deterioration in a relatively short period of time

3.1.3
accelerated test
test to check the life expectancy of an electronic component or electronic assembly in a short period of time by applying a physically severe condition(s) to the unit under test

3.1.4
acceleration factor
AF
ratio of stress in reliability testing to the normal operating condition

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3.1.5
acceptance inspection
<criterion> inspection that determines conformance of a product to design specifications as the basis for acceptance

3.1.6
acceptance quality level
AQL
number of defects (in %) within a population (lot) at which the lot has the chance to be accepted with an acceptance probability of about 90 % when testing a sample

3.1.7
acceptance tests
tests deemed necessary to determine the acceptability of a product as agreed to by both purchaser and vendor

3.1.8
accuracy
degree to which the result of a measurement or calculation agrees with the true value

3.1.9
active device
electronic component whose basic character changes while operating on an applied signal

Note 1 to entry: This includes diodes, transistors, thyristors, and integrated circuits that are used for the rectification, amplification, switching, etc., of analogue or digital circuits in either monolithic or hybrid form.

3.1.10
add-on component
discrete or integrated packaged or chip components that are attached to a film circuit in order to complete the circuit's function

3.1.11
adhesive
non-metallic materials that can join solids by surface bonding and internal strength (adhesion and cohesion)

Note 1 to entry: In surface mounting, an epoxy adhesive is used to adhere SMDs to the substrate.

[SOURCE: IEC 60050-212:2010, 212-15-44]

3.1.12
all metal package
hybrid circuit package made solely of metal, without glass or ceramic

3.1.13
allowable temperature
temperature range in which an electronic circuit or component can perform its intended functions

3.1.14
alphanumerical, adj
pertaining to data that contain the letters of an alphabet, the decimal digits, and may contain control characters, special characters and the space character

3.1.15
alpha particle
He^4 nucleus generated from a nuclear decay that is capable of generating hole-electron pairs in microelectronic devices and switching cells, causing soft errors in some devices

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3.1.16
alternating current
AC
electric current that is a periodic function of time with a zero direct component or, by extension, a negligible direct component

Note 1 to entry: For the qualifier AC, see IEC 60050-151.

[SOURCE: IEC 60050-131:2002, 131-11-24]

3.1.17
ambient
surrounding environment coming into contact with the system or component in question

3.1.18
amplitude
<voltage> maximum value of a voltage of an alternating voltage within one period

3.1.19
analogue circuit
electrical circuit that provides a continuous relationship between its input and output

3.1.20
anisotropy
condition for a substance having differing values for properties, such as permittivity, depending on the direction within the material

3.1.21
anode
electrode capable of emitting positive charge carriers to and/or receiving negative charge carriers from the medium of lower conductivity

Note 1 to entry: The direction of electric current is from the external circuit, through the anode, to the medium of lower conductivity.

Note 2 to entry: In some cases (e.g. electrochemical cells), the term "anode" is applied to one or another electrode, depending on the electric operating condition of the device. In other cases (e.g. electronic tubes and semiconductor devices), the term "anode" is assigned to a specific electrode.

[SOURCE: IEC 60050-151:2001, 151-13-02]

3.1.22
application-specific integrated circuit
ASIC
integrated circuit designed for specific applications

[SOURCE: IEC 60050-521:2002, 521-11-18]

3.1.23
area array package
package that has terminations arranged in a grid on the bottom of the package and contained within the package outline

3.1.24
assembly
assembled board
number of parts, subassemblies or combinations thereof joined together

Note 1 to entry: This term can be used in conjunction with other terms listed herein, for example, "printed board assembly".

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3.1.25
attenuation
decrease of the energy of an electromagnetic wave during its propagation, represented quantitatively by the ratio of the power flux densities at two specified points

Note 1 to entry: Attenuation is generally expressed in decibels.

[SOURCE: IEC 60050-705:1995, 705-02-05]

3.2 B

3.2.1
backfill
filling a hybrid circuit package with a dry inert gas prior to hermetic sealing

3.2.2
backplane
backpanel
interconnection device used to provide point-to-point electrical interconnections

Note 1 to entry: It is usually a printed board that has discrete wiring terminals on one side and connector receptacles on the other side.

3.2.3
backward crosstalk
near-end crosstalk
noise induced into an adjacent line, as seen at that end of the adjacent line which is closest to the signal source, when this line has been placed near an active line

Note 1 to entry: See also "forward crosstalk".

3.2.4
balanced transmission line
transmission line that has distributed inductance, capacitance, resistance, and conductance elements that are equally distributed between its conductors

3.2.5
ball
raised metal (or other conductive material) feature on a package substrate used to facilitate bonding to the next level of interconnect

3.2.6
ball grid array
BGA
surface-mount package wherein the bumps for terminations are formed in a grid on the bottom of a package

SEE: Figure 1.

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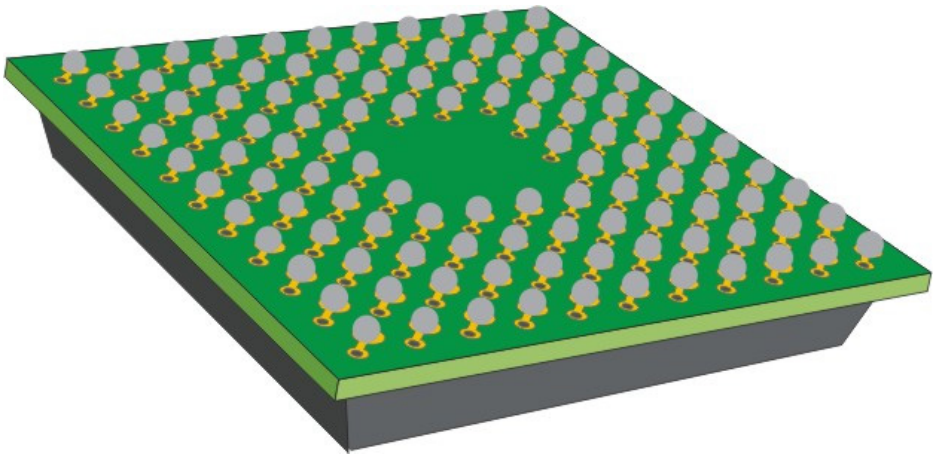

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Figure 1 – Ball grid array (BGA)

3.2.7
barcode
linear arrangement of bars and spaces in a predetermined pattern

3.2.8
barcode marking
identification code consisting of a pattern of vertical bars whose width and spacing identifies the item marked

3.2.9
barcode symbol
print of photographically reproduced barcode composed of parallel bars and spaces of various widths

Note 1 to entry: A barcode symbol contains a leading quiet zone, a start character, data characters, a stop character, and a trailing quiet zone; in some cases, a check character is included.

3.2.10
bare die
unpackaged discrete semiconductor or integrated circuit with pads on the upper surface suitable for interconnection to the substrate or package

3.2.11
base film
<flexible circuits> film that is the base material for the flexible printed wiring board and on the surface of which the conductive pattern can be formed

Note 1 to entry: When the heat resistance is required, polyimide film is mostly used, and polyester film is usually used when the heat resistance is not required.

3.2.12
base material
substrate
insulating material upon which a conductive pattern may be formed

Note 1 to entry: The base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.

3.2.13
base material thickness
thickness of the base material excluding conductive foil or material deposited on the surfaces

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3.2.14
base plane
plane that includes the lowest point of the mounting surface of the package, except for packages using stand-offs

3.2.15
basic specification
BS
document that describes the common elements for a set, family or group of products, materials, or services

3.2.16
bending resistance
ability of a material to withstand repeated bending to specified parameters without producing cracks and breaks in excess of the specification allowance

3.2.17
bias
<fabric> filling yarn that is off-square with the warp ends of a fabric

3.2.18
bipolar device
device in which both majority and minority carriers are present

Note 1 to entry: Bipolar and metal-oxide semiconductor (MOS) are the two most common device types.

3.2.19
bond
interconnection that performs a permanent electrical and/or mechanical function

3.2.20
bond pads
metallised areas on the die that are used for temporary or permanent electrical connection (bonding)

3.2.21
bond strength
pull strength
force perpendicular to a board's surface required to separate two adjacent layers of the board

Note 1 to entry: Bond strength is expressed as force per unit area.

3.2.22
bonding pad
<IC> area of metallization on an integrated circuit die that permits connection of fine wires or a circuit element to the die

3.2.23
bonding wire
gold or aluminium wire used for making electrical connections between lands, lead frames, and terminals

3.2.24
bow
warp
<fabric> filling yarn that lies in an arc across the width of a fabric

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3.2.25
break-down voltage
voltage at which the insulation between two conductors ruptures

3.2.26
bridging
<electrical> unintentional formation of a conductive path between conductors

3.2.27
bulk packaging
method for packaging loose parts, into a bag or case

3.2.28
bumped die
semiconductor die with raised metal features that facilitate inner-lead bonding

SEE: Figure 2.

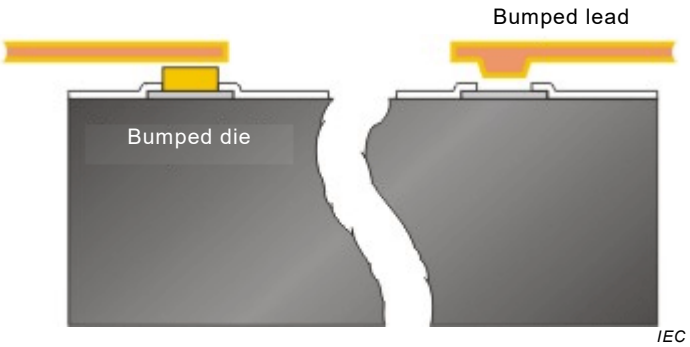

Figure 2 – Bumped die

3.2.29
burn-in
<test> process of electrically stressing a device at an elevated temperature, for a sufficient amount of time to cause the failure of marginal devices (infant mortality)

3.2.30
burn-in
<dynamic> burn-in at high temperatures that simulates the effects of actual or simulated operating conditions

3.2.31
burn-in
<static> burn-in at high temperatures with unvarying voltage, either forward or reverse bias

3.3 C

3.3.1
capacitance
measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them

[SOURCE: IEC 60050-131:2008, 131-12-13]

3.3.2
capacitive coupling
electrical interaction between two conductors that is caused by the capacitance between them

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3.3.3
ceramic dual in-line package
CERDIP
dual in-line package that has a package body of ceramic material and is hermetically sealed by a glass

Note 1 to entry: See also "dual in-line package".

3.3.4
ceramic pin grid array
ceramic PGA
pin grid array package (PGA) made of a ceramic material, hermetically sealed by metal, with leads formed on a grid extending from the bottom of the package

3.3.5
ceramic quad flat package
CQFP
quad flat package (QPF) made of a ceramic material, hermetically sealed by metal, with leads extending from all four sides

3.3.6
certification
verification that specified training or testing has been performed and that required proficiency or parameter values have been attained

3.3.7
characteristic impedance
quantity defined for a mode of propagation at a given frequency in a specific uniform transmission line or uniform waveguide by one of the three following relations:

$$Z_1 = S/|I|^2$$

$$Z_2 = |U|^2/S$$

$$Z_3 = U / I$$

where

Z is the complex characteristic impedance,

S is the complex power, and

U and I are the values, usually complex, respectively of a voltage and a current conventionally defined for each type of mode by analogy with transmission line equations.

EXAMPLE 1 For a parallel-wire transmission line, U and I can be uniquely defined and the three equations are consistent. If the transmission line is lossless, the characteristic impedance is real.

EXAMPLE 2 For a waveguide, the conventional definitions for U and I depend on the type of mode and generally lead to three different values of the characteristic impedance.

EXAMPLE 3 For a circular waveguide in the dominant mode TE11, U = RMS voltage along the diameter where the magnitude of the electric field strength vector is a maximum, I = the r.m.s. longitudinal current.

EXAMPLE 4 For a rectangular waveguide in the dominant mode TE10, U = the RMS voltage between midpoints of the two conductor faces normal to the electric field strength vector, I = the RMS longitudinal current following on one surface normal to the electric field strength vector.

[SOURCE: IEC 60050-726:1982, 726-07-01]

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3.3.8
chemical vapour deposition
process in which vapours and gases react chemically to produce deposits at the surface of a substrate

[SOURCE: IEC 60050-841:2004, 841-22-07]

3.3.9
chip

SEE: "die".

Note 1 to entry: Common parlance for die.

3.3.10
chip carrier
low-profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package

Note 1 to entry: It can be leaded or leadless.

3.3.11
chip-on-board
COB
printed board assembly technology that places unpackaged semiconductor dice and interconnects them by wire bonding or similar attachment techniques

SEE: Figure 3.

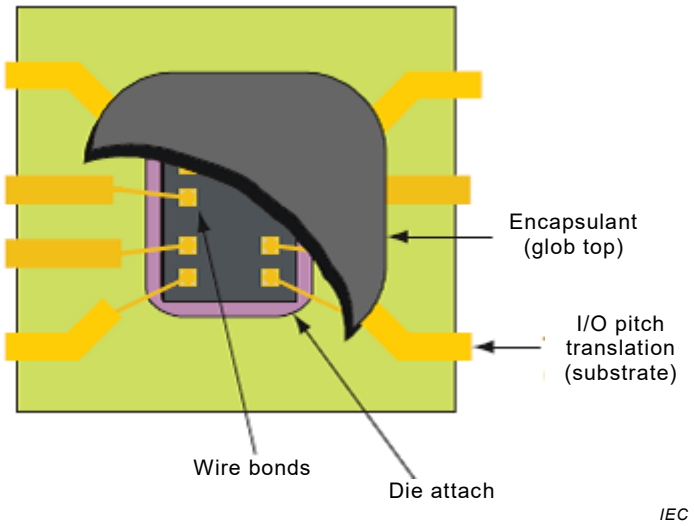

Figure 3 – Chip on board (COB)

Note 1 to entry: The silicon area density is usually smaller than the density of the printed board.

Note 2 to entry: A mounting and attachment technique where the die is mounted onto a substrate, often a printed-circuit board.

3.3.12
chip-on-flex
COF
semiconductor chip mounted directly onto a flexible printed board

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