

INTERNATIONAL STANDARD

NORME INTERNATIONALE



**Discrete semiconductor devices –
Part 15: Isolated power semiconductor devices**

**Dispositifs discrets à semiconducteurs –
Partie 15: Dispositifs de puissance à semiconducteurs isolés**

Withdawn



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DISCRETE SEMICONDUCTOR DEVICES –

Part 15: Isolated power semiconductor devices

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International Standard IEC 60747-15 has been prepared by subcommittee 47E, Discrete semiconductor devices of IEC technical committee 47: Semiconductor devices.

This bilingual version (2013-05) corresponds to the monolingual English version, published in 2003-06.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/236/FDIS	47E/238/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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DISCRETE SEMICONDUCTOR DEVICES –

Part 15: Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the product specific standards, requirements and test methods for isolated power semiconductor devices. These requirements are added to those given in other parts of IEC 60747, IEC 60748 and IEC 60749 for the corresponding non-isolated power devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-6, *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-7, *Environmental testing – Part 2-7: Tests – Test Ga and guidance: Acceleration, steady state*

IEC 60068-2-14, *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*

IEC 60068-2-20, *Environmental testing – Part 2-20: Tests – Test T: Soldering*

IEC 60068-2-27, *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock*

IEC 60068-2-47, *Environmental testing – Part 2-47: Test methods – Mounting of components, equipment and other articles for vibration, impact and other similar dynamic tests*

IEC 60068-2-48, *Environmental testing – Part 2-48: Test methods – Guidance on the application of the tests of IEC 60068 to simulate the effects of storage*

IEC 60068-3-4, *Environmental testing – Part 3-4: Supporting documentation and guidance – Damp heat tests*

IEC 60191-4:1999, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*

IEC 60270:2000, *High voltage test techniques – Partial discharge measurements*

IEC 60319, *Presentation and specification of reliability data for electronic components*

IEC 60664-1:1992, *Insulation coordination for equipment within low-voltage systems – Principles, requirements and tests*

IEC 60721-3-3:1994, *Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather-protected locations*

IEC 60747-1:1983, *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*
Amendment 1 (1991)
Amendment 3 (1996)

IEC 60747-2:2000, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6:2000, *Semiconductor devices – Part 6: Thyristors*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60747-8:2000, *Semiconductor devices – Part 8: Field effect transistors*

IEC 60747-9:1998, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 60749-5: *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6: *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-10: *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock*

IEC 60749-12: *Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency*

IEC 60749-14: *Semiconductor devices – Mechanical and climatic test methods – Part 14: Robustness of terminations (lead integrity)¹*

IEC 60749-15: *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices¹*

IEC 60749-21: *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability¹*

IEC 60749-25: *Semiconductor devices – Mechanical and climatic test methods – Part 25: Rapid change of temperature (air, air)¹*

IEC 60749-26: *Semiconductor devices – Mechanical and climatic test methods – Part 26: Rapid change of temperature (air, air)¹*

IEC 60749-36: *Semiconductor devices – Mechanical and climatic test methods – Part 36: Acceleration, steady-state*

IEC 61287-1:1995, *Power convertors installed on board rolling stock – Part 1: Characteristics and test methods²*

ISO 1302:2002, *Geometrical Product Specifications (GPS) – Indication of surface texture in technical product documentation*

ISO 2768-2:1989, *General tolerances – Part 2: Geometrical tolerances for features without individual tolerance indications*

¹ In preparation.

² A new edition is being prepared.

3 Terms and definitions

For the purposes of this part of IEC 60747, the following definitions apply.

3.1

isolated power semiconductor device

semiconductor device that contains an integral electrical insulator between cooling surface or base plate (envelope) and any isolated circuit elements

NOTE 1 Included are solid-state relays (SSRs) incorporating opto-isolated driving units (see IEC 60747-5-1, IEC 60745-5-2 and IEC 60745-5-3), monolithically integrated ICs with power stages and isolated cooling surface, i.e. intelligent power devices and isolated discrete plastic encapsulated packages that have an isolated cooling surface.

NOTE 2 The surface of the package transferring the heat to a heat sink or ambient is referred to as "base plate". The surface of the package not transferring the heat is referred to as "envelope".

3.2

constituent parts of the isolated power semiconductor device

3.2.1

circuit element

any constituent part of a circuit that contributes directly to its operation and performs a definable function

NOTE Examples include rectifier diodes, thyristors, bipolar transistors, MOSFETs, IGBTs affixed on metallized isolator substrates and integrated driver and protection circuits.

3.2.2

interconnection

internal connection between circuit elements and between circuit elements and terminals (see subclause 3.7.2 of IEC 60747-1)

NOTE They are considered to be parts of their associated circuit elements.

3.2.3

base plate

metallic or metallized cooling surface part of the package that transfers the heat from inside to a heat sink outside

3.2.4

terminals

externally available points of connection, isolated from base plate

3.2.4.1

main terminals

terminals having the high potential of the power circuit and carrying the main current

3.2.4.2

control terminals

terminals having only low current capability for the purpose of control function to which the external control signals are applied or from which sensing parameters are taken

3.2.4.3

high-voltage control terminals

terminals having the high potential of the power circuit, but carrying only low current for control function

NOTE Examples include current shunts and collector sense terminals having the high potential of the main terminals.

3.2.4.4

low-voltage control terminals

terminals at a low potential against base plate having a control function, and isolated from the “main terminals” as well as from high voltage control terminals

NOTE Examples include the terminals of isolated temperature sensors and isolated gate driver inputs, etc.

3.3

classification of categories of isolated power devices

isolated power semiconductor devices are classified as follows:

3.3.1

chip content: types according to their main functional circuit elements

3.3.1.1

thyristor module

isolated power semiconductor device containing thyristor chips

3.3.1.2

diode module

isolated power semiconductor device containing diode chips

3.3.1.3

bipolar transistor module

isolated power semiconductor device containing bipolar transistor chips and their inverse diode chips

3.3.1.4

IGBT module

isolated power semiconductor device containing isolated gate bipolar transistor (IGBT) chips and their inverse diode chips

3.3.1.5

MOSFET module

isolated power semiconductor device containing MOSFET chips

3.3.2

circuit configuration: types according to their main functional circuit

3.3.2.1

single switch

one functional circuit element, the “semiconductor switch”, in one case (as the most simple functional device) (see Annex D, Figure D.2a)

NOTE 1 Examples include epoxy isolated discrete semiconductors with metallic cooling surface.

NOTE 2 “Switch” is here a commonly used synonym for “functional circuit elements”.

3.3.2.2

dual switch

two switches in one case, series connected, forming a “half bridge” circuit, a phase leg of a single-phase bridge or three-phase bridge circuit arrangement (see Annex D, Figure D.2b)

NOTE Examples include “brake chopper” circuit with a high side switch or a low side switch and the freewheeling diode on the other position, see Annex D, Figure D.2c and D.2d.

3.3.2.3

H – bridge

four switches in one case, two half bridges forming a “full bridge”, a single-phase bridge (see Annex D, Figure D.2e)

3.3.2.4

sixpack

six switches in one case, three half bridges forming a “three-phase bridge” (see Annex D, Figure D.2f)

3.3.2.5

sevenpack

seven switches in one case, three half bridges forming a three-phase bridge circuit and in addition a brake chopper circuit (see Annex D, Figures D.2g and D.2h)

NOTE Above circuit configurations are mainly used for transistor inverter circuits producing a.c. output of fixed or variable frequency from d.c. input voltage, using pulse width modulation (PWM), see Annex D, Figure D.2i (CIB-converter-inverter-brake chopper devices).

3.3.2.6

bridge rectifier

single-phase bridge converter circuit of 4 diodes in one case (see Annex D, Figure D.1: circuit B2U, two pulse bridge uncontrolled)

3.3.2.7

half controlled bridge rectifier

single-phase bridge converter circuit of 2 diodes and 2 thyristors in one case (see Annex D, Figure D.1: B2HK)

3.3.2.8

fully controlled bridge rectifier

single-phase bridge converter circuit of 4 thyristors in one case (see Annex D, Figure D.1: B2C, two pulse bridge controlled)

3.3.2.9

three phase bridge rectifier

three-phase bridge converter circuit of 6 diodes in one case (see Annex D, Figure D.1: B6U, six pulse bridge uncontrolled)

3.3.2.10

half controlled three phase bridge rectifier

three-phase bridge converter circuit of 3 diodes and 3 thyristors in one case (see Annex D, Figure D.1: B6HK)

3.3.2.11

fully controlled three phase rectifier

three-phase bridge converter circuit of 6 thyristors in one case (see Annex D, Figure D.1: B6C, six pulse bridge controlled)

3.3.2.12

a.c. controller

single-phase (or three-phase) proportional controller of two (or six) inverse-parallel connected thyristors producing a proportional a.c. output voltage from a.c. input voltage using phase angle control (see Annex D, Figure D.1: W1C or W3C)

NOTE 1 Above rectifier (or respectively controller) circuits are mainly used as input converters producing a fixed or – if thyristor controlled – proportional d.c. (or respectively a.c.) output voltage from a.c. input voltage, using phase-angle control. (See also JESD 14.)

NOTE 2 IEC 60971 provides details. Examples include circuits designated “B2U”,..... “B6C”,..... “W1C”, “W3C”.

3.3.3

other circuit configurations and combinations

for other circuit configurations and combinations for the above circuits, see Annex D

3.4**functionality: types according to additional functions**

such as for measurement, protection and control, including SSRs:

circuits as in 3.2.3, but with enhanced functionality by:

- current shunts or sensors
- temperature sensors
- overcurrent or overvoltage protection
- driver with or without integrated power supply
- further control circuitry
- opto-coupler and auxiliary circuits
- other functions

NOTE Such devices are called intelligent power modules (IPM) on the market. IPM and SMART power devices are specific names of such specific products.

3.5**solid-state relays****SSRs**

isolated power semiconductor devices that incorporate an opto-isolated electronic driving unit using an input section, fully isolated from the power output side and the metallic or metallized isolated cooling surface or base plate, performing a switch-on/switch-off function as an electronic relay producing a non-proportional output

NOTE For SSRs, IEC 60747-5-1, IEC 60747-5-2 and IEC 60747-5-3 also apply.

3.6**isolation voltage**

V_{isol}

isolation breakdown withstand voltage between terminals and base plate (or external heat sink) over a specified time

NOTE Subclause 1.3.9.1 of IEC 60664-1 defines 'rated insulation voltage' as r.m.s. withstand voltage value assigned by the manufacturer to the equipment or to a part of it, characterizing the specified isolation voltage withstand capability of its insulation.

3.7**partial discharge inception voltage**

V_i

voltage between main terminals and base plate at which partial discharges occur when the applied voltage is gradually increased from a lower value

NOTE 1 IEC 60270 defines inception voltage as greater than the extinction voltage.

NOTE 2 Subclause 1.3.18.4 of IEC 60664-1 defines 'partial discharge inception voltage', U_i , as the lowest peak value of the test voltage at which the apparent charge becomes greater than the specified discharge magnitude when the test voltage is increased above a low value for which no discharge occurs.

3.8**partial discharge extinction voltage**

V_e

voltage between main terminals and base plate at which partial discharges disappear when the applied voltage is gradually decreased from a higher value

NOTE 1 IEC 60270 defines the extinction voltage as lower than the inception voltage.

NOTE 2 Subclause 1.3.18.5 of IEC 60664-1 defines 'partial discharge extinction voltage', U_e , as the lowest peak value of the test voltage at which the apparent charge becomes less than the specified discharge magnitude when the test voltage is reduced below a high level where such discharges have occurred.

3.9 creepage distance along surface

d_s

shortest distance along the surface of the insulating material between two conductive parts at different potentials

NOTE See subclause 1.3.3 of IEC 60664-1 (IEV 151-15-50).

3.10 clearance distance in air

d_a

shortest distance in air between two conductive parts at different potentials

NOTE See 1.3.2 of IEC 60664-1.

3.11 peak case non-rupture current

peak current that will not lead to a rupture of the package, ejecting plasma and massive particles under specified conditions

NOTE The value indicated depends on the type of the device, e.g. thyristor, diode, IGBT, and the packaging technology, e.g. whether wire bonded.

3.11.1 peak case non-rupture current for diodes and thyristors

I_{RSMC}

peak reverse current of a half sine wave, when the device has lost its reverse blocking capability, that should not be exceeded in order to avoid bursting of the case or emission of a plasma beam or massive particles under specified conditions

NOTE Specified in IEC 60747-2 for diode devices, respectively IEC 60747-6 for thyristor devices.

3.11.2 peak case non-rupture current for bipolar transistors, IGBT and MOSFETs

I_{CNR}

peak collector current that should not be exceeded in order to avoid bursting of the case or emission of a plasma beam or ejection of massive particles under specified conditions

3.12 parasitic stray inductance between main terminals

L_P

inner wiring stray inductance, effective in the main current path between the main terminals

NOTE 1 L_P of a half-bridge module (dual switch) is the effective parasitic stray inductance L_{CE} between the power terminal (+) (top collector) and power terminal (–) (bottom emitter).

NOTE 2 Parasitic stray inductance L_P will cause a voltage spike at switch-off (above the continuous d.c. voltage V_{CC}) on chip level, higher than the voltage, measured between the terminals.

3.13 parasitic stray capacitance between switching circuit elements and case

C_P

coupling capacitance between all terminals connected together and the base plate (or heat-sink surface)

NOTE This capacitance can serve as a bypass for parasitic high frequency currents that can cause electro-magnetic interference (EMI).

3.14 power cycling (load) capability

$N_{f,p}$

number of power cycles $N_{f,p}$ until failure of the cumulative percentage p (=percentile) of a device population

NOTE Subclause 7.4.6 of IEC 60747-2 (diodes) and 9.4.6 of IEC 60747-6 (thyristors) define “power cycling load test”. Subclause 10.1.3.3 of Amendment 1 to IEC 60747-9 (IGBT) defines “intermittent operating life tests”.

4 Letter symbols

4.1 General

IEC 60747-1 applies.

4.2 Additional subscripts/symbols

p = parasitic

ref = reference point (for measuring temperatures)

s = heat sink (subscript of heat-sink temperature T_s)

t = time (parameter) used for currents, voltages as function of time: in brackets: (t)

t = terminal (subscript of mounting torque to terminal M_t)

1 = primary side (of a transformer or control input)

2 = secondary side (power output side)

4.3 List letter symbols

4.3.1 Voltages and currents (see also IEC 60747-1)

Terminal current

I_{tRMS}

Isolation voltage

V_{isol}

Partial discharge inception voltage

V_i

Partial discharge extinction voltage

V_e

Isolation leakage current

I_{isol}

Peak case non-rupture current (for diode and thyristor devices)

I_{RSMC}

Peak case non-rupture current (for IGBT and MOSFET devices)

I_{CNR}

4.3.2 Mechanical terms

Mounting torque for screws to heat sink

M_s

see Note 1

Mounting torque for terminal screws

M_t

see Note 1

Mounting force for pressure mounted devices

F

Maximum acceleration in all 3 axis (x, y, z)

a

Mass

m

Flatness of the case (base-plate, cooling surface)

e_c

see Note 2

Flatness of the cooling surface (heat sink)

e_s

Roughness of the case (base plate)

R_{Zc}

see Note 3

Roughness of the cooling surface (heat sink)

R_{Zs}

see Note 3

Thickness of thermal compound grease (case – sink)

$D_{(c-s)}$

see Annex B

NOTE 1 Under given mounting instructions. In respect of thermal compound properties see mounting instructions.

NOTE 2 See for instance IEC 60191-2:1995, outline 191-IEC-080B (34 mm wide module) and 191-IEC-081B (62 mm wide module) deviation from flatness 100 µm – see Note 4.

NOTE 3 In USA: “ R_a ” is used instead, (R_z = about 3* R_a). There is no fixed factor between the two.

NOTE 4 Example: Seating plane. Deviation from flatness shall be $<20\text{ }\mu\text{m}$ concave and $<100\text{ }\mu\text{m}$ convex, the roughness $<10\text{ }\mu\text{m}$. Flatness and roughness are to be specified as, for instance, defined in the related publication IEC 60191-2.

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4.3.3 Other terms

Total max. power dissipation per functional circuit element at $T_c = 25\text{ °C}$	P_{tot}
Parasitic inductance, effective between terminals x and y or between terminals and chips (to be specified)	L_{Pxy}
Parasitic capacitance between all terminals connected together and cooling surface (case, base plate, ground)	C_P
Ohmic lead resistance between terminal x and related functional circuit element x'	$R_{\text{xx'}}$
Terminal temperature	T_t
Sensor temperature	T_{sen}
Significant temperature of the temperature sensor No.1 (to be specified)	T_{sen1}
Significant case temperature at the reference point (to be specified)	T_{cref}
Number of power load cycles until failure of a percentage p of a population of devices	$N_{\text{f,p}}$

5 Essential ratings (limiting values) and characteristics

5.1 General

Isolated power semiconductor devices should be specified as case rated or heat-sink rated devices.

NOTE Actual values regarding isolation voltage, partial discharge voltage, creepage and clearance distance are not described in this standard. The values shall be based on each standard, which will be applied to any equipment using the isolated power semiconductor devices.

5.1.1 Temperatures

The ratings and characteristics should be quoted at a temperature of 25 °C or another specified elevated temperature chosen from Amendment 3 (1996) to IEC 60747-1.

NOTE $T_{\text{stg}} = -40\text{ °C}$ is specified in IEC 60749-25.

5.1.2 Climatic characteristics

Limiting values of environmental parameters for the final application are as follows:

- ambient temperature;
- humidity;
- speed and pressure of air;
- irradiation by sun and other heat sources;
- mechanical active substances;
- chemically active substances;
- biological issues.

These shall be described by class, as specified in Table 1 and Annex C of IEC 60721-3-3.

5.2 Ratings (limiting values)

Unless otherwise stated, all limiting ratings apply at a temperature of 25 °C or another elevated temperature specified from the list in IEC 60747-1. The following ratings shall be valid for the whole range of operating conditions as stated for the particular device.

5.2.1 Isolation voltage, V_{iso}

Maximum r.m.s. or d.c. value between the isolated terminals and the base plate, applied between the high potential terminals, all connected with each other, and the ground potential of the base plate (or heat sink underneath) for a specified time at the final test procedure of the device and of the final equipment to assure the capability to isolate the electrical system from ground potential.

NOTE 1 Details for the dielectric isolation voltage test for solid insulation shall be secured following 2.2.2.2, 4.1.2, 4.1.2.1 and 4.1.2.3.1 of IEC 60664-1 (for low voltage equipment), respectively IEC 61287 (for rolling stock) depending on the overvoltage category (application), the applied maximum working voltage, etc.

NOTE 2 Specified values are under discussion. The future IEC 62103 (=EN 50178) proposes reduced isolation voltages in comparison to before.

5.2.2 Peak case non-rupture current (where appropriate)

Maximum surge current that does not cause the bursting of the case or emission of plasma and particles.

5.2.2.1 Peak case non-rupture current (I_{RSMC}) of isolated diode and thyristor modules

Maximum peak reverse current of a half sine wave (e.g. 10 ms), when the device has lost its reverse blocking capability, that should not be exceeded in order to avoid bursting of the case or emission of a plasma beam or massive particles.

NOTE Specified in IEC 60747-2 for diode devices and in IEC 60747-6 for thyristors devices.

5.2.2.2 Peak case non-rupture current (I_{CNR}) of bipolar transistors, IGBTs and MOSFETs modules

Maximum peak collector current during a short-circuit that should not be exceeded in order to avoid bursting of the case or emission of a plasma beam or ejection of massive particles under specified conditions, i.e. of specified duration $t_{\text{p(SC)}}$ and wave shape, at a driving d.c. voltage V_{CC} (e.g. two-thirds V_{CES}), driving conditions and a maximum stored energy E_{C} of the feeding d.c. line capacitor, C , and specified short-circuit inductance L_{SC} (see Note 4 below and Annex A).

NOTE 1 If an isolated device suffers a short-circuit, then most of the energy stored in the system is discharged into the device. The prime source of such energy is the DC line capacitor. Due to the very low parasitic inductance (between 5 nH and 100 nH) in the circuit with isolated IGBT devices, the characteristic time for the discharge of energy is only 30 μs to 100 μs . Other parts of the system may have larger stored energies (e.g. transformers, motors, etc.), but their characteristic time for discharge is considerably longer.

NOTE 2 For wire bonded isolated IGBT devices, the minimum limit for material ejection (explosion of the device) is at a stored capacitive energy of about 10 kJ. Therefore it is necessary in some applications to verify the reliability of the isolated device in a test and measurement procedure.

NOTE 3 Still to be specified for IGBTs in IEC 60747-9.

NOTE 4 $L_{\text{SC}} = L_{\text{LSC}} + L_{\text{CSC}} + L_{\text{P}}$

where

L_{SC} is the inductance of the complete short-circuit between plus and minus;

L_{LSC} is the inductance of the load short-circuited;

L_{CSC} is the parasitic inductance of the capacitor bank;

L_{P} is the internal parasitic (stray) inductance of the module between collector and emitter terminal respectively between plus and minus bus bar.

5.2.3 Maximum terminal current (I_{tRMS}) (where appropriate)

Maximum r.m.s. value of the current through the main terminal under specified conditions as minimum mounting torque, M_t and maximum allowed terminal temperature ($T_{tmax} = T_{stg}$ or $T_{tmax} = < T_{vjmax}$).

NOTE 1 Examples include the common terminal of devices containing multiple isolated functional circuit elements, all feeding into one terminal, i.e. of a sixpack etc.

NOTE 2 It should not be necessary to derate this current with junction temperature, as dissipation caused in the terminal is not in the semiconductor junction and should be removed over the connections.

5.2.4 Total power dissipation (P_{tot})

Maximum value per functional circuit element at $T_c = 25\text{ °C}$ (or $T_s = 25\text{ °C}$), when $T_{vj} = T_{vjmax}$, at d.c. load, not regarding any power dissipation caused by switching and any lead resistances of internal connections.

$$P_{tot} = V \cdot I - (R_{cc'} + R_{ee'}) I^2 \quad (1)$$

where

V is the measured forward voltage between the related main terminals;

I is the maximum allowable average current;

$(R_{cc'} + R_{ee'})$ is the lead resistance to terminals.

$$P_{tot} = (T_{vjmax} - T_c) / R_{th(j-c)} \quad (2)$$

for case rated devices, respectively

$$P_{tot} = (T_{vjmax} - T_s) / R_{th(j-s)} \quad (3)$$

for heat sink rated devices.

5.2.5 Minimum and maximum temperatures of isolated devices (T_{stg} , T_c , T_{vj} , T_{sold})

Maximum allowed solder temperature T_{sold} during solder process over a specified solder processing time t_{sold} . For other temperatures see Amendment 3 to IEC 60747-1.

NOTE This is essential for solderable terminals for printed circuit board (PCB) mounting, important especially for lead-free soldering, see also IEC 60068-2-58.

5.2.6 Mechanically limiting ratings

Allowed limiting values that do not cause any mechanical damage or failure but secure mechanical function over the life time of the device and are necessary to meet the data sheet values:

- minimum and maximum mounting torque M_s for screws (to be specified) to heat sink (see Note 1);
- minimum and maximum mounting torque M_t for terminal screws (to be specified) (see Note 1);
- minimum and maximum mounting force F for pressure mounted devices (see Note 1);
- maximum pulling force F_t for terminals (robustness) (see IEC 60749-14);
- maximum acceleration, a , in all three axes (x, y, z) (see IEC 60749-36, IEC 60068-2-7 and IEC 60068-2-47);
- flatness e_c of the case (base plate) (see Note 2 and IEC 60191-2);
- roughness R_{zc} of the case (base plate) (see Note 3 and IEC 60191-2);

- flatness e_s of the heat sink surface necessary (see manufacturer's mounting instructions).

NOTE 1 Under given mounting instructions. For thermal compound properties, see mounting instructions and Annex B.

NOTE 2 For example IEC 60191-2:1995, outline 191-IEC-108 B (34 mm wide transistor module) and 191-IEC-108 B (62 mm wide transistor module) describe maximum deviation from flatness to be 100 μm (see Note 4).

NOTE 3 In the USA: " R_a " is used instead, (R_z = about $3 \cdot R_a$). There is no fix factor between those two.

NOTE 4 For example, the seating plane deviation from flatness shall be $<20 \mu\text{m}$ (concave) and $<100 \mu\text{m}$ (convex), the roughness $R_{zc} < 10 \mu\text{m}$. If thermal compound is used, $R_{zc} < 64 \mu\text{m}$ may also be suitable (see manufacturer's instructions). Flatness and roughness are defined in the related publication IEC 60191-2. If the case outline is IEC standardized, see Annex B.

5.2.6.1 Minimum mounting torque of screws to heat sink (M_s)

Minimum mounting torque that shall be applied to the fixing screws to the heat sink that is necessary to guarantee the data sheet values of thermal resistance, using the mounting instructions of the manufacturer.

5.2.6.2 Minimum mounting torque of screws to terminals (M_t)

Minimum mounting torque that shall be applied to screwed main terminals that is necessary to guarantee the data sheet values of their current carrying capability, based on mounting instructions.

5.2.6.3 Minimum mounting force (F)

Minimum mounting force for pressure-mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device that is necessary to guarantee the data sheet values of thermal resistance and current-carrying capability.

NOTE Such devices include isolated discrete devices with a metallic cooling surface (with outlines as for IEC 60191-2 / 191IEC I-73a – known also as case outline JEDEC TO-220 or similar case outlines).

5.2.6.4 Maximum allowed terminal pull-out force (F_t)

Maximum allowed value of the force that is not enough to pull the terminal out of its position and that does not damage the case of the device, respectively the proper electrical contact.

NOTE 1 Pulling leads and/or mechanical vibrations should be avoided.

NOTE 2 In some cases, no pulling force on terminals are acceptable at all: $F_t = 0$.

5.3 Characteristics

5.3.1 Distances

5.3.1.1 Creepage distance along surface (d_s)

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate.

NOTE 1 IEC 60112 and 2.7 and 3.2 of IEC 60664-1, together with Figure D.1 apply.

NOTE 2 Subclause 4.2 of IEC 60664-1 shows typical examples of various shapes of creepage distances, while 2.5 shows pollution degrees and Table 2 shows minimum clearances.

NOTE 3 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance considerably (for details see the examples in IEC 60664-1). This is essential, if dust, moisture or dirt starts to cover the surface and increases the leakage current over the surface, which might start burning the plastic encapsulation material.

5.3.1.2 Clearance distance in air (d_a)

Minimum value of distance through air between terminals of different potential of the isolated device and of the base plate.

NOTE For details see 2.5 of IEC 60664-1 (pollution degree), as well as 3.1, Tables 1 and 2. See also 4.2 of IEC 60664-1 showing typical examples of various shapes of clearance distances.

5.3.2 Parasitic stray inductance (L_p)

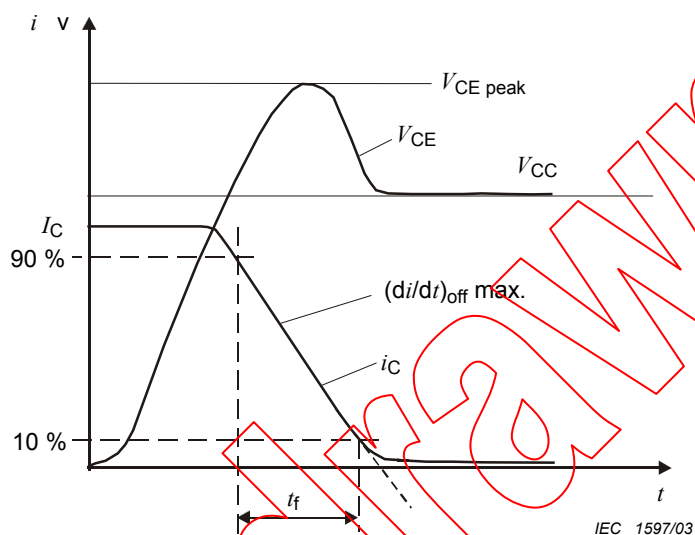
Maximum or typical value of the inner wiring stray inductance of the circuit element, effective in the main current path between the main terminals.

NOTE 1 The voltage spike at switch-off can be higher than the continuous d.c. voltage V_{CC} on chip level, and higher than the voltage measured between the terminals.

Withdrawn

NOTE 2 The value of the parasitic inner wiring inductances L_P shall be indicated as follows:

- for single switches between the main terminals in the main current path, for example L_{CE} between collector and emitter terminal of an IGBT single switch;
- for dual switches, half bridge phase legs, sixpacks, choppers, etc. between the main terminals in the main current path to be connected to the d.c. link, e.g. L_{CE} between collector C1 of the upper IGBT, to be connected to plus of a d.c. link, and emitter E2 of the lower IGBT, to be connected to minus of the d.c. link;
- for others: between the main terminal x and the related chip x' (to be specified):



$$(di/dt)_{off} = \max di/dt \text{ (read on oscilloscope) } = \text{about } 0,8 \cdot I_C / t_f \quad (4)$$

$$V_{CEpeak} - V_{CC} = -L_P \cdot (di/dt)_{off} \quad (5)$$

Figure 1a – Parasitic inductance L_P creates an overvoltage spike at a $(di/dt)_{off}$ at chip level

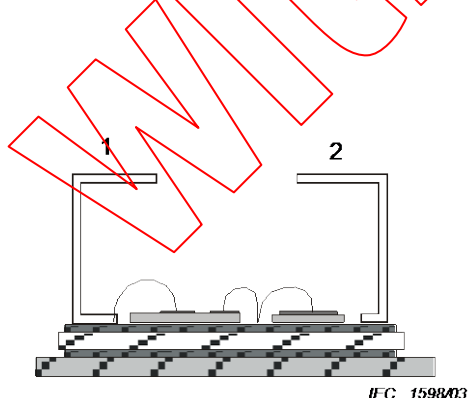


Figure 1b – Basic mechanical arrangement inside

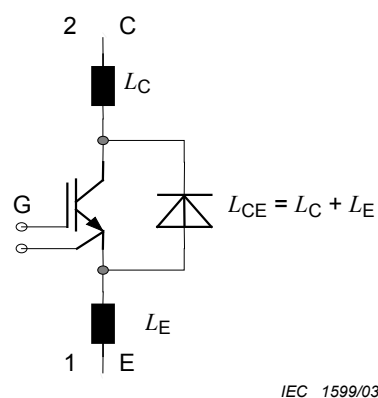


Figure 1c – Parasitic inductances inside a single switch

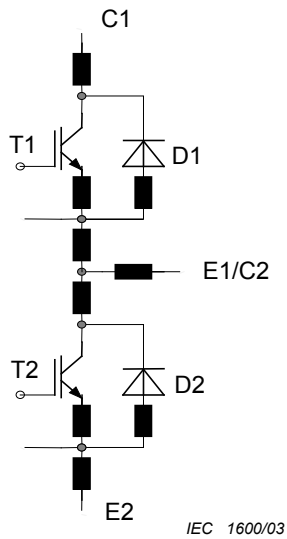


Figure 1d – Parasitic inductance network (L_p) inside a dual switch device

Figure 1 – Explanation of parasitic inductance L_p

For a definition of parasitic stray inductance L_p of inner wiring between the power terminals of the device and the circuit elements, see 3.12 above. Where appropriate, an equivalent circuit diagram of all the parasitic elements should be given, which is especially useful for simulations. See Figure 2, as follows here below.

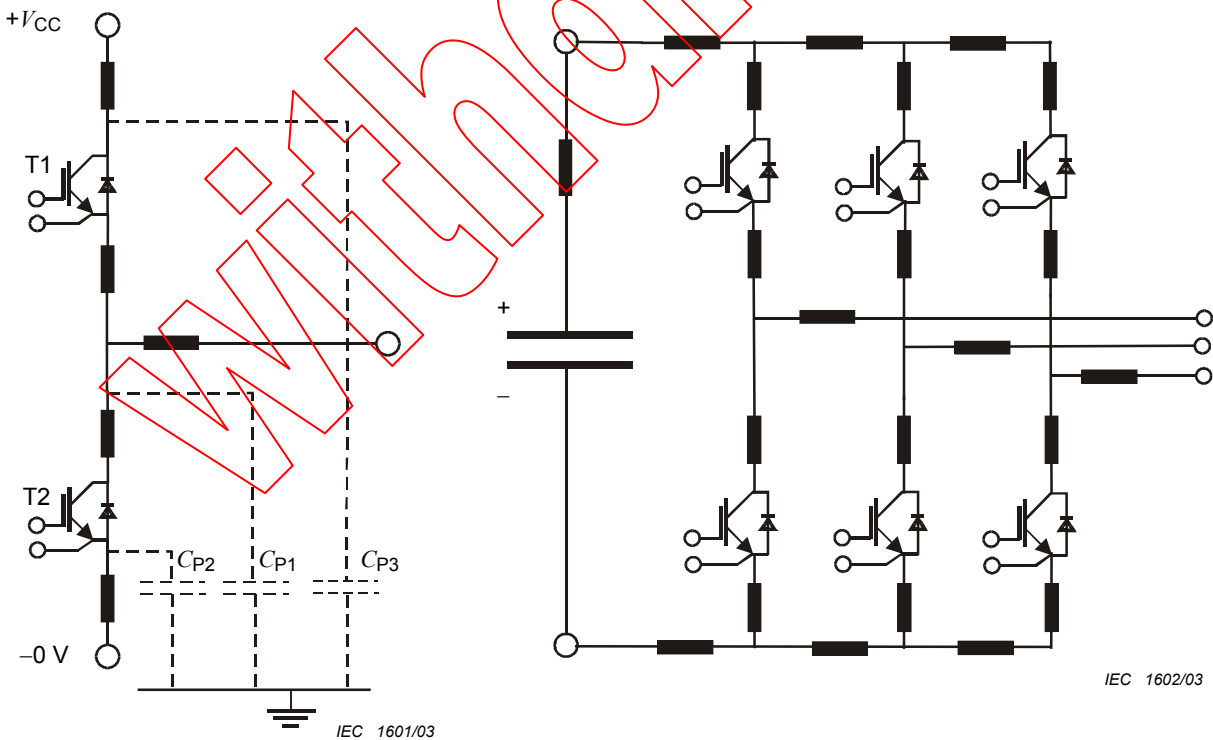


Figure 2a – L_p and parasitic stray capacitances C_p of a dual IGBT module

Figure 2b – L_p of a three-phase inverter bridge IGBT module

Figure 2 – Examples for distributed parasitic stray inductances L_p

5.3.3 Parasitic stray capacitance between switching circuit elements and case (C_p)

Maximum value of parasitic stray capacitance of the metal parts on the isolating layer between all terminals, connected to each other, and the cooling surface, i.e. base plate of the case, connected to ground.

5.3.4 Partial discharge inception voltage (V_{iM} or $V_{i(RMS)}$) (where appropriate)

Minimum peak value V_{iM} or r.m.s. value $V_{i(RMS)}$ between the isolated terminals and the base plate, at which such discharges are observed (for details see IEC 60270).

NOTE In practice, for tests on component level, the inception voltage V_i is the lowest voltage at which the partial discharge magnitude exceeds a charge of 10 pC.

5.3.5 Partial discharge extinction voltage (V_{eM} or $V_{e(RMS)}$) (where appropriate)

Minimum peak value V_{eM} or r.m.s. value $V_{e(RMS)}$ value between the isolated terminals and the base plate, at which such discharges are observed (for measurement details see IEC 60270).

NOTE In practice, for tests on component level, the extinction voltage V_e is the lowest voltage at which the partial discharge magnitude becomes less than 10 pC.

5.3.6 Thermal resistances ($R_{th(....)}$; $R_{th(j-c)}$; $R_{th(c-s)}$; $R_{th(j-s)}$; $R_{th(j-a)}$)

Maximum or typical value of thermal resistance $R_{th(j-c)}$ between the junction (j) and case (c) (= base plate) etc. using a specified external reference point $T_{c\text{ ref}}$ on the base plate.

NOTE 1 The basic document for $R_{th(....)}$ is IEC 60747-1.

NOTE 2 $R_{th(j-c)}$ should be indicated to determine the virtual junction temperature of each chip depending on the reference point temperature and the power dissipation in the chip.

The thermal resistance

$R_{th(j-c)}$ is the value between junction and case (base plate with reference point temperature $T_{c\text{ ref}}$),

$R_{th(c-s)}$ is the value between case and heat sink (reference point temperature $T_{s\text{ ref}}$),

$R_{th(j-s)}$ is the value between junction and heat sink (for heat sink rated devices),

$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-s)} + R_{th(s-a)}$ is the sum between junction and ambient temperature T_a .

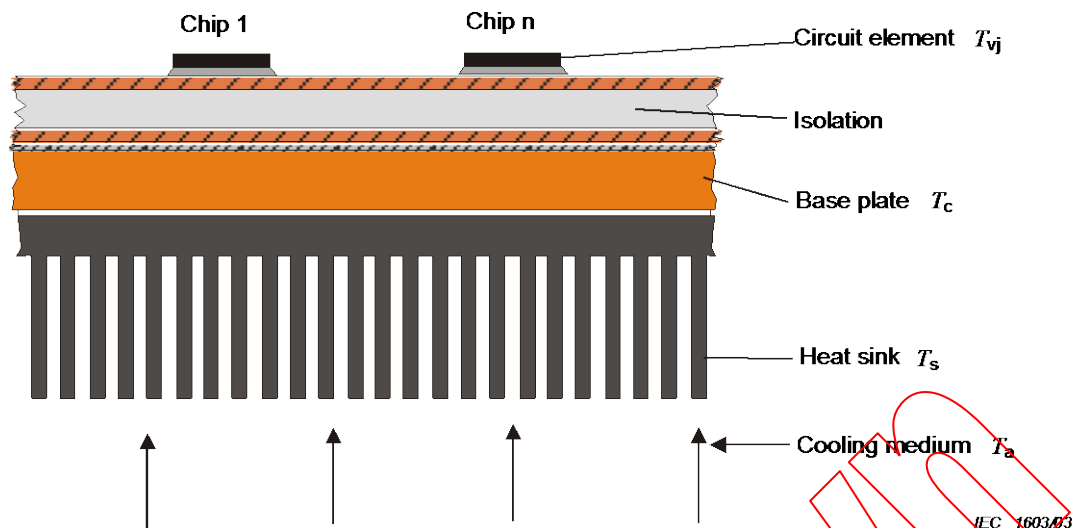


Figure 3a – Example of a cross-section of an isolated power device mounted on a heat sink, with the temperatures T_{vj} , ..., T_a

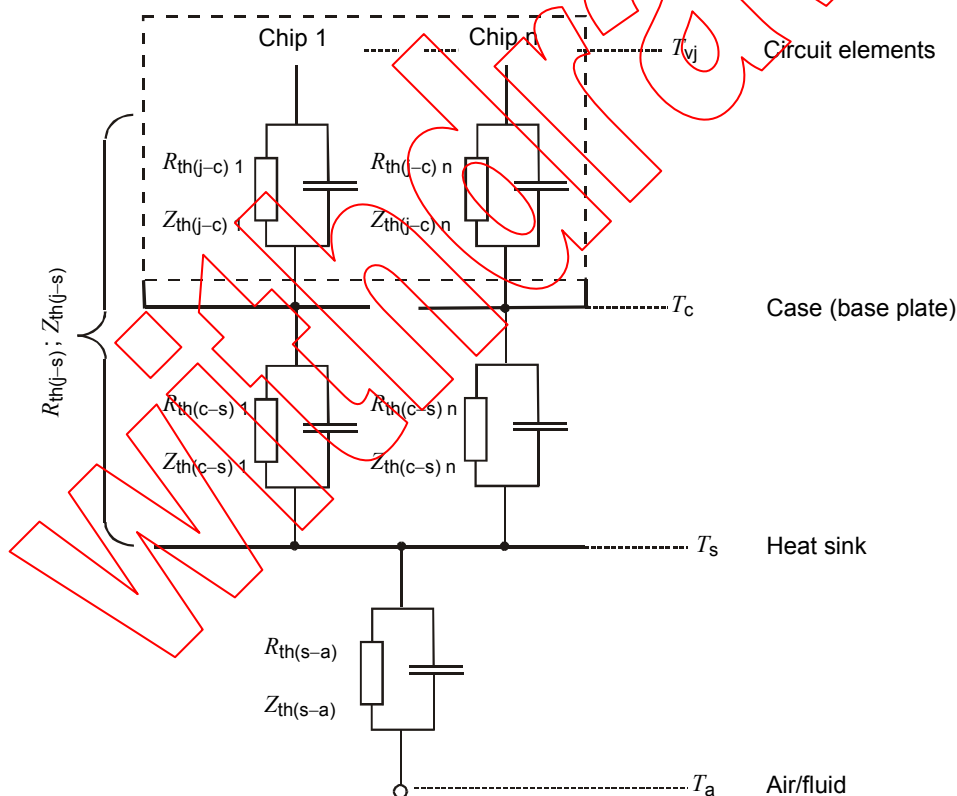


Figure 3b – Model of thermal resistances of circuit elements $R_{th(j-c)}$, $R_{th(c-s)}$, $R_{th(s-a)}$, resp. $Z_{th(j-c)}$, $Z_{th(j-s)}$ and $Z_{th(j-a)}$, schematically

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-s)} + R_{th(s-a)} \quad (6)$$

$$Z_{th(j-a)} = Z_{th(j-c)} + Z_{th(c-s)} + Z_{th(s-a)} \quad (7)$$

5.3.6.1 Thermal resistance junction to case ($R_{th(j-c)}$)

The maximum value of thermal resistance junction to case per circuit element for case rated devices is specified as

$$R_{th(j-c)} = (T_{vj} - T_c) / P_{tot} \quad (8)$$

where

T_{vj} is the virtual junction temperature of the functional circuit element (chip);

T_c is the measured temperature of the case (base plate);

P_{tot} is the dissipation of the functional circuit element.

5.3.6.2 Thermal resistance case to heat sink ($R_{th(c-s)}$)

Maximum or typical value of thermal resistance case to heat sink of the isolated case rated devices ("module"), when the case is mounted according to 5.2.6 Note 1.

5.3.6.3 Thermal resistance case to heat sink per circuit element ($R_{th(c-s)}(X)$) (where appropriate)

Maximum or typical value of thermal resistance case to heat sink of the respective functional circuit element "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)) of the isolated case rated devices ("module"), when the case is mounted according to 5.2.6 Note 1.

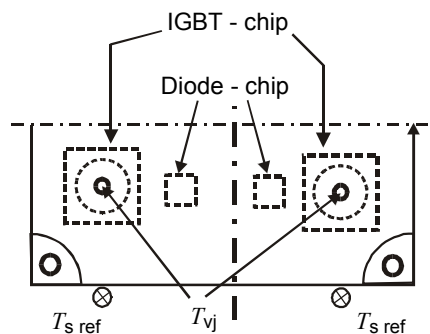
$$R_{th(c-s)}(X) = (T_{vj} - T_s) / P_{tot}(X) \quad (9)$$

where $P_{tot}(X)$ is the total power dissipation of the respective functional circuit element "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M) at the specified load, transferred under the chip from the base plate (cooling surface of the case) to the heat sink.

5.3.6.4 Thermal resistance junction to heat sink ($R_{th(j-s)}$)

Maximum or typical value of thermal resistance junction to heat sink (for heat sink rated isolated devices) when the device is mounted according to clause 5.2.6 Note 1.

$$R_{th(j-s)} = (T_{vj} - T_s) / P_{tot} \quad (10)$$



IEC 1605/03

NOTE The recommended reference point T_{sref} for T_s is as near to the chip as possible along the long side of the module on the heat sink measured from above, because this is generally easier to access than from underneath through the heat-sink. The thermal resistance $R_{th(c-s)}$ depends on several mechanical parameters such as type and thickness of the used thermal compound grease (which should be specified in manufacturer's mounting instructions, for example 30 μm to 50 μm), the maximum deviation of flatness of the cooling surface of the device's base plate and of the heat sink and the mounting torque of the fixing screws, as per specified mounting instructions.

Figure 4a – Case rated, seen from above

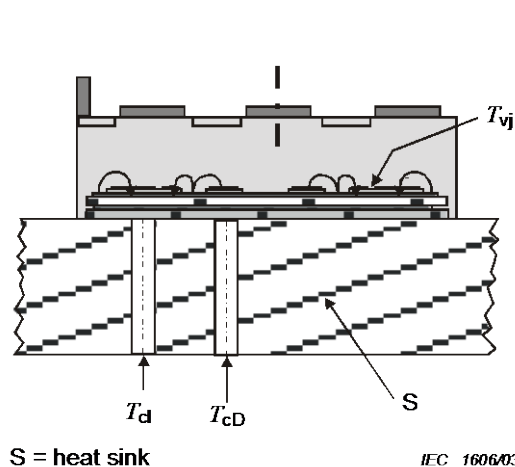


Figure 4b – Case-rated, cross section

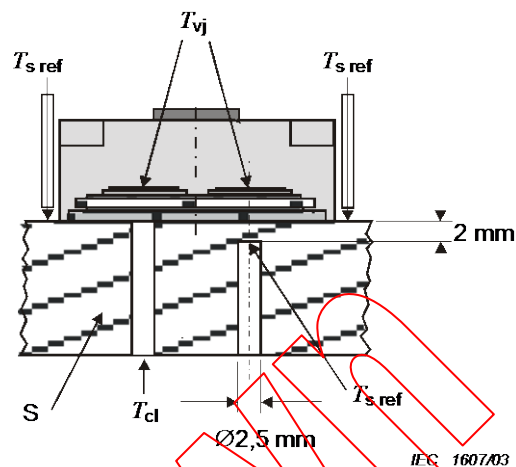


Figure 4c – Heat-sink rated, cross section

Figure 4 – Reference points for measuring the temperatures T_{vj} , T_c , T_{cl} , T_{cd} , T_s to be specified for an isolated power device, seen from above

In Figure 4a, T_s is taken from above at hottest accessible point, nearest to the circuit element (chip) (see note below).

In Figure 4b, the isolated device is seen as a cross-section from the front. $T_c = T_{cl}$ (under IGBT-chip) respectively T_{cd} (under a diode chip) are taken from below.

In Figure 4c, the isolated device is without base plate (or not accessible base plate): T_s is taken from underneath through a specified sack hole of 2,5 mm diameter ending at 2 (± 1) mm below the heat sink surface (to be specified, type test feature).

5.3.6.5 Transient thermal impedance Z_{th}

Thermal resistance as a function of time t of the pulse duration t_p elapsed after step change of power dissipation as $Z_{th(j-c)}$ or $Z_{th(j-s)}$ and shall be specified in one of the following ways:

- A thermal resistance elements $R_{th1} \dots R_{thn}$ and thermal capacities $C_{th1} \dots C_{thn}$ of a thermal RC network; or
- B thermal resistance elements $R(i)$ and thermal time constants $\tau(i)$ with $i = 1$ to n of the resulting equivalent thermal RC network – for thermal calculation and simulation of $T_{vj} = f(t)$, derived from a Fourier-analysis of $Z_{th}(t)$ by measuring $T_{vj} = f(t)$ (preferred).
- C $Z_{th(j-c)}(t)$ curve for single pulse operation, starting at a time interval of an application-typical pulse width – for example 10 ms for a thyristor, 10 μ s for an IGBT – and ending at steady state $R_{th(j-c)}$ (see Figure 5).

A curve should be given (see Figure 5) showing the maximum transient thermal impedance Z_{th} as a function of time t_p , elapsed after a step change of power dissipation, extending from steady state value $R_{th(j-c)}$ at times > 1 s down to 1 ms or less (10 μ s for IGBT and MOSFET modules) or, alternatively, a mathematical elements relation ($R(i)$ and $\tau(i)$) shall be specified.

NOTE 1 $\tau(i)$ is the time constant of the $R(i)$ portions of the Fourier analysis for calculation and simulation using a computer.

NOTE 2 Annex A of IEC 60747-2 (rectifier diodes) and Annex A of IEC 60747-6 (thyristors) apply.

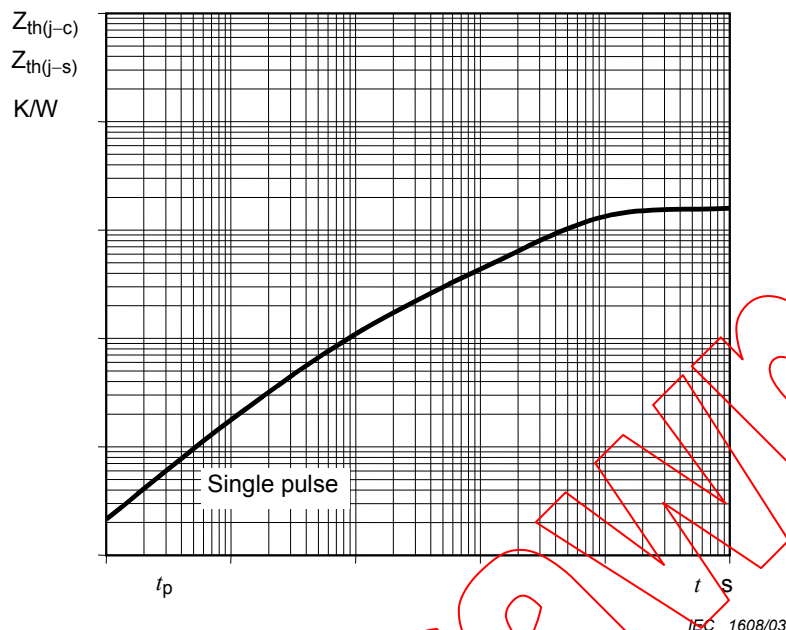


Figure 5 – Transient thermal impedance $Z_{th(j-c)} = f(t_p)$ of an isolated power semiconductor device as a function of the pulse duration time t_p , elapsed after a step change of applied power dissipation

5.3.7 Mechanical characteristics

For mechanical characteristics, see IEC 60747-1, Chapter VI, Clause 7.

5.3.7.1 Outline drawing, indication of pin-out and circuit diagram

Dimensions with tolerances shall be specified, where appropriate, as well as identification of terminals and a reference to a standard IEC outline drawing and base drawing, where appropriate (see IEC 60191-2). Outline tolerances should be based on the tolerance classes specified in ISO 2768-2.

5.3.7.2 Mass (m) of the device

Quantity mass shall be given without accessories (mounting hardware).

5.3.7.3 Marking

The devices shall be clearly and indelibly marked as follows:

- manufacturer's name or identification (logo);
- manufacturer's or supplier's type no. or designation;
- date code, (preferred structure: YYWW, for "year, year, week, week")
- identification of the terminals, where appropriate (see pin #1-marking rules IEC 60191-4).

NOTE 1 A bar code may be applied in addition, if the space is sufficient, otherwise on the smallest packing unit.

NOTE 2 The permanence of marking should be secured (see IEC 60749-9).

5.3.7.4 Electrostatic discharge (ESD) sensitive devices (where appropriate)

IGBTs, MOSFETs, intelligent power semiconductor devices (IPMs) and also some diodes or other should be marked with the relevant sign (Figure 5 of IEC 60747-1), at least on their smallest packing unit. IEC 60749-26 or IEC 60749-27 apply.

5.3.7.5 Method of intended attachment

The method of intended attachment is to the electrical circuit of application (i.e. soldering, FASTON, screwing, wrapping of termination, pressure contacting) should be indicated, together with mounting instructions.

5.3.8 Climatic characteristics

NOTE Table 1 of IEC 60721-3-3 and Annex C of this standard refer.

6 Verification of ratings (limiting values)

6.1 Isolation voltage between terminals and base plate (V_{isol})

Specified in point b) of 4.1.2, IEC 60664-1 and 2.4.6.17 of IEC 61287-1 ($t = 10$ s).

a) Purpose

The purpose of this test is to prove the ability of the isolated power device to withstand the rated isolation voltage.

b) Circuit diagram

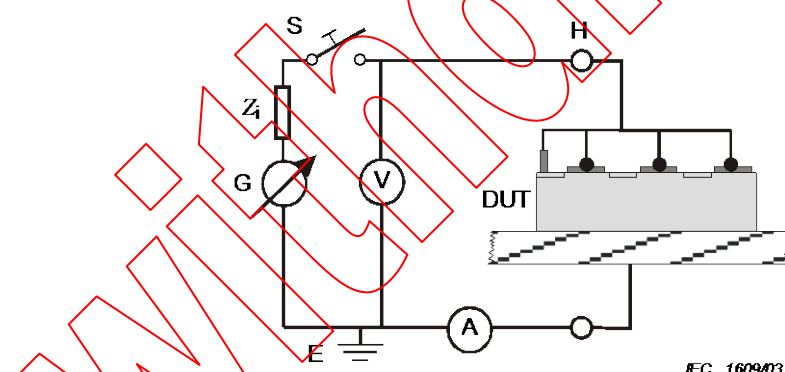


Figure 6 – Basic circuit diagram for isolation breakdown withstand voltage test (“high pot test”) with V_{isol}

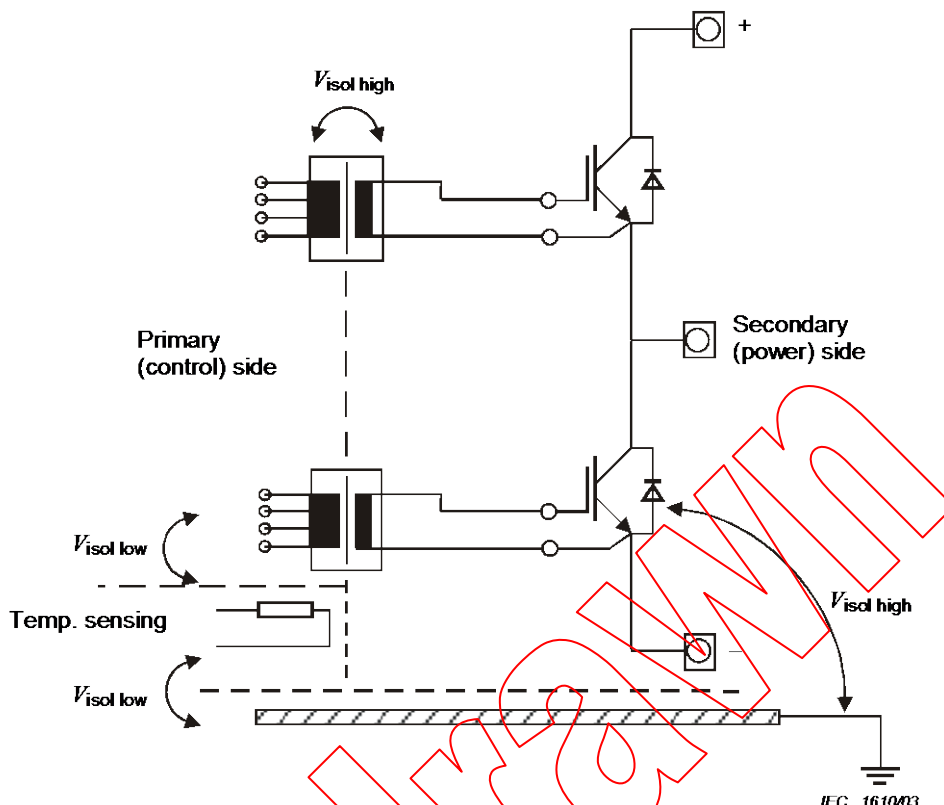


Figure 7 – Isolation levels of an isolated power device with integrated driver and protection functions

Full isolation voltage between high potential main terminals connected together and both grounded base plate with low voltage control terminals, both connected together.

Reduced isolation voltage is applied between low-voltage control (temperature-sensing) terminals and base plate.

c) Circuit description and requirements (see Figure 6)

G = voltage source with high impedance Z_i , capable to supply V_{isol}

S = main switch

V = voltmeter for V_{isol}

A = milli-ampere meter or current probe for I_{isol}

E = earth/ground potential

H = high potential terminal

d) Test procedure

The voltage source, G, is capable of supplying the isolation voltage V_{isol} as a.c. or d.c. voltage with a high internal impedance Z_i to limit the possible break-through current in case of breakdown of the device under test (DUT). All main terminals and high-voltage control terminals are connected together and connected to the high potential output terminal, H, of the voltage source G. The base plate of the DUT, respectively its metallized cooling surface and all low-voltage terminals, are connected to ground potential E. An ampere meter or current probe A is applied to measure the isolation leakage current.

NOTE Any low-voltage control terminal shall be grounded with the base plate.

Then the switch S is closed and the voltage gradually increased from about zero to 50 % of the V_{isol} rated and then slowly to full rated value V_{isol} maintaining it for 1 min for the

test or for 1,2 times that value for 1 s in a 100 % production test, with the leakage current below the specified value for passed devices. For details see 4.1.2.3 of IEC 60664-1.

e) **Specified conditions**

- ambient or case temperature;
- V_{isol} ;
- I_{isol} as max test limit;
- test time t , if less than 60 s.

6.2 Peak case non-rupture current

6.2.1 Peak case non-rupture current (I_{RSMC}) of isolated diode and thyristor devices

NOTE The test method is specified in 7.3.4 of IEC 60747-2 for diodes and 9.3.6 of IEC 60747-6 for thyristors.

6.2.2 Peak case non-rupture current (I_{CNR}) of bipolar transistors, IGBTs and MOSFETs

NOTE This test method is still under discussion. For a definition, see 3.10.2. For details, see 5.2.2.2 and for the proposed test methods see Annex A.

6.3 Maximum terminal current (I_{trms})

The purpose of this test is to prove the ability of all main terminals of the isolated power device to withstand the rated maximum terminal current without exceeding its maximum allowable temperature T_t (to be specified, see 5.2.3 above).

NOTE The relevant part of IEC 60747 concerning the relevant functional circuit elements applies for the value of the rated (absolute maximum) current.

6.4 Surge (non-repetitive) current test (I_{FSM} ; I_{TSM})

NOTE For wire bonded devices such as diode, thyristor, IGBT and MOSFET modules, which can be used also as input rectifiers, the robustness of the bonds can be tested by the surge (non-repetitive) current test (I_{FSM}). See IEC 60747-2, which applies for the diode part of the device and IEC 60747-6, which applies for the thyristor part of the device.

7 Methods of measurement of characteristics

Purpose

The purpose of this measurement is to confirm that the characteristic values are maintained.

7.1 Rated partial discharge inception and extinction voltages (V_i) (V_e)

7.1.1 Rated partial discharge inception voltage (V_i)

Between high potential terminals and base plate (where appropriate).

7.1.2 Rated partial discharge extinction voltage (V_e)

Between high potential terminals and base plate (where appropriate).

NOTE Measurement procedures apply as described in IEC 60270, in 4.1.2.4 of IEC 60664-1 and in 2.4.6.18 of IEC 61287-1.

7.2 Parasitic stray inductance between main terminals (L_P)

See also 3.12, 5.3.2 and Figure 2.

This measuring method uses reduced voltage V_{CC} and the di/dt of diodes incorporated in the device at switch-off, sensing the voltage at outside main terminals. This is usable for single switch devices as well as for half bridge circuit devices (DUAL modules), and half bridge branches of sixpack inverter devices.

a) Purpose

To measure the voltage step dV caused by the internal parasitic stray inductance at current decline and $(di_F/dt)_{off}$ of a diode path at switch-off to calculate the parasitic inductance L_P of the main current path from the main current-in-terminal via the switching functional circuit element to the main current-out-terminal of an isolated power semiconductor device under specified conditions. $L_P = -dV / (di_F/dt)$

Withdrawn