

INTERNATIONAL STANDARD



Semiconductor devices – ~~Discrete devices~~
Part 15: Discrete devices – Isolated power semiconductor devices



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**SEMICONDUCTOR DEVICES –
~~DISCRETE DEVICES~~****Part 15: Discrete devices – Isolated power semiconductor devices**

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IEC 60747-15 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

This third edition cancels and replaces the second edition published in 2010. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) The intelligent power semiconductor modules (IPM), which was previously excluded from the first and second edition, is now included in this document (Annex C);
- b) The thermal resistance is described for each switch (6.2.4);
- c) Added isolation test between temperature sensor and terminals, in case there is an agreement with the user (6.1.2).

The text of this International Standard is based on the following documents:

Draft	Report on voting
47E/832/FDIS	47E/844/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

This International Standard is to be used in conjunction with IEC 60747-1:2006 and Amendment 1: 2010.

A list of all parts in the IEC 60747 series, published under the general title *Semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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SEMICONDUCTOR DEVICES – ~~DISCRETE DEVICES –~~

Part 15: Discrete devices – Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the requirements for isolated power semiconductor devices ~~excluding devices with incorporated control circuits~~. These requirements are additional to those given in other parts of IEC 60747 for the corresponding non-isolated power devices and parts of IEC 60748 for ICs.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-1:2007, *Environmental testing – Part 2-1: Tests – Test A: Cold*

IEC 60270:2015, *High-voltage test techniques – Partial discharge measurements*

IEC 60664-1:~~2007~~2020, *Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests*

IEC 60721-3-3:~~1994~~2019, *Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*
IEC 60747-1:2006/AMD1:2010

IEC 60747-2:2016, *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*

IEC 60747-6:2016, *Semiconductor devices – Part 6: Thyristors*

IEC 60747-7:2019, *Semiconductor discrete devices and integrated circuits – Part 7: Bipolar transistors*

IEC 60747-8:2021, *Semiconductor devices – Part 8: Field-effect transistors*

IEC 60747-9:2019, *Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)*

IEC 60748 (all parts), *Semiconductor devices – Integrated circuits*

IEC 60749-5:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-10:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock*

IEC 60749-12:2017, *Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency*

IEC 60749-15:2020, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices*

IEC 60749-21:2011, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-25:2003, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-34:2010, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1

isolated power semiconductor device

semiconductor power device that contains an integral electrical insulator between the cooling surface or base plate and any isolated circuit elements

3.2

constituent parts of the isolated power semiconductor device

3.2.1

switch

any single component that performs a switching function in an electrical circuit, e.g. diode, thyristor, MOSFET, etc.

Note 1 to entry: A switch might be a parallel or series connection of several chips with a single functionality.

3.2.2

base plate

part of the package having a cooling surface that transfers the heat from inside to outside

3.2.3

main terminal

terminal having a high potential of the power circuit and carrying the main current

Note 1 to entry: The main terminal can comprise more than one physical connector.

3.2.4

control terminal

terminal having a low current capability for the purpose of control function, to which the external control signals are applied or from which sensing parameters are taken

3.2.4.1

high voltage control terminal

terminal electrically connected to an isolated circuit element, but carrying only low current for control function

Note 1 to entry: Examples include current shunts and collector sense terminals having the high potential of the main terminals.

3.2.4.2

low voltage control terminal

terminal having a control function and isolated from the high voltage control terminals

Note 1 to entry: Examples include the terminals of isolated temperature sensors and isolated gate driver inputs, etc.

3.2.5

insulation layer

integrated part of the device case that insulates any part having high potential from the cooling surface or external heat sink and any isolated circuit element

3.3

peak case non-rupture current

peak current, which will not lead to a rupture of the package, ejecting plasma and massive particles under specified conditions

3.4

thermal interface material

heat conducting material between base plate and external heat sink

4 Letter symbols

4.1 General

General letter symbols are defined in Clause 4 of IEC 60747-1:2006.

4.2 Additional subscripts/symbols

p parasitic

t terminal

isol isolation

~~m~~ – mount

4.3 List of letter symbols

4.3.1 Voltages and currents

Terminal current

I_{tRMS}

Isolation voltage

V_{isol}

Partial discharge inception voltage

V_{i}

Partial discharge extinction voltage

V_{e}

Isolation leakage current

I_{isol}

~~Peak case non-rupture current (for diode and thyristor devices) — I_{RSMC}~~

~~Peak case non-rupture current (for IGBT and MOSFET devices) — I_{CNR}~~

4.3.2 Mechanical symbols

Mounting torque for screws to heat sink	M_s
Mounting torque for terminal screws	M_t
Mounting force	F
~~Maximum~~ Acceleration in all 3 axis (x, y, z)	a
Mass	m
Flatness of the case (base plate)	e_c
Flatness of the ~~cooling~~ heat sink surface ~~(heat sink)~~	e_s
Roughness of the case (base plate)	R_{Zc}
Roughness of the ~~cooling~~ heat sink surface ~~(heat sink)~~	R_{Zs}
Thickness of thermal interface material (case – heat sink)	$d_{(c-s)}$

4.3.3 Other symbols

~~Total maximum power dissipation per switch at $T_e = 25\text{ °C}$~~	~~P_{tot}~~
Parasitic inductance, effective between terminals and chips ~~(to be specified)~~	L_p
Parasitic capacitance between terminals and cooling surface (case, base plate, ground)	C_p
Lead resistance between terminal x and ~~related switch~~ internal device connection x'	r_{xx}
Terminal temperature	T_t
Number of power load cycles until failure of a percentage p of a population of devices	$N_{f;p}$

5 Essential ratings (limiting values) and characteristics

5.1 General

Isolated power semiconductor devices should be specified as case rated or heat sink rated devices. The ratings and characteristics should be quoted at a temperature of 25 °C or another specified elevated temperature. Requirements for multiple devices having a common encapsulation are described in 5.12 of IEC 60747-1:2006.

5.2 Ratings (limiting values)

5.2.1 Isolation voltage or isolation test voltage (V_{isol})

Maximum RMS or DC value between main terminals and high voltage control terminals at one side and low voltage control terminals (where appropriate) and base plate at the other side for a specified time.

5.2.2 Peak case non-rupture current ~~(I_{RSMC} or I_{CNR})~~ (where appropriate)

Maximum value for each main terminal that does not cause the bursting of the case or emission of plasma and particles.

5.2.3 Terminal current (I_{RMS}) (where appropriate)

Maximum RMS value of the current through the main terminal under specified conditions at minimum mounting torque M_t and maximum allowed terminal temperature ($T_{\text{tmax}} = T_{\text{stg}}$ or $T_{\text{tmax}} \leq T_{\text{vjmax}}$).

~~5.2.4 Total power dissipation (P_{tot})~~

~~Maximum value per switch at $T_e = 25^\circ\text{C}$ (or $T_s = 25^\circ\text{C}$), when $T_{\text{vj}} = T_{\text{vjmax}}$, at d.c. load.~~

5.2.4 Temperatures

5.2.4.1 Solder temperature (T_{sold}) (where appropriate)

Maximum solder temperature T_{sold} during solder process over a specified solder processing time t_{sold} .

5.2.4.2 Storage temperature (T_{stg})

Minimum and maximum storage temperature.

5.2.5 Mechanical ratings

5.2.5.1 Mounting torque for screws to heat sink (M_s)

Minimum and maximum mounting torque that shall be applied to the fixing screws to the heat sink.

5.2.5.2 Mounting torque for screws to terminals (M_t)

Minimum and maximum mounting torque that shall be applied to screwed terminals.

5.2.5.3 Mounting force (F)

Minimum and maximum mounting force for pressure mounted devices, fixed by clips, that shall be applied to the isolated pressure contact device.

5.2.5.4 Terminal pull-out force (F_t)

Maximum force.

5.2.5.5 Acceleration (a)

Maximum value along each axis (x, y, z).

5.2.5.6 Flatness of the heat sink surface (e_s) (where appropriate)

Maximum deviation from flatness for the heat sink surface over the whole mounting area.

5.2.5.7 Roughness of the heat sink surface (R_{Zs}) (where appropriate)

Maximum roughness of the heat sink surface over the whole mounting area.

5.2.6 Climatic ratings (where appropriate)

Limiting values of environmental parameters for the final application as follows:

- ambient temperature;
- humidity;
- speed and pressure of air;
- irradiation by sun and other heat sources;
- mechanical active substances;
- chemically active substances;
- biological issues,

shall be described in classes as specified in IEC 60721-3-3:19942019, Table 1.

5.3 Characteristics

5.3.1 Mechanical characteristics

5.3.1.1 Creepage distance along surface (d_s)

Minimum value of distance along surface of the insulating material of the device between terminals of different potential and to base plate.

NOTE 1 IEC 60112:2020 (details to comparative tracking index "CTI") and IEC 60664-1:20072020, 5.2 apply.

NOTE 2 Air gaps between plastic surface and grounded metal or between terminals of opposite polarity smaller than 1,0 mm (for pollution degree 2), or 1,5 mm (pollution degree 3) shorten the countable creepage distance considerably (details see 60664-1:20072020, examples). This is essential, if dust, moisture or dirt starts to cover the surface and increases the leakage current over surface, which might start burning the plastic encapsulation material.

5.3.1.2 Clearance distance in air (d_a)

Minimum value of distance through air between terminals of different potential of the isolated device and to base plate.

NOTE For details, see IEC 60664-1:20072020, 4.6 and 5.1 which show typical examples of various shapes of clearance distances.

5.3.1.3 Mass (m) of the device

Maximum value excluding accessories (mounting hardware).

5.3.1.4 Flatness of the case (base plate) (e_c) (where appropriate)

Maximum and minimum allowed deviation from flatness for the base plate and its direction (convex or concave).

5.3.2 Parasitic inductance (L_p)

Maximum or typical value between the main terminals of each main current path.

5.3.3 Parasitic capacitances (C_p)

Maximum value of parasitic capacitance between the specified main terminal(s) and the cooling surface.

5.3.4 Partial discharge inception voltage (V_{iM} or $V_{i(RMS)}$) (where appropriate)

Minimum peak value V_{iM} or RMS value $V_{i(RMS)}$ between the isolated terminals and the base plate (details, see IEC 60270:2015).

5.3.5 Partial discharge extinction voltage (V_{eM} or $V_{e(RMS)}$) (where appropriate)

Minimum peak value V_{eM} or RMS value $V_{e(RMS)}$ between the isolated terminals and the base plate (for details, see IEC 60270:2015).

5.3.6 Thermal resistances

5.3.6.1 Thermal resistance junction to case for case rated devices ($R_{th(j-c)X}$)

Maximum value of thermal resistance junction to a specified reference point at the case (base plate) per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)).

5.3.6.2 Thermal resistance case to heat sink ($R_{th(c-s)}$) (where appropriate)

Maximum or typical value of thermal resistance between two specified points at the case and at the heat sink of the case rated device ("module"), when the case is mounted according to manufacturer's mounting instructions.

5.3.6.3 Thermal resistance case to heat sink per switch ($R_{th(c-s)X}$) (where appropriate)

Maximum or typical value of thermal resistance between the two specified points of the case and the heat sink of the switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)) of the isolated case rated devices ("module"), when the case is mounted according to the manufacturer's mounting instructions.

5.3.6.4 Thermal resistance junction to heat sink for heat sink rated devices ($R_{th(j-s)X}$)

Maximum or typical value of thermal resistance junction to a specified point at the heat sink per switch "X" (for example of the diode (D), thyristor (T), IGBT (I) or MOSFET (M)), when the device is mounted according to the manufacturer's mounting instructions.

5.3.6.5 Thermal resistance junction to sensor ($R_{th(j-r)}$) (where appropriate)

Value of thermal resistance junction to an integrated temperature sensor when the device is mounted according to the manufacturer's mounting instructions.

NOTE—The position of this thermal resistance should be shown in the thermal resistance equivalent circuit.

5.3.7 Transient thermal impedance (Z_{th})

Thermal impedance as a function of the time elapsed after a step change of power dissipation for each thermal resistance specified in 5.3.6 and shall be specified in one of the following ways.

6 Measurement methods

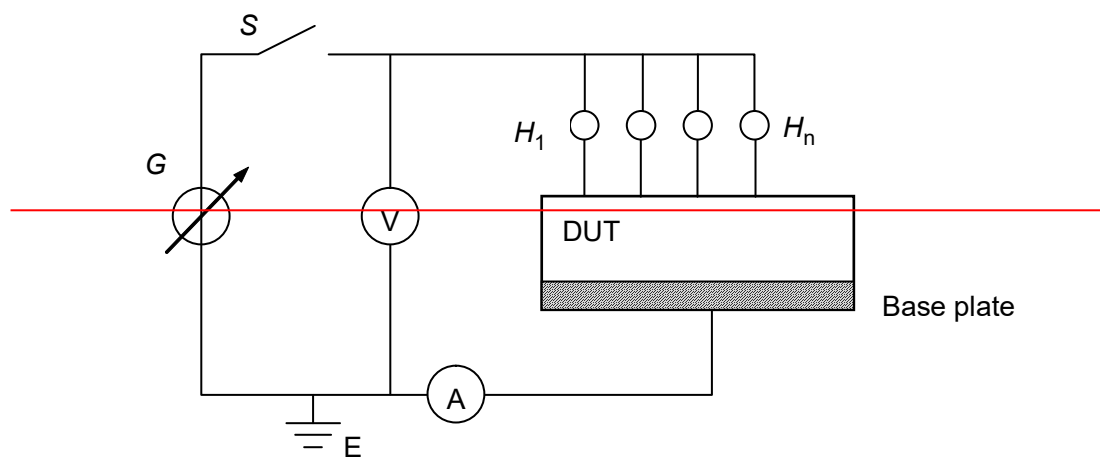
6.1 Verification of isolation voltage rating

6.1.1 Verification of isolation voltage rating between terminals and base plate (V_{isol})

– Purpose

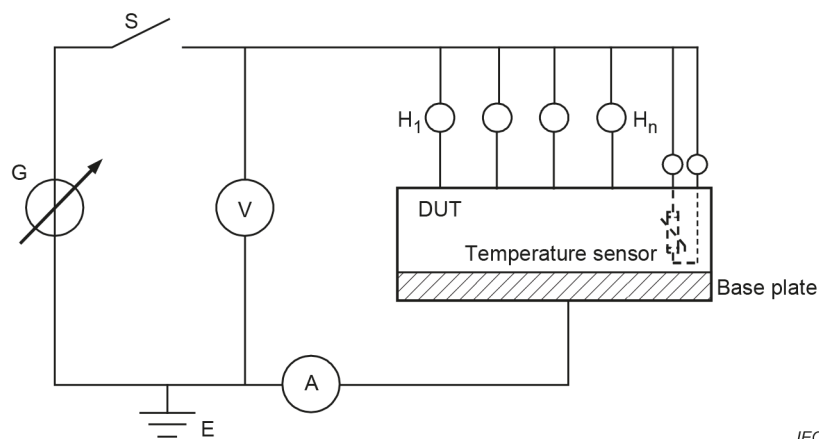
Proof of the ability of the isolated power device to withstand the rated isolation voltage.

– Circuit diagram



IEC 2976/10

See Figure 1.



IEC

Key

DUT	device under test
G	voltage source with high impedance, capable to supply V_{isol}
S	main switch
V	voltmeter for V_{isol}
A	ammeter or current probe for I_{isol}
$H_1 \dots H_n$	high potential terminal

Figure 1 – Basic circuit diagram for isolation breakdown withstand voltage test ("high pot test") with V_{isol}

The voltage source G is capable to supply the isolation voltage V_{isol} as the AC or DC voltage with a high internal impedance to limit the possible breakthrough current in case of breakdown of the DUT.

All main terminals and high voltage control terminals are connected together and connected to the high potential output terminal H of the voltage source G. The base plate of the DUT, respectively its metallized cooling surface and all low voltage terminals are connected to ground potential E. An amperemeter or current probe A is applied to measure the isolation leakage current.

If there is an agreement with user, perform an isolation test between the temperature sensor and the terminals (V_{isol1}) (See 6.1.2).

– Test procedure

Switch S is closed and the voltage is slowly raised to the specified value and maintained at that value for the specified time. The current measured on ammeter A shall not exceed the specified value. The voltage is then reduced to zero.

– Specified conditions

Specified in IEC 60664-1:2007/2020.

- Ambient or case temperature
- V_{isol}
- I_{isol} as maximum test limit
- Test time t , if less than 60 s.

6.1.2 Verification of isolation voltage rating between temperature sensor and terminals (V_{isol1})

– Purpose

To verify that the isolation voltage between the temperature sensor and the other terminals in case the temperature sensor is connected to the base plate potential.

– Circuit diagram

See Figure 2.

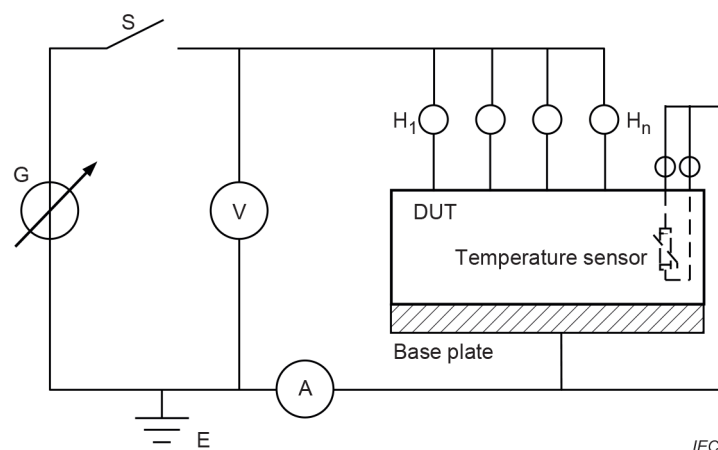


Figure 2 – Basic circuit diagram for isolation voltage test between temperature sensor and terminals (V_{isol1})

– Circuit description and requirements, test procedure and specified conditions

Similar as described in 6.1.1, but optionally a lower test voltage V_{isol1} may be specified and applied.

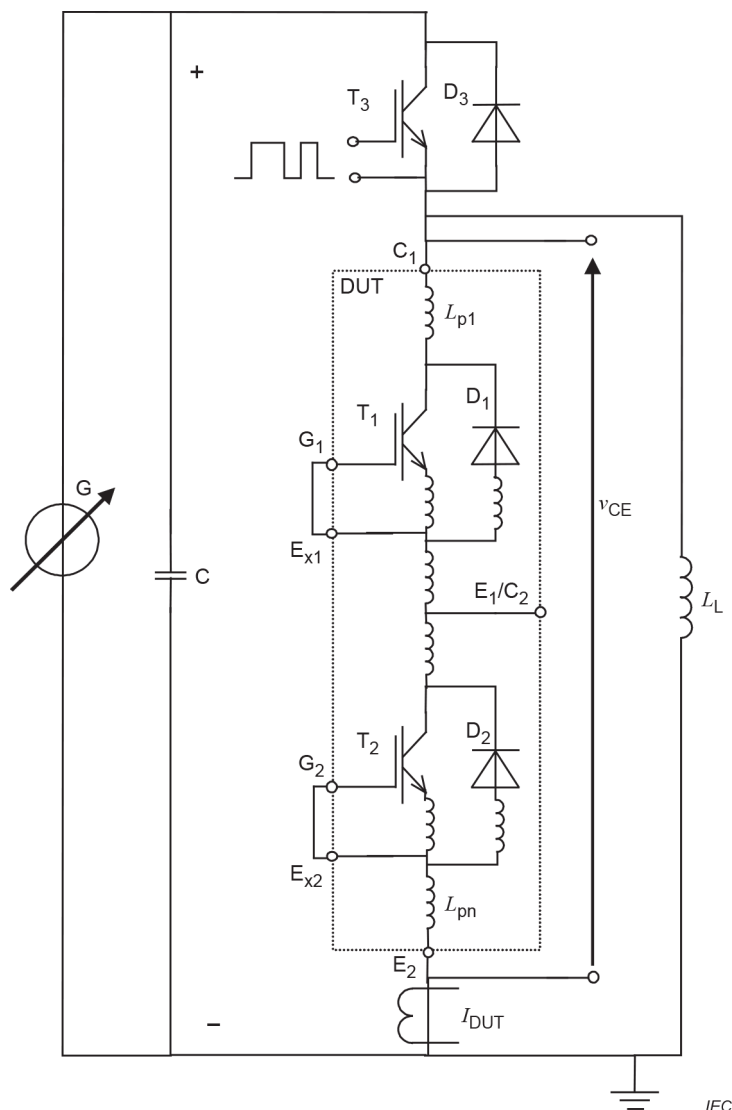
6.2 Methods of measurement

6.2.1 Partial discharge inception and extinction voltages (V_i) (V_e)

Between high potential terminals and base plate (where appropriate). See IEC 60270:2015 and IEC 60664-1:2007/2020.

6.2.2 Parasitic inductance (L_p)

- Purpose
To measure the parasitic inductance between two main terminals.
- Circuit diagram
See Figure 3.



Key

DUT	device under test T_1+T_2 , for example IGBT (Single or Dual – shown – or branch of a three phase arrangement), fast diode or MOSFET device
C	main capacitor bank as reservoir
L_L	load inductance, at least 100 times the parasitic inductance
$L_{p1} \dots L_{pn}$	portions of parasitic inductance L_p
I_{DUT}	current probe
G	voltage source to charge the capacitor
T_1	DUT, top switch (shown as IGBT in Figure 3)
T_2	DUT, bottom switch (shown as IGBT in Figure 3), optional
T_3	auxiliary IGBT switch

Figure 3 – Circuit diagram for measurement of parasitic inductances (L_p)

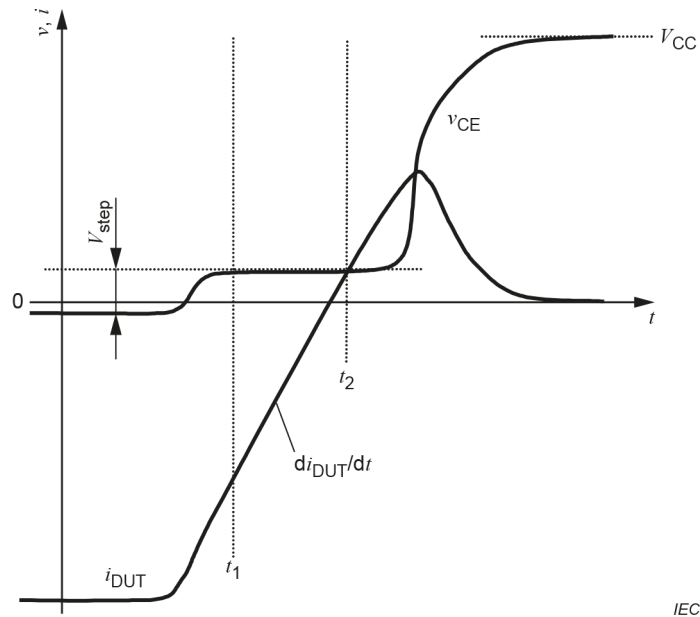


Figure 4 – Wave forms

– Circuit description and requirements

The circuit of Figure 3 consists of a DC supply G for the charge reservoir C; T_3 is an auxiliary switch, a gate drive unit for T_3 , the DUT inserted into the test set-up with the gate control terminals shorted, a dual channel oscilloscope, which senses the voltage v_{CE} between main terminals "C₁" and "E₂", a current probe, which senses the current i_{DUT} through the diode path of the DUT, connected to the dual channel oscilloscope. This measuring method uses reduced voltage V_{CC} and the di/dt of diodes incorporated in the device at switch-off, sensing the voltage at outside main terminals. This is usable for single switch devices as well as for half bridge circuit devices (DUAL modules).

– Measurement procedure

The waveforms observed by this measurement shown in Figure 4.

A pulsed current method is used. Auxiliary transistor T_3 switches the load current to the inductor L_L on and off. When T_3 is off, the current freewheels via the diodes of the DUT. When T_3 switches on again, it causes the current through the diodes to fall at an almost linear rate di_{DUT}/dt . During this time ($t_1 - t_2$), the voltage across the DUT forms at step of V_{step} caused by the internal parasitic inductance at current decline (di_{DUT}/dt). The value of the parasitic inductance of the main current path can be calculated from

$$L_p = V_{step} / |(di_{DUT}/dt)| \quad (1)$$

NOTE—Use low inductance (sheeted) bus baring and low inductance current probe.

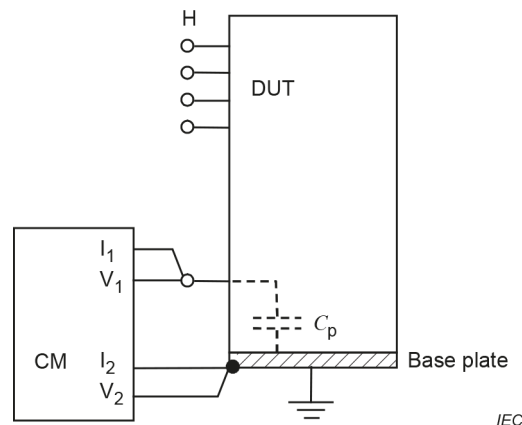
6.2.3 Parasitic capacitance terminal to case (C_p)

– Purpose

To measure the parasitic capacitance C_p between specified main terminal(s) and the case (base plate)

– Circuit diagram

See Figure 5.

**Key**

- C_p parasitic capacitance
H high potential terminal
CM capacitance meter

Figure 5 – Circuit diagram for measurement of parasitic capacitance (C_p)

– Measurement procedure

Mount the device to a grounded heat sink according to the manufacturer's mounting instructions. Connect the current source connector " I_1 " of the capacitance meter CM to the specified terminal and connector " I_2 " to ground (base plate) of the DUT. Connect the voltage sensing connector of the capacitance meter to test points " V_1 " and " V_2 " to ground. CM is set to the specified frequency. The capacitance C_p can be read on CM. For the measurement of the total coupling capacitance C_p connect all main terminals to each other and proceed with the measurement as described above.

– Specified conditions

- Measurement frequency f of the CM.

6.2.4 Thermal characteristics

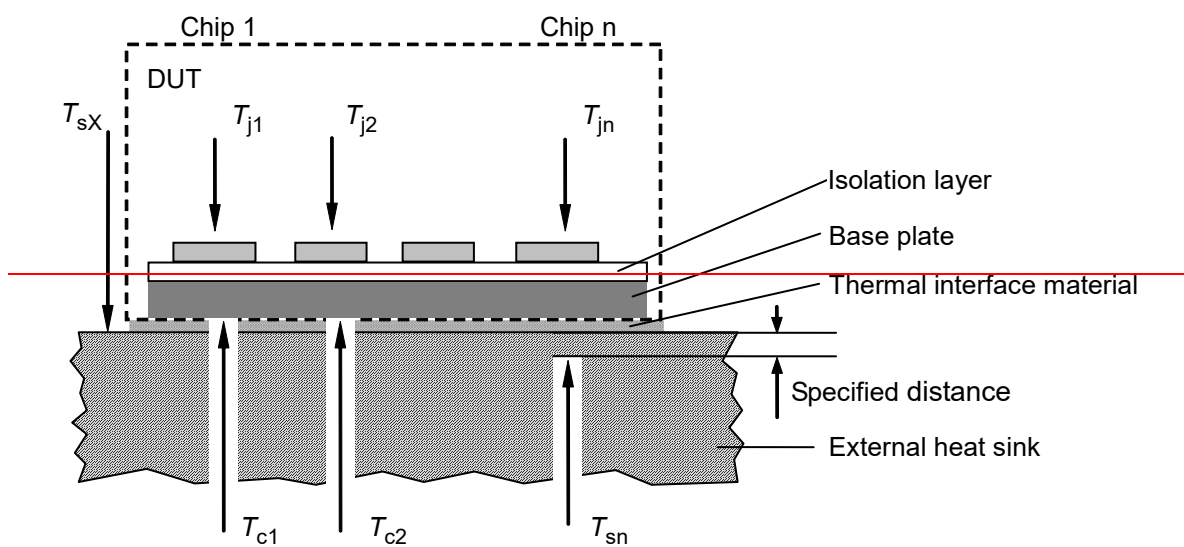
6.2.4.1 General description of measuring methods

– Purpose

To measure thermal characteristics between the switch and the cooling system.

– Reference points for temperature measurement and description

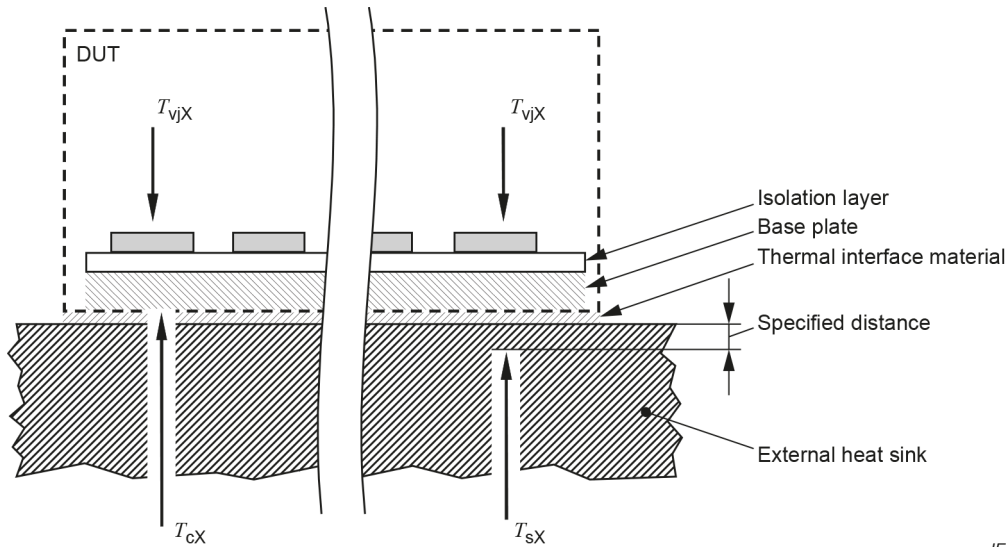
Same methods should be used as for the corresponding non-isolated device. Thermal resistance and impedance are measured in the same way as described in the documents for diodes IEC 60747-2:2016, thyristors IEC 60747-6:2016, bipolar transistors IEC 60747-7:2019, FETs IEC 60747-8:2021 and IGBTs IEC 60747-9:2019.



IEC 2980/10

Key

- $T_{j1...n}$ — junction temperature of chip 1 to n
- $T_{c1...n}$ — case temperature under chip 1 to n
- $T_{s1...n}$ — heatsink temperature under chip 1 to n
- T_{sx} — heatsink temperature at a specified surface point



IEC

Key

- T_{vjX} junction temperature of chip X
- T_{cX} case temperature under chip X
- T_{sX} heat sink temperature under chip X

Figure 6 – Cross-section of an isolated power device with reference points for temperature measurement of T_c and T_s

– Measurement procedure

Cross-sectional view of an isolated power device is shown in Figure 6.

$T_{eT_{cX}}$ is measured by a temperature measuring instrument from underneath through a small hole through the heat sink and any thermal interface material underneath the switch X(chip). $T_{eT_{sX}}$ is taken from above at hottest accessible point, nearest to the switch X(chip) or from underneath through a specified sack hole ending at 2 (±1) mm below the heat sink surface (to be specified, type test feature). $T_{jT_{vjX}}$ is determined using indirect methods like described in the individual documents.

NOTE—The thermal resistance $R_{th(j-s)}$ and $R_{th(c-s)}$ depends on several mechanical parameters such as type and thickness of the used thermal interface material (should be specified in manufacturer's mounting instructions, for example 30 to 50 μm), the maximum deviation of flatness of the cooling surface of the device's base plate and of the heat sink and the mounting torque of the fixing screws, as per specified mounting instructions.

6.2.4.2 Thermal resistance junction to case per switch (X) $R_{th(j-c)X}$

$$R_{th(j-c)} = (T_j - T_e) / P \quad (2)$$

where

T_j is the virtual junction temperature of the switch;

T_e is the temperature of the case (base plate) under the switch (chip);

P is the power dissipation of a switch (see Figure 5).

$$R_{th(j-c)X} = (T_{vjX} - T_{cX}) / P_X \quad (2)$$

where

X is the D (Diode), T (Thyristor), I (IGBT), M (MOSFET), B (BJT);

T_{vjX} is the virtual junction temperature of the switch X;

T_{cX} is the temperature of the case (base plate) under the switch X(chip);

P_X is the applied power dissipation at the each switch D, T, I, M, B.

Second index might be needed to distinguish multiple devices in one product (e.g., Inverter IGBTs and Brake IGBTs).

6.2.4.3 Thermal resistance case to heat sink per switch (X) $R_{th(c-s)X}$ or per device $R_{th(c-s)}$

$$R_{th(c-s)(X)} = (T_e - T_s) / P_X \quad (3)$$

where

X is the D (Diode), I (IGBT); M (MOSFET)

T_e is the temperature taken at the specified point of the case (as above) under the chip

T_s is the temperature of the heat sink, taken at the reference point for testing T_s specified

P_X is the complete power dissipation of the switch

P is the power dissipation of the complete device

$$R_{th(c-s)X} = (T_{cX} - T_{sX}) / P_X \quad (3)$$

where

- X is the D (Diode), T (Thyristor), I (IGBT), M (MOSFET), B (BJT);
- T_{cX} is the temperature taken at the specified point of the case (as above) under the chip;
- T_{sX} is the temperature of the heat sink, taken at the reference point for testing T_s specified;
- P_X is the applied power dissipation at the each switch D, T, I, M, B;
- P is the whole applied power dissipation of the device.

Second index might be needed to distinguish multiple devices in one product (e.g., Inverter IGBTs and Brake IGBTs).

– Specified conditions

- Mounting according manufacturer's instructions
- Thermal conductivity of the thermal interface material
- Reference points for thermal measurement

NOTE See Annex B for measuring method of the thickness of thermal interface material.

6.2.4.4 Thermal resistance junction to heat sink per switch (X) $R_{th(j-s)X}$ (for heat sink rated devices)

$$R_{th(j-s)} = (T_j - T_{sn}) / P \quad (4)$$

where

- T_j is the virtual junction temperature of the switch;
- T_{sn} is taken at the specified reference point n at the heatsink (see Figure 5);
- P is the power dissipation of the switch.

$$R_{th(j-s)X} = (T_{vjX} - T_{sX}) / P_X \quad (4)$$

where

- X is the D (Diode), T (Thyristor), I (IGBT), M (MOSFET), B (BJT);
- T_{vjX} is the virtual junction temperature of the switch X;
- T_{sX} is the temperature of the heat sink, taken at the reference point for testing T_s specified;
- P_X is the applied power dissipation at the each switch D, T, I, M, B.

Second index might be needed to distinguish multiple devices in one product (e.g. Inverter IGBTs and Brake IGBTs).

– Specified conditions

- Mounting according manufacturer's instructions
- Thermal conductivity of the thermal interface material
- Reference points for thermal measurement

6.2.4.5 Transient thermal impedance Z_{th}

– Measurement circuit and procedure

These are based on 6.2.4.2 to 6.2.4.4. Individual documents of the non-insulated devices apply.

$$\cancel{Z_{th(j-e)} = (|T_j(0) - T_e(0)| - |T_j(t) - T_e(t)|) / P} \quad (5)$$

$$\cancel{Z_{th(e-e)} = (|T_e(0) - T_e(0)| - |T_e(t) - T_e(t)|) / P} \quad (6)$$

$$\cancel{Z_{th(j-s)} = (|T_j(0) - T_s(0)| - |T_j(t) - T_s(t)|) / P} \quad (7)$$

$$Z_{th(j-c)X} = (|T_{vjX}(0) - T_{cX}(0)| - |T_{vjX}(t) - T_{cX}(t)|) / P_X \quad (5)$$

$$Z_{th(c-s)X} = (|T_{cX}(0) - T_{sX}(0)| - |T_{cX}(t) - T_{sX}(t)|) / P_X \quad (6)$$

$$Z_{th(j-s)X} = (|T_{vjX}(0) - T_{sX}(0)| - |T_{vjX}(t) - T_{sX}(t)|) / P_X \quad (7)$$

– Specified conditions

- Mounting according manufacturer's instructions
- Thermal conductivity of the thermal interface material
- Reference points for thermal measurement.

7 Acceptance and reliability

7.1 General requirements

In addition to the following subclauses, the requirements applicable to the non-isolated devices as given in the other relevant parts of IEC 60747 apply.

7.2 List of endurance tests

See Table 1.

Table 1 – Endurance tests

Subclause	Environmental testing – designation	Short form	Normative reference
7.2.1	High temperature reverse bias or high temperature blocking	HTRB	IEC 60749-5
7.2.2	High humidity and high temperature reverse bias or high humidity and high temperature blocking	H ³ TRB	IEC 60749-5
7.2.3	Power cycling (load) capability		IEC 60749-34
7.2.4	High temperature storage	HTS	IEC 60749-6
7.2.5	Low temperature storage	LTS	IEC 60068-2-48 ⁴ ₁
7.2.6	Thermal cycling	TC	IEC 60749-25
7.2.7	Resistance to solder heat		IEC 60749-15
7.2.8	Solderability		IEC 60749-21
7.2.9	Mechanical shock		IEC 60749-10
7.2.10	Vibration (variable frequency)		IEC 60749-12

⁴ ~~Withdrawn in 2008.~~

7.3 Acceptance defining criteria

See Table 2.

Table 2 – Acceptance defining characteristics for endurance and reliability tests

Acceptance defining characteristic	Acceptance criteria	Measurement conditions
I_{isol}	< USL	Specified V_{isol}
R_{th}	< USL	Mounting instructions
USL: upper specification limit.		

7.4 Type tests and routine tests

7.4.1 Type tests

The experience which has been obtained with other isolated power semiconductor devices, using the same or similar components such as switches or packages, should be considered when deciding which tests are mandatory.

Type tests are carried out on new products on a sample basis, in order to determine the electrical and thermal and mechanical and climatic ratings (limiting values) characteristics to be given in the data sheet and to establish the test limits for future routine tests. Some or all of the tests should be repeated from time to time on samples drawn from current production or deliveries so as to confirm that the quality of the product continuously meets the requirements.

The minimum type tests to be carried out are as follows.

New isolated power semiconductor devices should undergo the type tests listed in Table 3, marked with "X" (X = mandatory). Some of the type tests are destructive.

Table 3 – Minimum type and routine tests for isolated power semiconductor devices

Subclause	Items	Type test	Routine test	Destructive
5.2.1, 6.1	Isolation voltage (V_{isol}), (V_{isol1})	X	X	
5.2.2, Annex A	Peak case non-rupture current ~~I_{RSMC}~~ I_{CNR}	X ^a		X
5.3.1	outline dimensions, creepage, clearance	X		
5.3.1.4	flatness of base plate ~~or of cooling surface~~	X	X ^b	
5.3.6, 6.2.4	thermal resistances (R_{th})	X		
5.3.7, 6.2.4.5	transient thermal impedance (Z_{th})	X		
5.3.2, 6.2.2	parasitic inductance (L_{p})	X ^a		
5.3.3, 6.2.3	parasitic capacitance (C_{p})	X ^a		
5.3.4, 5.3.5, 6.2.1	partial discharge voltages (V_{im} or $V_{\text{i(RMS)}}$) / (V_{em} or $V_{\text{e(RMS)}}$)	X ^a	X ^b	
5.2.5.4	terminal pull-out force (F_{t})	X	~~X^b~~	X
7.2.6 ^c	thermal cycling	X		X
7.2.3 ^c	power cycling (load)	X		X
7.2.9 ^c , 7.2.10 ^c	mechanical ~~tests~~ shock, vibration	X		X
5.2.6	climatic ~~characteristics classification~~ ratings	X ^a		
NOTE Tests for isolation voltage, partial discharge voltage, creepage and clearance distance should be based on each standard which should be applied to any final equipment using the isolated power semiconductor device. For example, see ~~IEC 60950 (Safety information technology, IEC 61287 (rolling stock))~~ IEC 62368-1, IEC 61287-1, etc.				
^a Type test only for devices with specified maximum values.				
^b Routine test only for devices with specified maximum or minimum values.				
^c See Table 1 for normative references of test.				

7.4.2 Routine tests

The routine tests should be carried out on the current production or deliveries normally on a 100 % basis. The ratings and characteristics specified in the data sheet should be verified for each criterion or specimen. Routine test may comprise a selection of the isolated devices into groups of routine tests in Table 3. The minimum routine tests to be carried out on isolated devices are listed in Table 3. Other routine tests are carried out as described in the other parts of the IEC 60747, which is valid for the particular switch.

~~D_2 = inverse diode of T_2 , low side~~

~~G_4 = DC supply voltage source V_{GG} , which can be switched off from mains under all conditions~~

~~$GU1$ = gate drive unit of T_4~~

~~$GU2$ = gate drive unit of T_2~~

~~L_{Load} = load inductance~~

~~L_s = parasitic inductance of the circuit (40 nH to 250 nH)~~

~~R_e = discharge resistor for protection purposes~~

~~R_G = gate resistor~~

~~R_i = internal source resistance~~

~~R_s = fuse resistor, mostly set to zero~~

~~S_4 = auxiliary switch (IGBT), high side~~

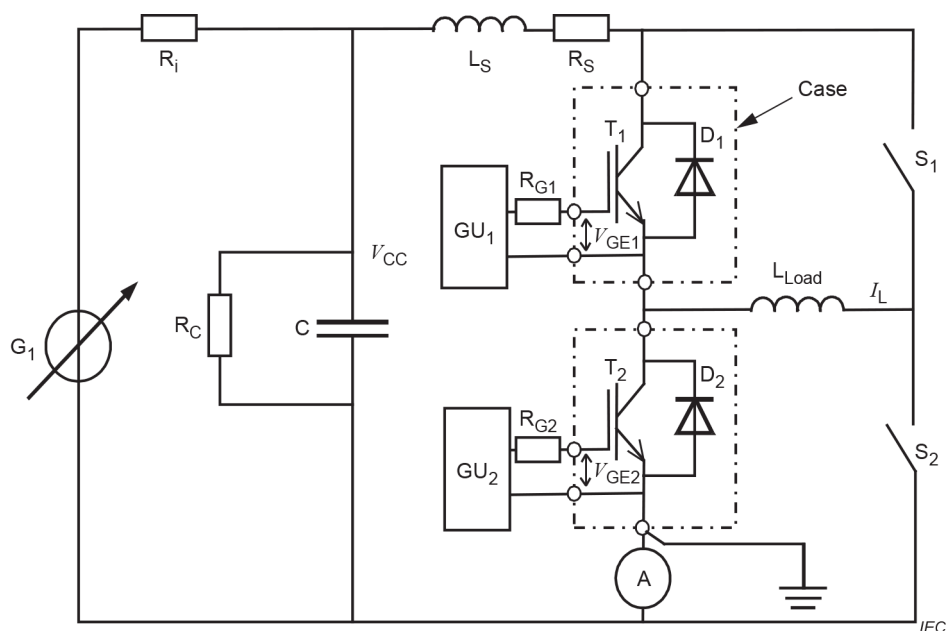
~~S_2 = auxiliary switch (IGBT), low side~~

~~T_4 = high side IGBT switch = device under test (DUT)~~

~~T_2 = low side IGBT switch~~

~~I_L = load current~~

~~V_{GE} = gate voltage~~



Key

- A Ammeter to measure the device current which can be peak case non-rupture current, if the case did not burst, monitored by a current probe having low inductance
- C line capacitor bank, chargeable to full voltage
- D₁ inverse diode of T₁, high side
- D₂ inverse diode of T₂, low side
- G₁ DC supply voltage source V_{CC} , which can be switched off from mains under all conditions
- GU₁ gate drive unit of T₁
- GU₂ gate drive unit of T₂
- L_{Load} load inductance
- L_s stray inductance of the circuit (specified value)
- R_c discharge resistor for protection purposes
- R_{G1} gate resistor of T₁
- R_{G2} gate resistor of T₂
- R_i internal source resistance
- R_s fuse resistor, mostly set to zero
- S₁ auxiliary switch (IGBT), high side
- S₂ auxiliary switch (IGBT), low side
- T₁ high side IGBT switch = device under test (DUT)
- T₂ low side IGBT switch
- I_L load current
- V_{GE1} gate voltage of T₁
- V_{GE2} gate voltage of T₂

Figure A.1 – Circuit diagram for test of peak case non-rupture current I_{CNR}

The set-up consists of a two-quadrant converter with two identical isolated IGBT devices. S_1 and S_2 are auxiliary switches, for example IGBT devices, used to establish the desired load current and to induce a short circuit failure. T_1 and T_2 are identical isolated IGBT devices (SINGLE switch or both in a half bridge circuit as DUAL switch). [This Annex A describes testing methods using \$S_2\$.](#)

A.3 Test procedure

- Test A:

First, close switch S_2 , turn on T_1 , the load current increases as defined by load inductance L_{Load} . After I_L have exceeded the safe operating area (SOA) for turn-off of T_1 , it is attempted to turn off T_1 . The initial part of the turn-off process takes place, the current in the device is reduced and part of the current is commuted to the diode D_2 . The device T_1 then undergoes a turn-off failure. The diode in the low side device D_2 carries substantial current at this instant. The failure of T_1 forces the diode D_2 to turn off at virtually unlimited di/dt , drawn by L_{Load} . This is outside the diode SOA, and the diode D_2 also fails.

- Test B:

T_1 is turned on until a substantial load current is reached. At this moment the device T_2 is turned on. It is induced to fail, because it sees the full voltage together with full current. The device T_1 then goes into desaturation and also fails. ~~(Top-bottom shoot-through which creates a short circuit between plus bus bar and minus bus bar, discharging the capacitor bank, creating an arc in the devices. This leads to production of gases of the surrounding plastic gel etc. until the energy of the capacitor bank is used). In reality such a failure could be due to cosmic ray or due to thermal overload. Manipulating the device can artificially induce it.~~

~~Tests C and further tests:~~

These tests are executed until a value of stored energy of the capacitor bank and of peak current is found, which is not high enough to rupture or break the case. The values of achieved peak current $I_C = I_{CNR}$ peak case non-rupture current, V_{CC} , C_{max} and of $E_C = \frac{1}{2} C V_{CC}^2$ are monitored. ~~The value I_{CNR} is the value of a percentage (10 % = 2/20) of a tested population (minimum 10 pieces) of devices, at which the case did not burst, or case split, but did not eject internal particles.~~

A.4 Post test measurements and criteria

The DUT is subjected to a visual test, whether cracks and signs of plasma from arcing inside are visible from outside. There shall be no signs of particles thrown out nor shall there be evidence that the device has externally melted or burst into flames.

~~NOTE 2 The ejection of particles is unavoidable for energies higher than about 10 kJ. What can be achieved by good design is that no massive parts are ejected, which can cause severe consequential damage.~~

A.5 Specified conditions

- Case or virtual junction temperature ($T_c = 25\text{ °C}$, $T_{vj} = 25\text{ °C}$ or 125 °C)
- Supply voltage V_{CC}
- Capacitance of capacitor bank C
- Stored energy of capacitor bank E_C
- ~~Parasitic~~Stray inductance of short circuit L_{SC}
- Load current I_L

- Gate voltage V_{GEon} and V_{GEoff}
- Gate resistance R_{Gon} and R_{Goff}
- Percentage of tested devices not burst to total number of tested devices.

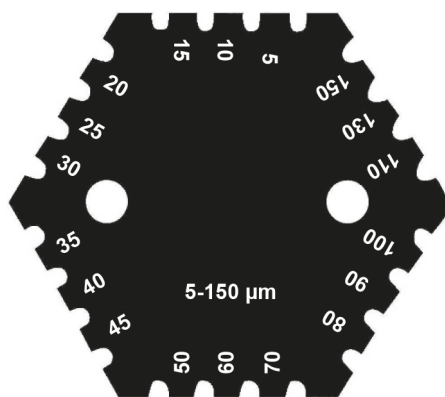
NOTE See Bibliography.

Annex B (informative)

Measuring method of the thickness of thermal compound paste

B.1 General

The measuring gauge is a comb out of stainless~~steel~~ steel or suitable plastic, which is not solvable by the fluid material of the thickness of layer to be tested. The outer teeth of the comb – those at the edges of the hexagon in Figure B.1 – form a base line. The inner teeth – those between the outer teeth – are progressively shortened, so that a space of distances is achieved between the teeth and the base line. The size of the distance can be read on a scale on the instrument. A typical measuring gauge is shown in Figure B.1.



IEC

Figure B.1 – Example of a measuring gauge for a layer of thermal compound paste of a thickness between 5 μm and 150 μm

B.2 Measuring method

Immediately after applying the layer, the measuring comb is pressed upon the substrate, so that the teeth are vertical to the surface and the measuring comb does not slip. Remove the comb and look at the teeth to ensure that is the shortest tooth that still touched the fluid layer. The thickness of the layer corresponds to the average mean value of the last touching tooth and the first non-touching tooth. At least two further measurements at different parts on the surface are to be executed in same way to get representative values for the covered area.

This method measures the thickness after grease printing. Therefore, it is very effective for the start-up inspection of the printing type grease application device. However, it is not suitable for inspection of dispenser type grease application equipment or each products warranty, so it is necessary to consider another method for those verifications.

Annex C (informative)

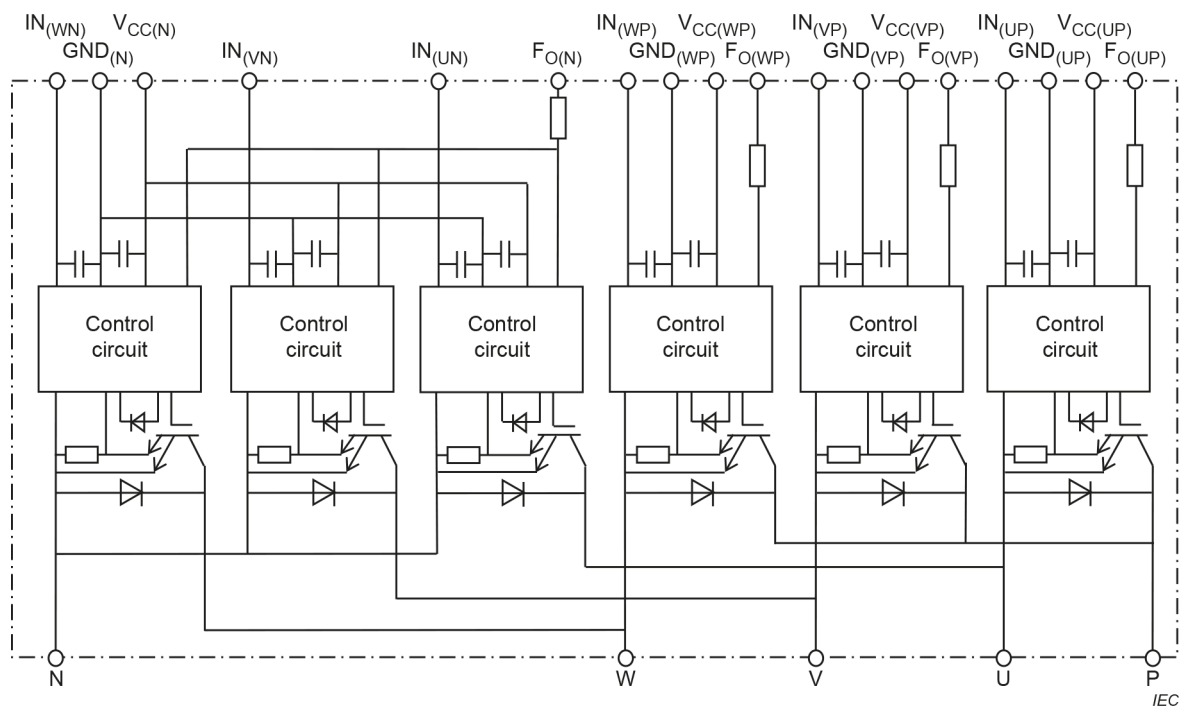
Intelligent power semiconductor modules (IPMs)

C.1 General

Isolated power semiconductor devices are categorized to several type, intelligent power semiconductor module is one of type of them. The intelligent power semiconductor modules (IPMs) include incorporated control circuits, such as gate driving circuit, protection function circuits from abnormal operation. This type of device is widely used in field, this annex shows functions of the IPM as of reference. And IGBT-IPM is used as an example in this annex. Add the descriptions for another type of IPMs if needed in the future.

C.2 Control terminals of IPM

Figure C.1 shows the internal circuit configuration block diagram of representative IPM, main terminals and control terminals.



Key

P	+DC main terminal
N	-DC main terminal
U, V, W	Output main terminals
$V_{CC(UP,VP,WP,N)}$	power supply (+) terminals for control circuits
$GND_{(UP,VP,WP,N)}$	power supply (-) terminals for control circuits / reference potential terminals
$IN_{(UP,VP,WP,UN,VN,WN)}$	input signal terminals of control circuit
$FO_{(UP,VP,WP,N)}$	alarm output terminals of control circuit

Figure C.1 – Example of internal circuit configuration block diagram of IPM

C.3 Essential ratings (limiting value) and characteristics

C.3.1 General

The ratings and characteristics of IPM regarding incorporated control circuit are described in this clause. The input signal for driving the IGBT is low active, that is, the IPM in which the IGBT is turned on when the signal level changes from High to Low is taken as an example. Figure C.1 shows an example of 6 in 1 type IPM that is widely used in the market, but from this section onwards using 2 in 1 type IPM for simplification explain.

NOTE If more than one rating or characteristic names, letter symbols are used in actual application, those are indicated by using "/" as separator.

C.3.2 Ratings (limiting value) and testing method

C.3.2.1 Supply voltage V_D / V_{CC}

Maximum voltage that can be applied between V_{CC} terminal and GND terminal under specified conditions. Both letter symbols V_D and V_{CC} may be used.

C.3.2.2 Input voltage V_{CIN} / Input signal voltage V_{in}

Maximum voltage that can be applied between IN terminal and GND terminal under specified conditions.

C.3.2.3 Fault output voltage V_{FO} / Alarm signal voltage V_{ALM}

Maximum voltage that can be applied between F_O terminal and GND terminal under specified conditions.

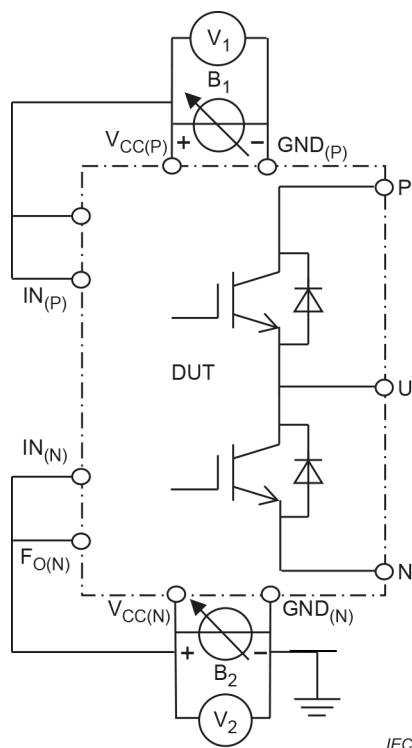
Testing method for the above three ratings is shown below.

- Purpose

To confirm that there is no abnormality when the rated voltage of the control circuit is applied to the control circuit of the DUT under the specified conditions.

- Test circuit

Testing circuit is shown in Figure C.2, as an example of 2 in1 type IPM.



Key

- DUT IPM under test
- B_1 Power supply voltage source of upper arm control circuit
- B_2 Power supply voltage source of lower arm control circuit
- V_1 Voltmeter for upper arm control circuit power supply observation
- V_2 Voltmeter for lower arm control circuit power supply observation

Figure C.2 – Testing circuit for supply voltage, input voltage / input signal voltage, and fault output voltage / alarm signal voltage

- Test procedure
 - 1) Connect the test circuit shown in Figure C.2 to the DUT.
 - 2) Set the DUT to the specified temperature by a hot plate or constant temperature chamber.
 - 3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_1 , and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_2 .
 - 4) Confirm that there are no abnormalities after the test.
- Specified conditions
 - a) Voltage of control circuit power supply B_1 , B_2 .
 - b) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

- Test procedure
 - 1) Connect the test circuit shown in Figure C.3 to the DUT.
 - 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
 - 3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2 , and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3 .
 - 4) Apply the ON-signal between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by the Variable pulse voltage source G .
 - 5) Increase the voltage of the power supply voltage source B_1 until over current protection / short circuit protection function is activated.
 - 6) When the over current protection / short circuit protection is activated, observe the current flowing to the $F_{O(N)}$ terminal with an ammeter (or current sensor with oscilloscope) and confirm that it can withstand the rated current.
 - 7) Confirm that there are no abnormalities after the test.
- Specified conditions
 - a) Collector current of over current protection / short circuit trip level;
 - b) Specified current I_{FO} or I_{ALM} to $F_{O(N)}$ terminal (adjustable by B_3 voltage);
 - c) Voltage of control circuit power supply B_2 , B_3 ;
 - d) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
 - e) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

C.3.2.5 Main circuit DC bus voltage at short circuit V_{SC}

Maximum DC bus voltage of the main circuit (voltage between the P terminal and the N terminal of the IPM) that can perform protective operation in the event of a short circuit when the specified test set temperature and specified control voltage are applied.

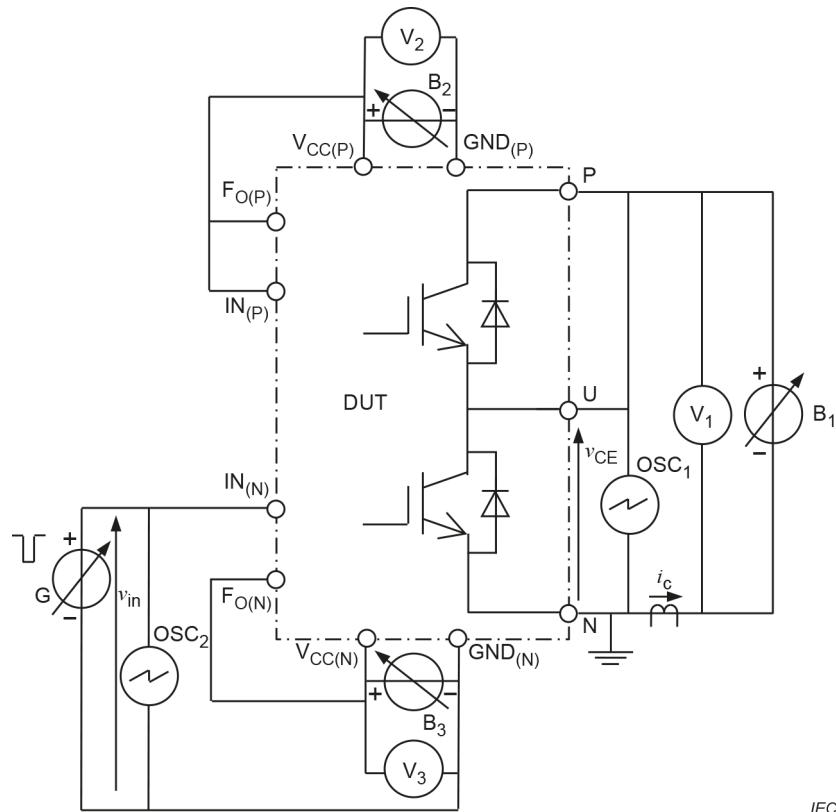
If a short circuit occurs at a voltage exceeding this value, protection cannot be performed, and the device may be destroyed.

Testing method is shown below.

- Purpose

To confirm that the DUT is protected by the protection function in the event a short circuit and can withstand the short circuit protection operation under the specified conditions.
- Test circuit

Testing circuit is shown in Figure C.4, and the waveforms are shown in Figure C.5.



IEC

Key

DUT	IPM under test
B ₁	Power supply voltage source for collector current
B ₂	Power supply voltage source of upper arm control circuit
B ₃	Power supply voltage source of lower arm control circuit
V ₁	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V ₂	Voltmeter for upper arm control circuit power supply observation
V ₃	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
OSC ₁	Oscilloscope for voltage v _{CE} between collector and emitter observation
OSC ₂	Oscilloscope for voltage v _{in} between IN _(N) and GND _(N) observation

Figure C.4 – Testing circuit for main circuit DC bus voltage at short circuit

– Test procedure

- 1) Connect the test circuit shown in Figure C.4 to the DUT.
- 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
- 3) Apply the specified voltage between the V_{CC(P)} terminal and the GND_(P) terminal by the power supply voltage source B₂, and between the V_{CC(N)} terminal and the GND_(N) by the power supply voltage source B₃. Also, apply the specified voltage between the P terminal and the N terminal by the power supply voltage source B₁.
- 4) Apply the ON-signal (longer enough to activate short circuit protection, usually 10 μs or more) between the IN_(N) terminal and the GND_(N) terminal by the Variable pulse voltage source G.
- 5) Confirm that there are no destruction or abnormalities after the short circuit test.

- Specified conditions
 - a) Voltage of control circuit power supply B_2, B_3 ;
 - b) Specified main DC bus voltage (between P and N terminal by voltage source B_1);
 - c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
 - d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

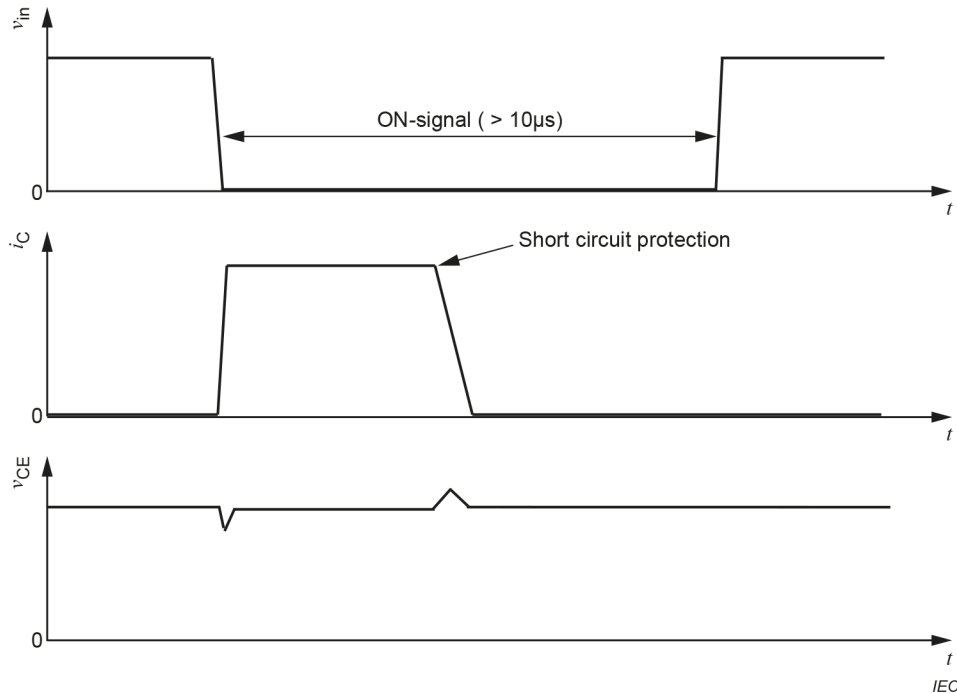


Figure C.5 – Waveforms of short circuit protection function

C.3.2.6 Acceptance defining criteria

All rating tests should be verified to be normal by measuring the characteristics of the IPM control circuit shown in Table C.1 after the tests are completed. The normal characteristic value is not higher than the upper limit USL of the acceptance criteria and is not lower than the lower limit LSL.

Table C.1 – Acceptance defining criteria for the IPM control circuit after rating tests

Subclause	Acceptance defining characteristics	Acceptance criteria
C.3.3.5	Short circuit trip level SC / Over current protection level I_{OC}	$SC / I_{OC} > LSL$
C.3.3.8	Control circuit under-voltage protection UV / V_{UV}	$LSL < UV / V_{UV} < USL$
C.3.3.3	Control circuit current $I_D / I_{CCP}, I_{CCN}$	$I_D / I_{CCP}, I_{CCN} < USL$
USL: upper specified limit. LSL: lower specified limit.		

C.3.3 Characteristics and measuring method

C.3.3.1 Turn-off times and turn-off switching energy at inductive load

Turn-off times and turn-off switching energy of IPM are defined with starting from the time when the input threshold voltage reached, under the specified measurement set temperature and specified control circuit conditions.

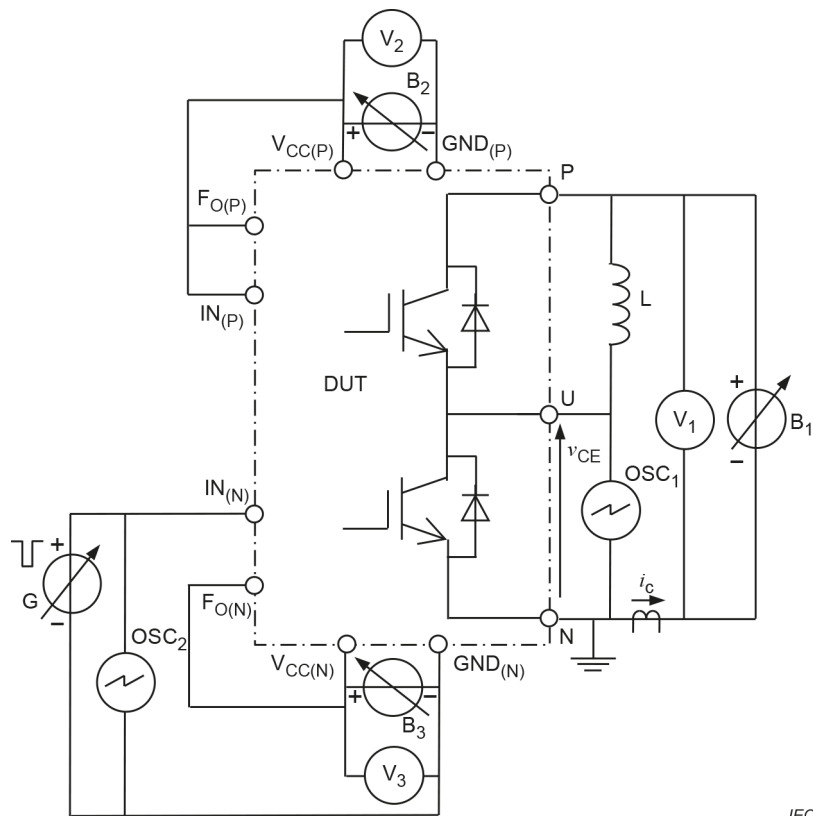
Measurement method is shown below.

– Purpose

To measure the turn-off switching times and turn-off switching energy when an inductive load current is passed through the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.6, and the waveforms are shown on left side of Figure C.7.

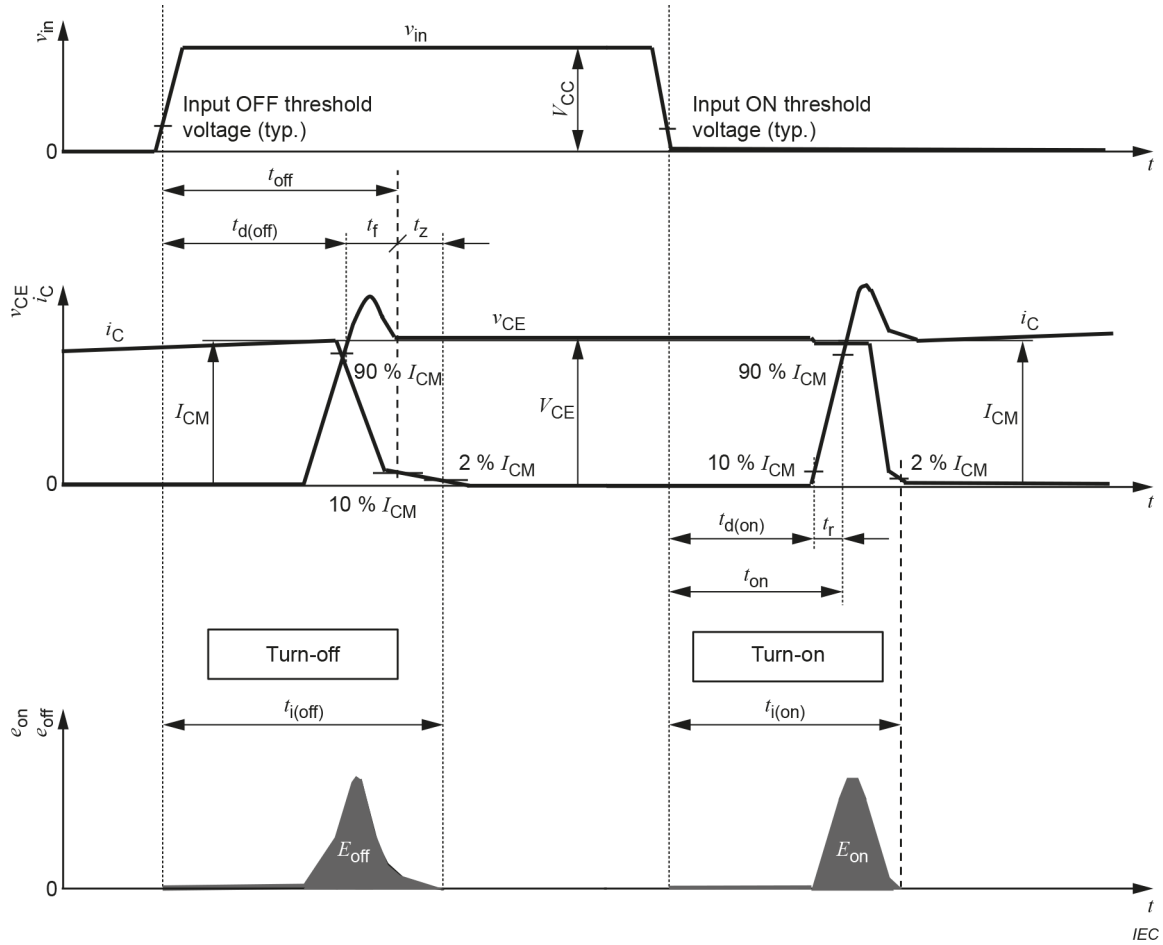


IEC

Key

DUT	IPM under test
B ₁	Power supply voltage source for collector current
B ₂	Power supply voltage source of upper arm control circuit
B ₃	Power supply voltage source of lower arm control circuit
V ₁	Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
V ₂	Voltmeter for upper arm control circuit power supply observation
V ₃	Voltmeter for lower arm control circuit power supply observation
G	Variable pulse voltage source
L	Load inductor
OSC ₁	Oscilloscope for voltage between collector and emitter observation
OSC ₂	Oscilloscope for voltage between IN _(N) and GND _(N) observation

Figure C.6 – Measurement circuit for switching times and switching energy at inductive load (lower arm device measurement)



Key

$t_{d(off)}$	Turn-off delay time	$t_{d(on)}$	Turn-on delay time
t_f	Fall time	t_r	Rise time
t_z	Tail time	t_{off}	Turn-off time
E_{off}	Turn-off energy	t_{on}	Turn-on time
$t_{i(off)}$	Integral time for turn-off energy	E_{on}	Turn-on energy
		$t_{i(on)}$	Integral time for turn-on energy

Figure C.7 – Switching waveforms at inductive load

– Measurement procedure

- 1) Connect the test circuit shown in Figure C.6 to the DUT.
- 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
- 3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2 , and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3 .
- 4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G in order to turn on the IGBT of DUT for the specified period. Adjust the voltage of the variable constant voltage power supply B_1 to raise the collector current flowing through the load inductor L to the specified current. Then, turn off the IGBT to observe the waveforms of the $IN_{(N)}$ terminal and $GND_{(N)}$ terminal voltage v_{in} , collector-emitter voltage v_{CE} , and collector current i_C with the oscilloscope and current sensor.

- 5) From the observed waveform, find the switching times at turn-on ($t_{d(off)}$, t_f , t_z , t_{off}) shown in Figure C.7, and calculate turn-on switching energy E_{off} which is integrated the product of the collector-emitter voltage v_{CE} and the collector current i_C over the integral time $t_{i(off)}$.
- Specified conditions
 - a) Collector current I_{CM} ;
 - b) Voltage of control circuit power supply B_2 , B_3 ;
 - c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
 - d) Specified main DC bus voltage (between P and N terminal by voltage source B_1);
 - e) Inductance value of the load inductor L ;
 - f) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

C.3.3.2 Turn-on times and turn-on switching energy at inductive load

Turn-on times and turn-on switching energy of IPM are defined with starting from the time when the input threshold voltage reached, under the specified measurement set temperature and specified control circuit conditions.

Measurement method is shown below.

- Purpose

To measure the turn-on switching times and turn-on switching energy when an induced load current is passed through the DUT under the specified conditions.
- Measurement circuit

Measurement circuit is shown in Figure C.7, and the waveforms are shown on right side of Figure C.7.
- Measurement procedure
 - 1) Connect the test circuit shown in Figure C.6 to the DUT.
 - 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
 - 3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2 , and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3 .
 - 4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G in order to turn on the IGBT of DUT for the specified period. Adjust the voltage of the variable constant voltage power supply B_1 to raise the collector current flowing through the load inductor L to the specified current. Turn off the IGBT once and circulate the current through the load inductor L and the freewheeling diode on the opposite arm. Then, turn on the IGBT again by applying second ON-signal pulse in order to observe the waveforms of the $IN_{(N)}$ terminal and $GND_{(N)}$ terminal voltage v_{in} , collector-emitter voltage v_{CE} , and collector current i_C with the oscilloscope and current sensor.
 - 5) From the observed waveform, find the switching times at turn-on ($t_{d(on)}$, t_r , t_{on}) shown in Figure C.7, and calculate turn-on switching energy E_{on} which is integrated the product of the collector-emitter voltage and the collector current i_C over the integral time $t_{i(on)}$.

NOTE By measuring the voltage and current waveforms of the opposite (upper) arm at the time of inductive load turn-on, the reverse recovery time, reverse recovery loss energy, and reverse recovery charge of the freewheeling diode can be measured.

- Specified conditions
 - a) Collector current I_{CM} ;
 - b) Voltage of control circuit power supply B_2 , B_3 ;
 - c) Specified input signal (double pulse) between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
 - d) Specified main DC bus voltage (between P and N terminal by voltage source B_1);
 - e) Inductance value of the load inductor L;
 - f) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

C.3.3.3 Control circuit current of upper arm I_D / I_{CCP} , and control circuit current of lower arm I_D / I_{CCN}

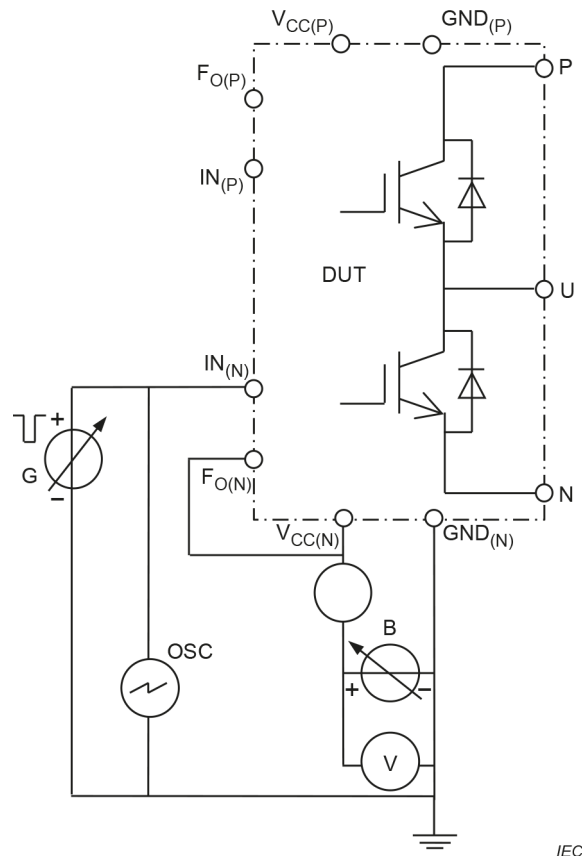
The maximum value of the effective current consumed by the control circuit of the IPM in the specified measurement set temperature, the specified control circuit conditions, and the input signal is off or the drive signal to the IGBT is input at the specified frequency.

Measurement method as example of lower arm is shown below.

- Purpose

To measure the control circuit current of the DUT under the specified conditions.
- Measurement circuit

Measurement circuit is shown in Figure C.8.



IEC

Key

- DUT IPM under test
- G Variable pulse voltage source
- B Power supply voltage source of lower arm control circuit
- OSC Oscilloscope for voltage between $IN_{(N)}$ and $GND_{(N)}$ observation
- V Voltmeter for lower arm control circuit power supply observation
- A Ammeter for lower arm control circuit power supply observation

Figure C.8 – Measurement circuit for control circuit current

- Measurement procedure
 - 1) Connect the test circuit shown in Figure C.8 to the DUT.
 - 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
 - 3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal by the power supply voltage source B, and apply the input signal between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G.
 - 4) Measure the control circuit current by ammeter A.
- Specified conditions
 - a) Voltage of control circuit power supply B;
 - b) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
 - c) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

C.3.3.4 Input ON threshold voltage $V_{th(on)}$ / $V_{inth(on)}$, and input OFF threshold voltage $V_{th(off)}$ / $V_{inth(off)}$

Maximum, minimum and typical values of the input ON / OFF threshold voltage to the control circuit for outputting the ON / OFF signal to the IGBT under the specified measurement set temperature and specified control circuit conditions.

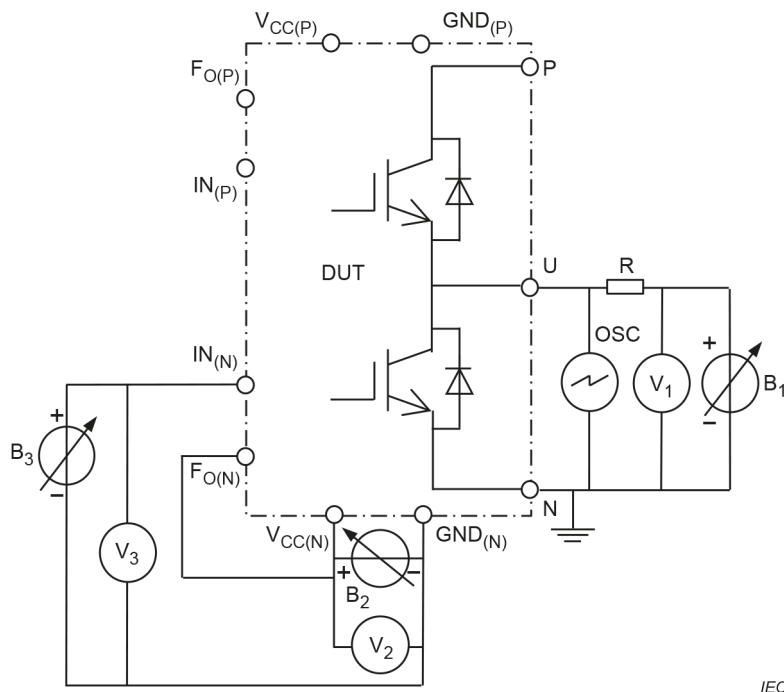
Measurement method as example of lower arm is shown below.

– Purpose

To measure the input ON threshold voltage and input OFF threshold voltage of the DUT under the specified conditions.

– Measurement circuit

Measurement circuit is shown in Figure C.9.



IEC

Key

- DUT IPM under test
- B_1 Power supply voltage source for collector current
- B_2 Power supply voltage source of lower arm control circuit
- B_3 Voltage source between $IN_{(N)}$ and $GND_{(N)}$
- V_1 Voltmeter for main DC bus voltage (between P terminal and N terminal) observation
- V_2 Voltmeter for lower arm control circuit power supply observation
- V_3 Voltmeter for lower arm input signal observation
- R Current limiting resistor
- OSC Oscilloscope for voltage between collector and emitter observation

Figure C.9 – Measurement circuit for input threshold voltage

- Measurement procedure for input ON threshold voltage
 - 1) Connect the test circuit shown in Figure C.9 to the DUT.
 - 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
 - 3) Apply the specified voltage between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ terminal by the power supply voltage source B_2 .
 - 4) Decrease voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal gradually, then, measure the voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by voltmeter V_3 when collector-emitter voltage go down to specified value.
- Measurement procedure for input OFF threshold voltage

After measurement of input ON threshold voltage, increase voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal gradually, then, measure the voltage of B_3 between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal by voltmeter V_3 when collector-emitter voltage go up to voltage of B_1 .
- Specified conditions
 - a) Voltage of B_1 for collector current supplying;
 - b) Voltage of control circuit power supply B_2 ;
 - c) Specified input signal between $IN_{(N)}$ terminal and $GND_{(N)}$ terminal;
 - d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

C.3.3.5 Over current protection level I_{OC} / Short circuit trip level SC

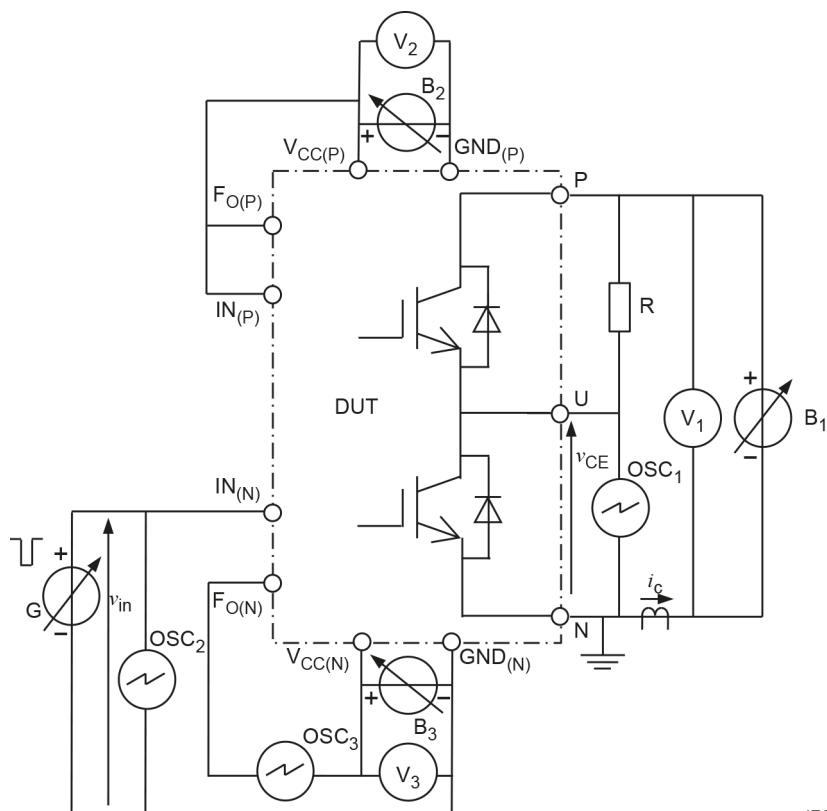
Minimum trip level for over current protection or short-circuit protection under the specified measurement set temperature and specified control circuit conditions.

Measuring method as example of lower arm is shown below.

- Purpose

To measure the over current protection level / short circuit trip level of the DUT under the specified conditions.
- Measurement circuit

Measuring circuit is shown in Figure C.10, and waveforms during the protection operation are shown in Figure C.11.



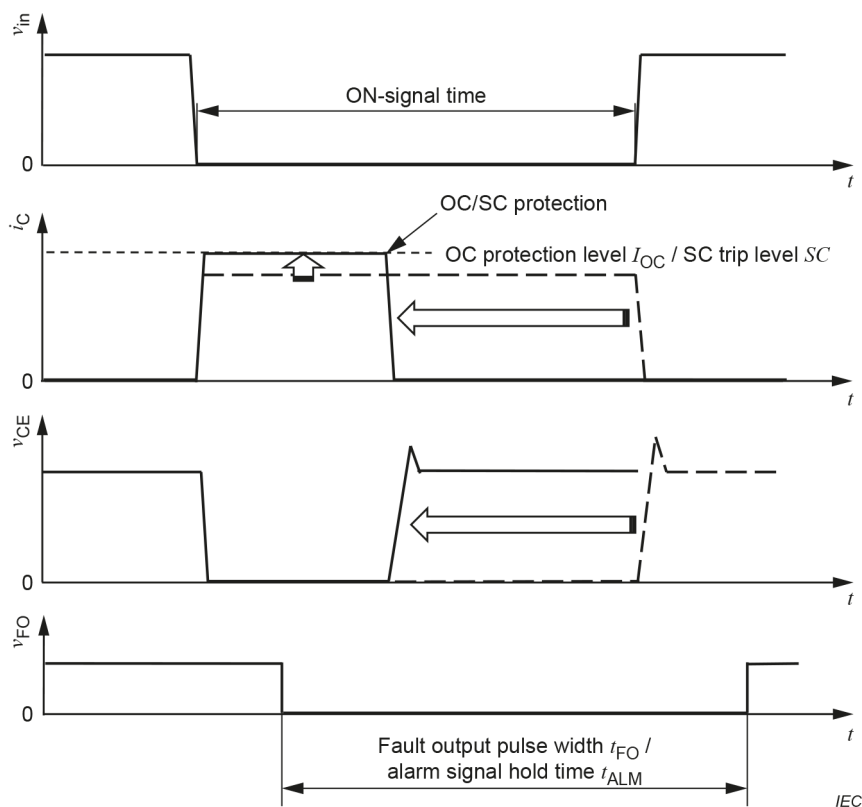
IEC

Key

- | | |
|------------------|---|
| DUT | IPM under test |
| B ₁ | Power supply voltage source for collector current |
| B ₂ | Power supply voltage source of upper arm control circuit |
| B ₃ | Power supply voltage source of lower arm control circuit |
| V ₁ | Voltmeter for main DC bus voltage (between P terminal and N terminal) observation |
| V ₂ | Voltmeter for upper arm control circuit power supply observation |
| V ₃ | Voltmeter for lower arm control circuit power supply observation |
| G | Variable pulse voltage source |
| R | Load resistor |
| OSC ₁ | Oscilloscope for voltage between collector and emitter observation |
| OSC ₂ | Oscilloscope for voltage between IN _(N) and GND _(N) observation |
| OSC ₃ | Oscilloscope for Fault / Alarm output signal observation |

Figure C.10 – Measuring circuit for over current protection level/short circuit trip level

- Measurement procedure for input ON threshold voltage
 - 1) Connect the test circuit shown in Figure C.10 to the DUT.
 - 2) Set the DUT to the specified temperature on a hot plate or constant temperature chamber.
 - 3) Apply the specified voltage between the $V_{CC(P)}$ terminal and the $GND_{(P)}$ terminal by the power supply voltage source B_2 , and between the $V_{CC(N)}$ terminal and the $GND_{(N)}$ by the power supply voltage source B_3 .
 - 4) Apply the ON-signal (the pulse voltage) between the $IN_{(N)}$ terminal and the $GND_{(N)}$ terminal with the variable pulse power supply G , and increase gradually the voltage of the variable constant voltage power supply B_1 to raise the collector current until the protection function operation.
 - 5) Then, measure the collector current just before protection operation, fault output pulse width or alarm time, and fault or alarm output signal v_{FO} simultaneously.
- Specified conditions
 - a) Voltage of control circuit power supply B_2 , B_3 ;
 - b) Input ON-signal (longer enough than $t_{dOC} / t_{off(SC)}$);
 - c) Voltage of B_1 for collector current supplying ($< V_{SC}$) with adjusting R_O ;
 - d) Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .



NOTE The fault or alarm output signal can be measured by current I_{FO} observation like Figure C.3 or current sensor with oscilloscope instead of voltage v_{FO} observation. In that case, the i_{FO} waveform is inverse shape of v_{FO} .

Figure C.11 – Waveforms during over current protection / short circuit protection

C.3.3.6 Over current protection delay time t_{doc} / Short circuit current delay time $t_{\text{off(SC)}}$

Typical value of collector turn-off delay time during over current protection or short circuit protection operation under the specified measurement set temperature and specified control circuit conditions.

Measurement method as example of lower arm is shown below.

- Purpose

To measure the over current protection delay time t_{doc} / short circuit current delay time $t_{\text{off(SC)}}$ of the DUT under the specified conditions.

- Measurement circuit

Measurement circuit is shown in Figure C.12, and waveforms during the protection operation are shown in Figure C.13.