

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors**

**Dispositifs à semiconducteurs – Dispositifs discrets –
Partie 8: Transistors à effet de champ**



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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

PRICE CODE
CODE PRIX

XC

ICS 31.080.30

ISBN 978-2-88912-279-0

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**SEMICONDUCTOR DEVICES –
DISCRETE DEVICES –****Part 8: Field-effect transistors**

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International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition of IEC 60747-8 cancels and replaces the second edition published in 2000. This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

- a) "Clause 3 Classification" was moved and added to Clause 1.
- b) "Clause 4 Terminology and letter symbols" was divided into "Clause 3 Terms and definitions" and "Clause 4 Letter symbols" was amended with additions and deletions.
- c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/398/FDIS	47E/406/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

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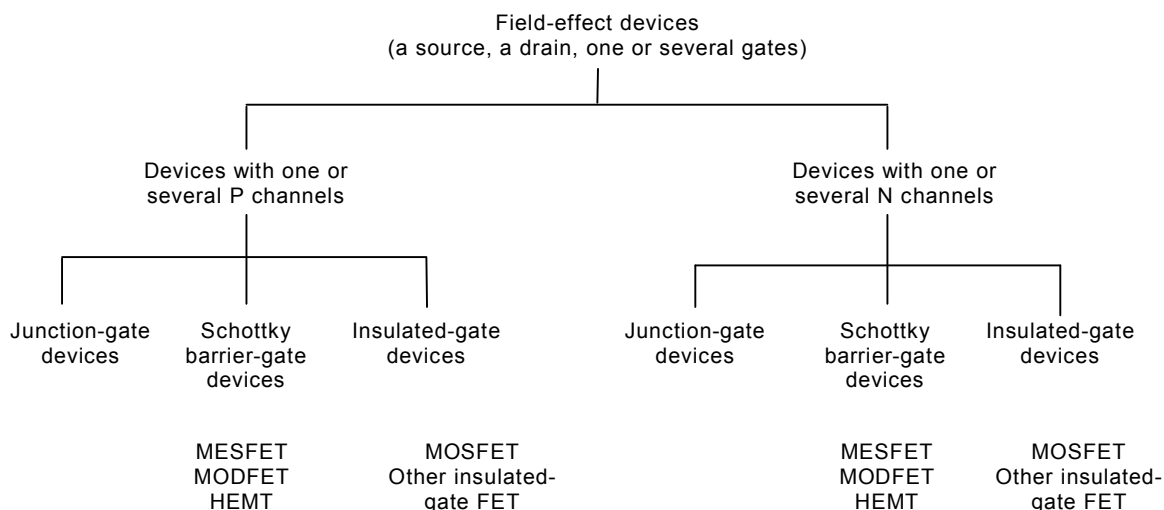
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion (normally on) type;
- type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1 Types of field-effect transistors

3.1.1

N-channel field-effect transistor

field-effect transistor that has one or more N-type conduction channels

3.1.2

P-channel field-effect transistor

field-effect transistor that has one or more P-type conduction channels

3.1.3

junction-gate field-effect transistor

JFET

field-effect transistor in which

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction

NOTE The gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel.

3.1.4

insulated-gate field-effect transistor

IGFET

field-effect transistor in which

- one or more gate electrodes are electrically insulated from the body;
- the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;
- the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions

NOTE The inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material. The conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

3.1.5

metal-oxide-semiconductor field-effect transistor

MOSFET

insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

3.1.6

depletion-type (normally on) field-effect transistor

field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage

3.1.7

enhancement-type (normally off) field-effect transistor

field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode

3.1.8

single-gate field-effect transistor

field-effect transistor having a gate region, a source region, and a drain region

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

3.1.9

dual-gate field-effect transistor

field-effect transistor having two independent gate regions, a source region, and a drain region

3.1.10

schottky-barrier-gate field-effect transistor

field-effect transistor in which

- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- one or more gate electrodes each form a Schottky-barrier with the channel region;

the gate-source voltage controls the conductance of the conduction channel by varying its cross-section

3.1.11

metal-semiconductor field-effect transistor

MESFET

Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

3.1.12

modulation-doped field-effect transistor or high electron mobility transistor MODFET or HEMT

metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance

NOTE MODFET and HEMT should be used interchangeably.

3.2 General terms

3.2.1 Physical regions (of a field-effect transistor)

3.2.1.1

source (of a field-effect transistor)

physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

3.2.1.2**drain (of a field-effect transistor)**

physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

3.2.1.3**gate (of an IGFET)**

insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

3.2.1.4**gate (of an JFET)**

region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

3.2.1.5**channel (of a depletion-type IGFET)**

inversion layer technologically placed below the gate region

3.2.1.6**channel (of a JFET)**

region between source region and drain region that has the same conductivity type as these two regions

3.2.1.7**subchannel (of an IGFET)**

region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones

3.2.1.8**substrate (of a JFET or IGFET)**

part of the original material that remains unchanged when the device elements are formed upon or within the original material

NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

3.2.1.9**substrate (of a JFET or IGFET)**

original semiconductor material before being processed

NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the "original substrate" and the "remaining substrate".

3.2.1.10**substrate (of a thin-film field-effect transistor)**

insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

3.2.2 Functional regions**3.2.2.1****functional source region**

supply region that delivers principal-current charge carriers into the channel

3.2.2.2**functional drain region**

collection region that acquires principal-current charge carriers from the channel

3.2.2.3

channel (of a IGFET)

functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.4

channel (of a JFET)

functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

3.2.2.5

subchannel space-charge region (of an IGFET)

space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

3.2.2.6

functional subchannel region

remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region

3.3 Terms related to ratings and characteristics

3.3.1

gate cut-off current (of a junction-gate field-effect transistor)

current flowing in the gate terminal of a junction field-effect transistor when the pn junction is biased in the reverse direction

3.3.2

gate leakage current (of an insulated-gate field-effect transistor)

leakage current through the insulated-gate of an insulated-gate field-effect transistor

3.3.3

capacitances

3.3.3.1

(short-circuit) input capacitance

capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

3.3.3.2

(short-circuit) output capacitance

capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

3.3.3.3

reverse transfer capacitance

capacitance between the drain and gate terminals excluding parallel capacitances between drain and source, and gate and source

3.3.4

gate-source resistance

d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

3.3.5

drain-source on-state resistance

d.c. resistance between the drain and source terminals when the FET is in its on-state

3.3.6**gate charge**

charge required to raise the gate-source voltage from zero to a specified value

3.3.6.1**total gate charge**

charge that is required to raise the gate-source voltage from zero to a specified value and calculated by the equation below (see Figure 1)

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t) dt$$

3.3.6.2**threshold gate charge**

charge required to raise gate-source from zero to $V_{GS(th)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(th)} = \int_{t_0}^{t_1} i_{GG}(t) dt$$

3.3.6.3**plateau gate charge**

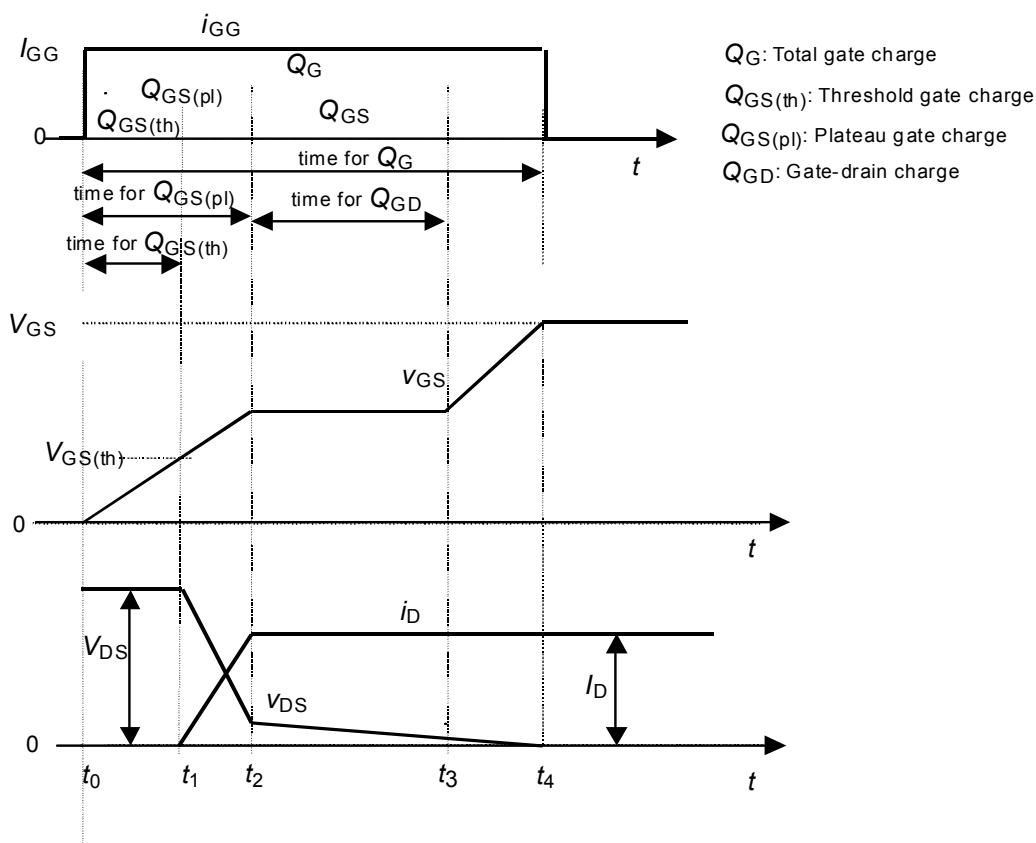
charge required to raise gate-source voltage from zero to plateau voltage $V_{GS(pl)}$ and calculated by the equation below (see Figure 1)

$$Q_{GS(pl)} = \int_{t_0}^{t_2} i_{GG}(t) dt$$

3.3.6.4**gate drain charge**

charge difference between beginning and end of plateau region, required to charge up C_{GD} and calculated by the equation below (see Figure 1)

$$Q_{GD} = \int_{t_2}^{t_3} i_{GG}(t) dt$$



IEC 2736/10

NOTE Time intervals indicated by arrow end lines are integral intervals to calculate the gate charges.

Figure 1 – Basic waveforms to specify the gate charges

3.3.7

overall efficiency

ratio of the output power to the sum of the input signal power and the d.c. input power

$$\eta_{tot} = \frac{P_{out}}{P_{in} + P_{(d.c.)}}$$

3.3.8

drain efficiency

ratio of the output power to the d.c. drain power

$$\eta_d = \frac{P_{out}}{P_{d(d.c.)}}$$

3.3.9

power-added efficiency

ratio of the difference between the output power and the input signal power to the d.c. input power

$$\eta_{\text{add}} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{d(d.c.)}}}$$

3.3.10**rate of rise of off-state voltage**

rate of rise of drain-source off-state voltage induced during reverse recovery period of the inverse diode

3.3.11**reverse-bias safe operating area**

drain current versus drain-source voltage region in which the MOSFET is able to turned-off repetitively with clamped inductive load without failure

3.3.12**short circuit safe operating area**

drain current versus drain voltage region in which the MOSFET is able to turn on and off non repetitively without failure

3.3.13**avalanche energy (for avalanche devices)**

avalanche energy capability during turn-off period

3.3.14**repetitive avalanche energy (for avalanche devices)**

repetitive avalanche energy capability during turn-off period

3.3.15**non-repetitive avalanche energy (for avalanche devices)**

non-repetitive avalanche capability during turn-off period (single pulse)

3.3.16**drain leakage current**

drain current in the off-state

3.3.17**breakdown voltage, drain to source**

drain-source breakdown voltage in the off-state

3.3.18**internal gate resistance**

short-circuit internal gate resistance (see Figure 32)

3.3.19**switching times**

input wave form is the gate to source voltage, and output waveform is the drain current (see IEC 60747-1:2006)

3.3.20**turn-on energy**

value of the integral of the product of drain-source voltage V_{DS} and drain current I_{D} during turn-on described in the following equation: $E_{\text{on}} = \int_0^{t_1} i_{\text{D}} \times v_{\text{DS}} \times dt$ (see Figure 2)

3.3.21

turn-off energy

value of the integral of drain-source voltage V_{DS} multiplied by drain current I_D during turn-off described in the following equation: $E_{off} = \int_{t_2}^{t_3} i_D \times V_{DS} \times dt$ (see Figure 2)

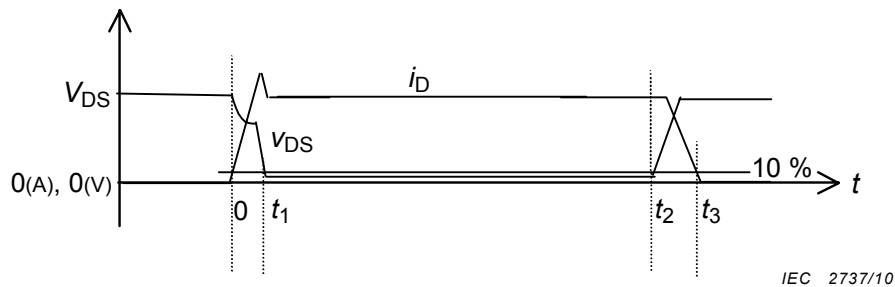


Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}

3.3.22

output capacitance charge

charge required to change the voltage at output capacitance C_{oss} during turn-on and turn-off

3.3.23

gate-source plateau voltage

voltage during turn-on, where V_{GS} is relatively constant (Miller-Plateau) and during which C_{GD} is charged

NOTE See Figure 1.

3.3.24

drain-source reverse voltage

voltage across the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.25

MOSFET forward recovery current

recovery current of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.26

MOSFET forward recovery time

recovery time of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.27

MOSFET forward recovery charge

recovery charge of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.3.28

MOSFET forward recovery energy

recovery energy of the MOSFET which results from the flow of current in the reverse direction from source to drain

3.4 Conventional used terms

Table 1 – Terms for MOSFET in this standard and the conventional used terms for the inverse diode integrated in the MOSFET

Preferred terms	Letter symbol	Deprecated terms for inverse diode with MOSFET in off-state
Drain-source reverse voltage	V_{DSR}	Inverse diode forward voltage
MOSFET forward recovery current	I_{FR}	Inverse diode reverse recovery current
MOSFET peak forward recovery current	I_{FRM}	Inverse diode peak reverse recovery current
MOSFET forward recovery time	t_{fr}	Inverse diode reverse recovery time
MOSFET forward recovery charge	Q_f	Inverse diode reverse recovery charge
MOSFET forward recovery energy	E_{fr}	Inverse diode reverse recovery energy
Reverse drain current	I_{DR}	Inverse diode forward current
Peak reverse drain current	I_{DRM}	Inverse diode peak forward current

4 Letter symbols

4.1 General

General letter symbols for MOSFETs are defined in Subclauses 4.4 and 4.5 of IEC 60747-1:2006.

4.2 Additional general subscripts

In addition to the list of recommended general subscripts given in 4.2.3 of IEC 60747-1:2006, the following special subscripts are recommended for field-effect transistors:

D, d	= drain
G, g	= gate
S, s	= source or termination with a short circuit
B, b; U, u	= substrate
T; th; (TO)	= threshold
O	= termination with an open circuit
R	= termination with a resistor
X	= termination with specified gate source voltage
pl	= plateau

4.3 List of letter symbols

Name and designation	Letter symbol	Remarks
4.3.1 Voltage		
Drain-source (d.c.) voltage	V_{DS}	
Gate-source (d.c.) voltage	V_{GS}	
Gate-source cut-off voltage (of a junction field-effect transistor and of a depletion type insulated-gate field-effect transistor)	$V_{GS(OFF)}$; V_{GSoff}	
Gate-source threshold voltage (of an enhancement type insulated-gate field-effect transistor)	V_{GST} ; $V_{GS(th)}$; $V_{GS(TO)}$	
Forward gate-source (d.c.) voltage	V_{GSF}	

Name and designation	Letter symbol	Remarks
Reverse gate-source (d.c.) voltage	V_{GSR}	
Gate-drain (d.c.) voltage	V_{GD}	
Source-substrate (d.c.) voltage	$V_{\text{SB}}; V_{\text{SU}}$	
Drain-substrate (d.c.) voltage	$V_{\text{DB}}; V_{\text{DU}}$	
Gate-substrate (d.c.) voltage	$V_{\text{GB}}; V_{\text{GU}}$	
Gate-gate voltage (for multi-gate devices)	$V_{\text{G1} - \text{G2}}$	
Gate-source breakdown voltage with drain short-circuited to source	$V_{(\text{BR})\text{GSS}}$	
Breakdown voltage, drain-source (for type B)	$V_{(\text{BR})\text{DSX}}$	
Breakdown voltage, drain-source (for type C)	$V_{(\text{BR})\text{DSS}}$	
Drain-source on-state voltage	$V_{\text{DS}(\text{on})}$	
Drain-source reverse voltage	V_{DR}	
Gate-source plateau voltage	$V_{\text{GS}(\text{pl})}$	
4.3.2 Currents		
Drain (d.c.) current	I_{D}	
Peak drain current	I_{DM}	
Peak reverse drain current	I_{DRM}	
Drain current, at a specified gate-source condition	I_{DSX}	
Drain current, at a specified external gate-source resistance	I_{DSR}	
Drain current, with gate short-circuited to source ($V_{\text{GS}} = 0$)	I_{DSS}	
Source (d.c.) current	I_{S}	
Source current, at a specified gate-drain condition	I_{SDX}	
Source current, with gate short-circuited to drain ($V_{\text{GD}} = 0$)	I_{SDS}	
Gate (d.c.) current	I_{G}	
Forward gate current	I_{GF}	
Gate cut-off current (of a junction field-effect transistor), with source open-circuited	I_{GDO}	
Gate-cut-off current (of a junction field-effect transistor), with drain open-circuited	I_{GSO}	
Gate cut-off current (of a junction field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate leakage current (of an insulated-gate field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate cut-off current (of a junction field-effect transistor), with specified drain-source circuit conditions	I_{GSX}	
Substrate current	$I_{\text{B}}; I_{\text{U}}$	
4.3.3 Power dissipation		
Total power dissipation	P_{tot}	
4.3.4 Small-signal parameters		
Drain-source resistance	r_{ds}	
Gate-source resistance	r_{gs}	

Name and designation	Letter symbol	Remarks
Gate-drain resistance	r_{gd}	
Gate resistance (with $V_{DS} = 0$ or $v_{ds} = 0$)	r_{gss}	
Drain-source on-state resistance	$r_{ds(on)}$	
Drain-source off-state resistance	$r_{ds(off)}$	
Internal gate resistance	R_g	
Open-circuit gate-source capacitance (drain-source and gate-drain open-circuited to a.c.)	C_{gso}	
Open-circuit gate-drain capacitance (drain-source and gate-source open-circuited to a.c.)	C_{gdo}	
Open-circuit drain-source capacitance (gate-drain and gate-source open-circuited to a.c.)	C_{dso}	
Short-circuit input capacitance in common-source configuration; gate-source capacitance (drain-source short-circuited to a.c.)	$C_{iss}; C_{11ss}$	
Short-circuit output capacitance in common-source configuration; drain-source capacitance (gate-source short-circuited to a.c.)	$C_{oss}; C_{22ss}$	
Common-source reverse transfer capacitance with input short-circuited to a.c.	$C_{rss}; C_{12ss}$	
Short-circuit output capacitance in common-drain configuration (gate-drain short-circuited to a.c.)	$C_{ods}; C_{22ds}$	
Gate-source capacitance (in the π equivalent circuit)	C_{gs}	
Gate-drain capacitance (in the π equivalent circuit)	C_{gd}	
Drain-source capacitance (in the π equivalent circuit)	C_{ds}	
Short-circuit input conductance in common-source configuration	G_{iss}	
Short-circuit output conductance in common-source configuration	G_{oss}	
Gate-source conductance (in the π equivalent circuit)	G_{gs}	
Gate-drain conductance (in the π equivalent circuit)	G_{gd}	
Drain-source conductance (in the π equivalent circuit)	G_{ds}	
Short-circuit input admittance	$y_{is} = \text{Re}(y_{is}) + j\omega C_{is}$ $y_{11s} = \text{Re}(y_{11s}) + j\omega C_{11s}$	
Short-circuit reverse transfer admittance	$y_{rs} = \text{Re}(y_{rs}) + j\omega C_{rs}$ $y_{12s} = \text{Re}(y_{12s}) + j\omega C_{12s}$	
Short-circuit forward transfer admittance	$y_{fs} = \text{Re}(y_{fs}) + j\text{Im}y_{fs}$ $y_{21s} = \text{Re}(y_{21s}) + j\text{Im}y_{21s}$	
Short-circuit output admittance	$y_{os} = \text{Re}(y_{os}) + j\omega C_{os}$ $y_{22s} = \text{Re}(y_{22s}) + j\omega C_{22s}$	
Modulus of the short-circuit reverse transfer admittance	$ y_{rs} ; y_{12s} $	
Phase of the short-circuit reverse transfer admittance	$\varphi_{ys}; \varphi_{y12s}$	
Modulus of the short-circuit forward transfer admittance	$ y_{fs} ; y_{21s} $	
Phase of the short-circuit forward transfer admittance	$\varphi_{ys}; \varphi_{y21s}$	

Name and designation	Letter symbol	Remarks
Forward transconductance (in the π equivalent circuit)	$g_{ms}; g_m; g_{fs}$	
Input reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{11s} OR S_{is} S_{11g} OR S_{ig} S_{11d} OR S_{id}	
Output reflection coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{22s} OR S_{os} S_{22g} OR S_{og} S_{22d} OR S_{od}	
Forward transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{21s} OR S_{fs} S_{21g} OR S_{fg} S_{21d} OR S_{fd}	
Reverse transmission coefficient: – in common-source configuration – in common-gate configuration – in common-drain configuration	S_{12s} OR S_{rs} S_{12g} OR S_{rg} S_{12d} OR S_{rd}	
4.3.5 Other parameters		
Total gate charge	Q_G	
Plateau gate charge	$Q_{GS(pl)}$	
Gate-drain charge	Q_{GD}	
Threshold gate charge	$Q_{GS(th)}$	
Power gain	$G_P; G_p$	
Output power at specified input power	P_o	
Overall efficiency	η_{tot}	
Drain efficiency	η_d	
Power added efficiency	η_{add}	
Cut-off frequency (in the common-source configuration)	f_{yfs}	
Noise voltage	V_n	
Noise figure	F	
Temperature coefficient of drain current	α_{ID}	
Temperature coefficient of drain-source resistance	α_{rds}	
Turn-on delay time	$t_{d(on)}$	Switching times (see Figure 3) $t_{on} = t_{d(on)} + t_r$ $t_{off} = t_{d(off)} + t_f$
Turn-off delay time	$t_{d(off)}$	
Rise time	t_r	
Fall time	t_f	
Turn-on time	t_{on}	
Turn-off time	t_{off}	
Turn-on energy	E_{on}	
Turn-off energy	E_{off}	
Repetitive avalanche energy	E_{AR}	
Non-repetitive single pulse avalanche energy	E_{AS}	
Frequency of unity forward transmission coefficient: – in common-source configuration – in common-gate configuration	f_{ss} OR f_{iss} f_{sg} OR f_{isg}	$f_{ss} = f$ for $ S_{21s} = 1$ $f_{sg} = f$ for $ S_{21g} = 1$

Name and designation	Letter symbol	Remarks
– in common-drain configuration	f_{sd} or f_{isd}	$f_{sd} = f$ for $ s_{21d} = 1$

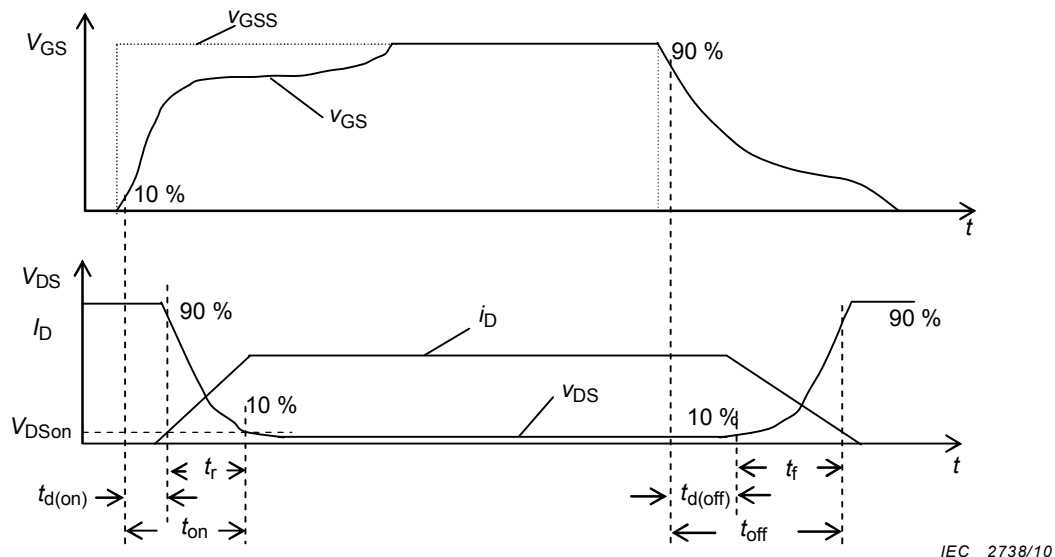


Figure 3 – Switching times

Name and designation	Letter symbol	Remarks
4.3.6 Matched-pair field-effect transistors		
Difference of gate leakage currents (for insulated-gate field-effect transistors) and difference of gate cut-off currents (for junction field-effect transistors)	$I_{G1} - I_{G2}$	The smaller value is subtracted from the larger value
Ratio of drain currents for zero gate-source voltage	I_{DSS1} / I_{DSS2}	The smaller of the two values is taken as the numerator
Difference of small-signal common-source output conductances	$g_{os1} - g_{os2}$	The smaller value is subtracted from the larger value
Ratio of small-signal common-source forward transfer conductances	g_{fs1} / g_{fs2}	The smaller of the two values is taken as the numerator
Difference of gate-source voltages	$V_{GS1} - V_{GS2}$	The smaller value is subtracted from the larger value
Change in difference of gate-source voltages between two temperatures	$ \Delta(V_{GS1} - V_{GS2}) _{\Delta T}$	
4.3.7 Inverse diodes integrated in MOSFETs		
Drain-source reverse voltage	V_{DSR}	Forward voltage of the inverse diode
MOSFET forward recovery current	I_{FR}	Reverse recovery current of the inverse diode
MOSFET peak forward recovery current	I_{FRM}	Peak reverse recovery current of the inverse diode
MOSFET forward recovery time	t_{fr}	Reverse recovery time of the inverse diode
MOSFET forward recovery charge	Q_f	Reverse recovery charge of the inverse diode
MOSFET forward recovery energy	E_{fr}	Reverse recovery energy of the inverse diode
Reverse drain current	I_{DR}	Forward current of the inverse diode

5 Essential ratings and characteristics

5.1 General

5.1.1 Device categories

Field-effect transistors are divided into three categories:

- type A: junction-gate type;
- type B: insulated-gate depletion type;
- type C: insulated-gate enhancement type.

5.1.2 Multiple-gate devices

For multiple-gate devices, the required gate ratings and characteristics shall be given for each gate separately, except where otherwise stated.

5.1.3 Handling precautions

Because of the very high input resistance of field-effect transistors, the gate insulation layer (for insulated-gate types) or the gate junction (for junction-gate types) may be irreversibly damaged if an excessive voltage is allowed to build up, e.g. due to contact with electrostatically charged persons, leakage currents from soldering irons, etc.

The requirements of IEC 60747-1:2006 Clause 8 apply to these devices.

5.2 Ratings (limiting values)

5.2.1 Temperatures

5.2.1.1 Minimum and maximum storage temperatures (T_{stg})

5.2.1.2 Virtual junction temperature (T_{vj})

Maximum rated value.

5.2.2 Power dissipation (P_{tot})

Maximum total power dissipation over the specified range of operating temperatures (ambient or case).

5.2.3 Safe operating area (SOA) for MOSFET only

Over the specified range of operating temperatures, under specified pulse conditions.

5.2.3.1 Forward-bias safe operating area (FBSOA)

Maximum safe operating area of V_{DS} and I_D in conduction state.

5.2.3.2 Reverse-bias safe operating area (RBSOA)

Maximum safe operating area of V_{DS} and I_D during turn-off state.

5.2.3.3 Short-circuit safe operating area (SCSOA)

Non-repetitive maximum safe operating area of V_{DS} and I_D during turn-off

TYPES		
A	B	C
+	+	+
+	+	+
+	+	+
	+	+
	+	+
	+	+

state from short circuit condition.

5.2.4 Voltages and currents

Ratings apply over the operating temperature range unless otherwise specified.

5.2.4.1 Maximum drain-source voltage

Under specified gate conditions.

5.2.4.2 Maximum reverse gate-source voltage and, where appropriate, maximum forward gate-source voltage

Under specified drain conditions.

5.2.4.3 Maximum gate-substrate voltage

Under specified source conditions;

For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)

5.2.4.4 Maximum drain-substrate voltage

Under specified gate to source conditions;

For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)

5.2.4.5 Maximum source-substrate voltage

Under specified gate to drain conditions.

For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types)

5.2.4.6 Maximum drain current (I_D)

5.2.4.7 Maximum peak drain current (I_{DM})

Under specified pulse conditions.

For MOSFET only.

5.2.4.8 Maximum continuous (d.c.) reverse drain current (I_{DR}) (forward current of the inverse diode)

5.2.4.9 Maximum peak reverse drain current (I_{DRM}) (Maximum peak forward current of the inverse diode)

Under specified pulse conditions.

5.2.4.10 Maximum forward gate current

5.3 Characteristics

Characteristics are to be given at 25 °C, except where otherwise stated and at (at least) one other temperature.

5.3.1 Characteristics for low-frequency amplifier

TYPES		
A	B	C
+	+	+
+	+	+
	+	+
	+	+
	+	+
+	+	+
	+	+
	+	+
+		

5.3.1.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.1.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.1.3 Drain current at zero gate-source voltage (I_{DSS})

Minimum and maximum values, for zero gate-source voltage, at a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.1.4 Drain current at specified gate-source voltage (I_{DSX})

Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.1.5 Gate-source cut-off voltage ($V_{GS(off)}$)

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.1.6 Gate-source threshold voltage ($V_{GS(th)}$)

Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.1.7 Short-circuit input capacitance (C_{iss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.

5.3.1.8 Short-circuit output conductance and, where appropriate, capacitance (g_{oss} , C_{oss})

TYPES		
A	B	C
+		
	+	+
+	+	+
+	+	
		+
+	+	
		+
+	+	+
+	+	+

	TYPES		
	A	B	C
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.			
5.3.1.9 Reverse transfer capacitance (where appropriate) (C_{rss})	+	+	+
Maximum small-signal value, in common-source configuration with input open-circuit to a.c., under specified bias conditions and at a specified low frequency.			
5.3.1.10 Forward transconductance (g_{ms}, g_m, g_{fs})	+	+	+
Minimum and maximum values under specified bias conditions and at a specified low frequency.			
5.3.1.11 For low-noise applications, noise voltage and, where appropriate, noise figure (V_n, F)	+	+	+
Maximum value, in common-source configuration, under specified conditions of bias, source resistance, center frequency and power bandwidth.			
5.3.1.12 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$ or $R_{th(j-c)}$)	+	+	+
Maximum value.			
5.3.2 Characteristics for high-frequency amplifier			
5.3.2.1 Gate cut-off current	+		
Gate leakage current		+	+
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
Together with:			
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.2 Drain cut-off current	+	+	+
Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.3 Drain current at zero gate-source voltage (I_{DSS})	+	+	
Minimum and maximum values, for zero gate-source voltage and a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.2.4 Drain current at specified gate-source voltage (I_{DSX})			+
Minimum and maximum values, for specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one			

other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.2.5 Gate-source cut-off voltage (V_{GSoff})

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.2.6 Gate-source threshold voltage ($V_{GS(th)}$)

Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.2.7 y-parameters

5.3.2.7.1 For all FETs under specified values of bias and frequency:

y_{is} – real and imaginary parts, maximum values;

y_{os} – real and imaginary parts, maximum values;

y_{fs} – real and imaginary parts, minimum and maximum values (see also 5.3.2.7.2);

y_{rs} – real and imaginary parts, maximum values.

5.3.2.7.2 For power MOSFET as alternative to y_{fs} , forward transconductance (g_{ms} , g_m , g_{fs}):

Minimum value with drain-source short circuit to a.c., for specified drain-source voltage and drain current, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.2.8 Output power at specified input power (P_o)

Minimum and typical values under specified circuit and bias conditions

or:

power gain (G_p)

Minimum and typical values under specified circuit and bias conditions

5.3.2.9 Where appropriate, overall efficiency (η_{tot})

Minimum and typical values under specified circuit and bias conditions

NOTE $\eta_{tot} = \frac{P_{out}}{P_{in} + P_{(d.c.)}}$

TYPES		
A	B	C
+	+	
		+
+	+	+
	+	+
+	+	+
+	+	+
+	+	+

5.3.2.10 Alternatively, collector efficiency (η_d)

Minimum and typical values under specified circuit and bias conditions

NOTE $\eta_d = \frac{P_{out}}{P_{d(d.c.)}}$

5.3.2.11 Power added efficiency (η_{add})

Minimum and typical values under specified circuit and bias conditions

NOTE $\eta_{add} = \frac{P_{out} - P_{in}}{P_{d(d.c.)}}$

5.3.2.12 Noise figure (F)

Maximum value, under specified conditions of bias, source impedance, centre frequency and power bandwidth. These conditions must be those which provide the lowest value of the noise figure.

5.3.2.13 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)

Maximum value.

5.3.3 Characteristics for high and low power switching and chopper**5.3.3.1 Gate cut-off current****Gate leakage current**

Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.3.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.3.3 Gate-source cut-off voltage (V_{GSoff})

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

TYPES		
A	B	C
+	+	+
+	+	+
+	+	+
	+	+
+		
	+	+
+	+	+
+	+	

5.3.3.4 Gate-source threshold voltage ($V_{GS(th)}$)

Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate-voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.3.5 On-state characteristics

5.3.3.5.1 Drain-source on-state voltage; ($V_{DS(on)}$)

Drain-source saturation voltage

Maximum value, at a specified large value of drain current and gate-source voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

or (for MOSFET only):

5.3.3.5.2 Drain-source on-state resistance ($r_{DS(on)}$)

Maximum value, at a specified large value of drain current and gate-source voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.3.5.3 Short-circuit output conductance (g_{oss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

5.3.3.6 Short-circuit input capacitance (C_{iss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.

5.3.3.7 Short-circuit output capacitance (where appropriate) (C_{oss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

5.3.3.8 Reverse transfer capacitance (where appropriate) (C_{rss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

5.3.3.9 Switching times (see Figure 3)

They are stated under the following conditions:

- common-source configuration;
- specified condition in which output loading capacitance and resistance shall be included;
- input pulse transition times, amplitude and repetition frequency to be specified;
- $V_{GS(off-state)}$ must be greater than or equal to the maximum gate-source cut-

TYPES		
A	B	C
		+
+	+	+
	+	+
+	+	+
+	+	+
+	+	+
+	+	+
+	+	+

	TYPES		
	A	B	C
off voltage for type A and B devices, or lower than the minimum gate-source threshold voltage for type C devices;			
e) $V_{GS(on-state)}$ must correspond to a high drain current;			
f) Maximum values of: $t_{d(on)}$, t_r , $t_{d(off)}$ and t_f separately.			
NOTE Where $t_{d(off)}$ is only a small fraction of the total turn-off time (t_{off}), a maximum value for t_{off} alone is adequate.			
5.3.3.10 Characteristics of the inverse diode (for power MOSFET only)			
5.3.3.10.1 Drain-source reverse voltage (V_{DSR}) (Forward voltage of the inverse diode)		+	+
Maximum value at specified reverse drain current (I_{DR}) (forward current of the inverse diode) and at $V_{GS} = 0$.			
5.3.3.10.2 Forward recovery time (t_{fr}) (Reverse recovery time of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.10.3 Peak forward recovery current (I_{FRM}) (Peak reverse recovery current of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.10.4 Forward recovery energy (E_{fr}) (reverse recovery energy of the inverse diode)		+	+
Maximum value under specified conditions.			
5.3.3.11 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$ or ($R_{th(j-c)}$)		+	+
Maximum value.			
5.3.3.12 Drain cut-off current or drain-source off-state resistance	+	+	+
Maximum value of drain-source cut-off current (or alternatively, minimum value of drain-source off-state resistance), at specified low values of drain-source voltage for both polarities and at a specified gate-source voltage.			
5.3.3.13 Forward transconductance (g_{ms}, g_m, g_{fs}) (for power MOSFET only)		+	+
Minimum value, for specified drain-source voltage and drain current, at a temperature of 25 °C at one other higher temperature, preferably equal to the maximum virtual junction temperature.			
5.3.3.14 Breakdown voltage, drain to source ($V_{(BR)DSX}$) (for type B)		+	
Minimum value, at maximum off-state drain current I_{D0} and specified gate-source voltage.			
5.3.3.15 Breakdown voltage, drain to source ($V_{(BR)DSS}$) (for type C)			+
Minimum value, at maximum off-state drain current I_{D0} and gate-source shorted.			

	TYPES		
	A	B	C
5.3.3.16 Gate-source on-state voltage ($V_{GS(on)}$) (for type B and C) Maximum value in the on-state		+	+
5.3.3.17 Internal gate resistance (r_g), where appropriate Maximum and/or typical value, under the electrical conditions specified and at specified frequency		+	+
5.3.3.18 Turn-on energy (per pulse) (E_{on}), where appropriate Maximum value under specified conditions: – drain-source voltage before turn-on; – drain peak current after turn-on; – gate-source voltage; – resistance in the gate-source circuit; – case or ambient temperature or virtual junction temperature.		+	+
5.3.3.19 Turn-off energy (per pulse) (E_{off}), where appropriate Maximum value under specified conditions: – drain peak current before turn-off; – drain-source voltage after turn-off; – gate-source voltage; – resistance in the gate-source circuit; – case or ambient temperature or virtual junction temperature.		+	+
5.3.3.20 Gate charges (Q_G, Q_{GD}, $Q_{GD(th)}$, $Q_{GS(pl)}$) Typical values at specified drain current (I_D), drain-source voltage (V_{DS}) and gate current (I_{GG}) (see Figure 1)		+	+
5.3.3.21 Thermal impedance channel-to-ambient or channel-to-case ($Z_{th(j-a)}$ or $Z_{th(j-c)}$), where appropriate Maximum value.		+	+
5.3.4 Characteristics for low-level amplifier			
5.3.4.1 Gate cut-off current Gate leakage current Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature. Together with: Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+

5.3.4.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.4.3 Drain current at zero gate-source voltage (I_{DSS})

Minimum and maximum values, at a specified drain-source voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.4.4 Drain current at specified gate-source voltage (I_{DSX})

Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.4.5 Gate-source cut-off voltage (V_{GSoff})

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.4.6 Gate-source threshold voltage ($V_{GS(th)}$)

Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.

5.3.4.7 Noise voltage (where appropriate) (V_n)

Maximum value in common-source configuration, under specified circuit conditions.

5.3.4.8 Small signal forward transconductance (g_{ms} , g_m , g_{fs})

Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature, at a specified frequency.

5.3.4.9 Characteristics of the inverse diode (where appropriate)**5.3.4.9.1 Reverse drain current (I_{DR}) (forward current of the inverse diode)**

Maximum value at specified Reverse drain current (I_{DR}) and at $V_{GS} = 0$.

5.3.4.9.2 Forward recovery time (t_{fr}) (Reverse recovery time of the inverse diode)

Maximum value under specified conditions.

TYPES		
A	B	C
+	+	+
+	+	
		+
+	+	
		+
+	+	+
+	+	+
	+	+

	TYPES		
	A	B	C
5.3.4.10 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$ or $R_{th(j-c)}$) Maximum value.		+	+
5.3.5 Characteristics for voltage-controlled resistor			
5.3.5.1 Gate cut-off current Gate leakage current Maximum value, at specified gate-source or gate-drain voltage, other terminal connections being specified, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.5.2 Small-signal drain-source resistance (r_{ds}) Minimum and maximum small-signal values, at zero drain-source voltage and at two or more specified gate-source voltages, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.5.3 Non-linearity distortion factor of drain-source small-signal resistance, where appropriate Maximum value (total or individual harmonic contents), at specified drain-source and gate-source voltages and at specified drain-source a.c. signal, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.	+	+	+
5.3.5.4 Temperature coefficient of the small-signal drain-source resistance Typical value.	+	+	+
5.3.5.5 Drain-source capacitance Maximum small-signal value, at zero drain-source voltage, at a specified gate-source voltage, with the gate short-circuited for a.c. to the source.	+	+	+
5.3.5.6 Drain-gate capacitance Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage.	+	+	+
5.3.5.7 Gate-source capacitance (where appropriate) Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage, with the drain short-circuited for a.c. to the source.	+	+	+
5.3.5.8 Forward transconductance (g_{ms}, g_m, g_{fs}) (for power MOSFET only) Minimum value, for specified drain-source voltage and drain current, at a temperature of 25 °C or at one other higher temperature, preferably equal to the maximum virtual junction temperature.		+	+

		TYPES		
		A	B	C
5.3.5.9 Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-a)}$) or ($R_{th(j-c)}$)	Maximum value.		+	+
5.3.6 Specific characteristics of matched-pair field-effect transistors for low-frequency differential				
5.3.6.1 Difference of gate cut-off currents Difference of gate leakage currents ($I_{G1} - I_{G2}$)	Maximum absolute value, at specified drain-gate or drain-source voltage and drain current.	+	+	+
5.3.6.2 Ratio of drain currents				
5.3.6.2.1 Ratio of drain currents for zero gate-source voltage (I_{DSS1} / I_{DSS2})	Minimum value of the ratio of the drain currents, at a specified drain-source voltage and zero gate-source voltage.	+	+	
5.3.6.2.2 Ratio of drain currents for specified gate-source voltage	Minimum value of the ratio of the drain currents, at specified drain-source and gate-source voltages.			+
NOTE This ratio should be stated as the smaller value divided by the larger value.				
5.3.6.3 Difference of small-signal common-source output conductances, where appropriate ($g_{os1} - g_{os2}$)	Maximum absolute value of the difference of the output conductances, at specified drain-gate or drain-source voltage, drain current, and frequency.	+	+	+
5.3.6.4 Ratio of small-signal common-source forward transconductances ($g_{fs1} - g_{fs2}$)	Minimum value of the ratio of forward transconductances, at specified drain-gate or drain-source voltage, drain current, and frequency	+	+	+
NOTE This ratio should be stated as the smaller value divided by the larger value.				
5.3.6.5 Difference of gate-source voltages ($V_{GS1} - V_{GS2}$)	Maximum absolute value of the difference of the gate-source voltages, at specified drain-gate or drain-source voltage and drain current.	+	+	+
5.3.6.6 Change in difference of gate-source voltages between two temperatures ($\Delta(V_{GS1} - V_{GS2}) _{\Delta T}$)	Maximum absolute value of the change of the difference of the gate-source voltages (as in 5.3.6.5) between two specified temperatures, at the same specified drain-gate or drain-source voltage and drain current.	+	+	+

6 Measuring methods

6.1 General

The polarities of the power supplies, shown in the circuits in this standard, are applicable to N-channel type devices. However, the circuits can be adapted for P-channel type devices by changing the polarities of the meters and the power supplies.

The general precautions listed in Subclause 6.4 of IEC 60747-1:2006 apply. In addition, special care shall be taken to use low-ripple d.c. supplies and to decouple adequately all bias supply voltages at the frequency of measurement. For four-terminal devices, the fourth terminal shall be connected as specified.

When handling these devices, the handling precautions given in IEC 61340 shall be observed. The entire circuit in the following subclauses shall be placed inside an electrostatic screen.

6.2 Verification of ratings (limiting values)

After the following test, confirm the FET characteristics specified in Table 2.

Table 2 – Acceptance defining characteristics

Characteristics	Acceptance criteria
I_{GSS}	$I_{GSS} < USL$
I_{DS^*}	$I_{DS^*} < USL$
$V_{GS(th)}$ (or $V_{GS(off)}$)	$V_{GS(th)} < USL$ or $V_{GS(th)} > LSL$
$V_{DS(on)}$	$V_{DS(on)} < USL$
$r_{DS(on)}$	$r_{DS(on)} < USL$ (only for MOSFET)
USL: upper specified limit LSL: lower specified limit	

6.2.1 Voltages and currents

6.2.1.1 Drain-source voltage (d.c.) (V_{DS^*})

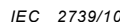
NOTE * = O, R, S or X

– Purpose

To verify the drain-source voltage (d.c.) V_{DS^*} under specified conditions.

– Circuit diagram

See Figure 4 below.



- **Circuit description and requirements**

- **Testing procedure**

- Specified conditions

- Reference point or junction temperature T_{vj}
- Gate-source bias conditions
- Drain-source voltage: rated drain-source voltage

- **Purpose**

- **Circuit diagram**

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- **Circuit description and requirements**

or gate reverse biased

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– **Testing procedure**

Drain-source voltage is set to specified conditions. V_{GG} is increased until gate-source voltage measured on voltmeter V_{GS} reaches the specified gate-source voltage V_{GS}^* . After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj} ;
- Drain-source bias conditions;
- Gate-source voltage: rated gate-source voltage.

6.2.1.3 Gate-drain (d.c.) voltage (V_{GD}^*)

– **Purpose**

To verify the gate-drain (d.c.) voltage for both polarities, under specified conditions.

– **Circuit diagram**

See Figure 6 below.

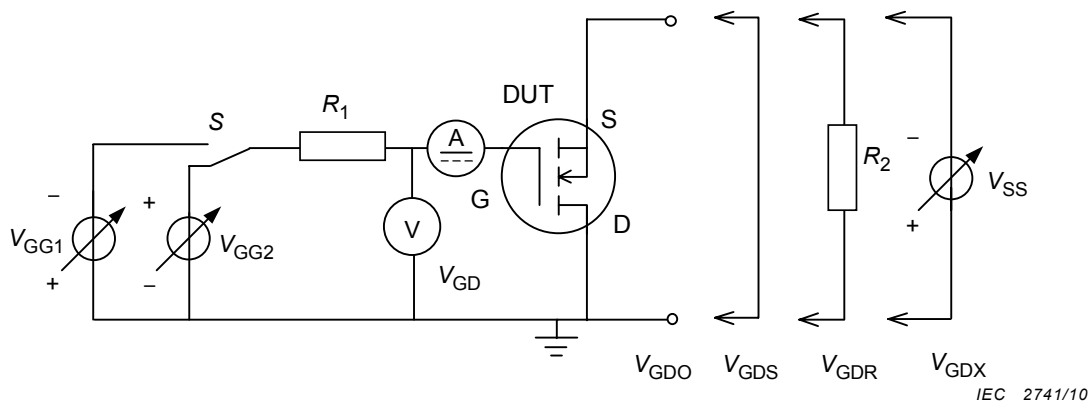


Figure 6 – Circuit diagram for testing of gate-drain voltage

– **Circuit description and requirements**

V_{SS} , V_{GG1} and V_{GG2} are the d.c. voltage supply. V_{GDX} is applied only for gate reverse biased condition of V_{GG2} .

– **Testing procedure**

Source-drain voltage is set to specified conditions. V_{GD} is increased until gate-drain voltage measured on voltmeter V_{DS} reaches the specified gate-drain voltage V_{GD}^* . After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj} ;
- Drain-source bias conditions;
- Gate-drain voltage: rated gate-drain voltage.

6.2.1.4 Drain current (I_D)

– **Purpose**

To verify that drain current capability of FETs is not less than the maximum rated value I_D under specified conditions.

– **Circuit diagram**

See Figure 7 below.

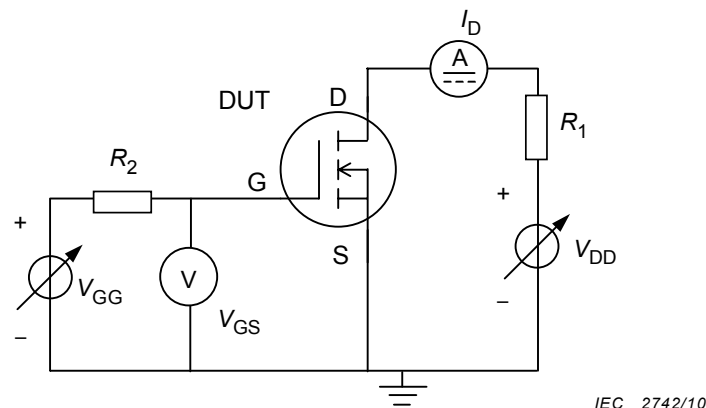


Figure 7 – Basic circuit for the testing of drain current

– **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 and R_2 are protective resistors.

– **Testing procedure**

Specified gate-source voltage is applied to the gate. Temperature (T_a or T_c or T_{vj}) and gate-source voltage are set and kept to the specified value. Drain current is supplied at specified conditions. After the above test, confirm the reference-defining characteristics of DUT being normal by the criteria of Table 2. Drain current is supplied at specified conditions until thermal equilibrium is reached.

– **Specified conditions**

- Reference point or junction temperature T_{vj} ;
- Gate-source voltage V_{GS} .
- Drain current I_D .

6.2.1.5 Peak drain current (I_{DM})

– **Purpose**

To verify the peak drain current under specified conditions.

– **Circuit diagram**

See Figure 8 below.

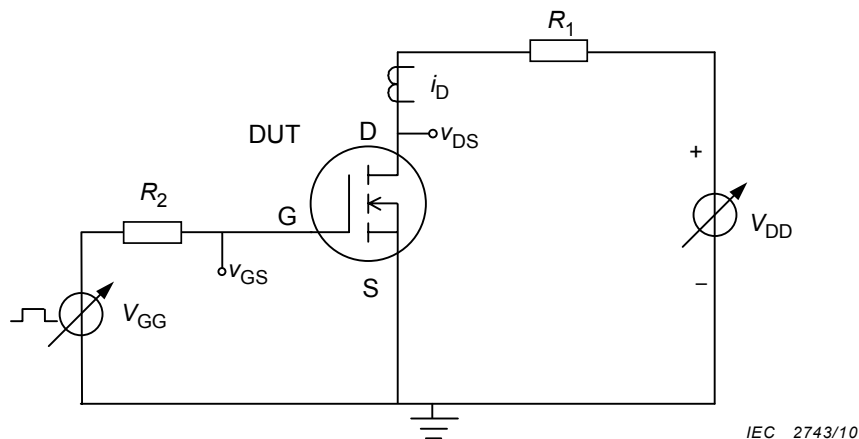


Figure 8 – Circuit diagram for testing of peak drain current

– **Circuit description and requirements**

V_{DD} is the d.c. voltage supply and V_{GG} is the gate pulse generator. R_1 and R_2 are protective resistors.

– **Testing procedure**

A specified gate-source voltage pulse is applied to turn the device on and off. Temperature (T_a or T_c or T_{vj}) is set and kept to the specified value. Peak drain current is conducted at the specified conditions. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– **Specified conditions**

- Reference point or junction temperature T_{vj}
- Gate-source voltage V_{GS}
- Pulse width and duty cycle
- Peak drain current I_{DM}

6.2.1.6 Reverse drain current (I_{DRS}) or (I_{DRX})

– **Purpose**

To verify the reverse drain current under specified conditions.

– **Circuit diagram**

See Figure 9 below.

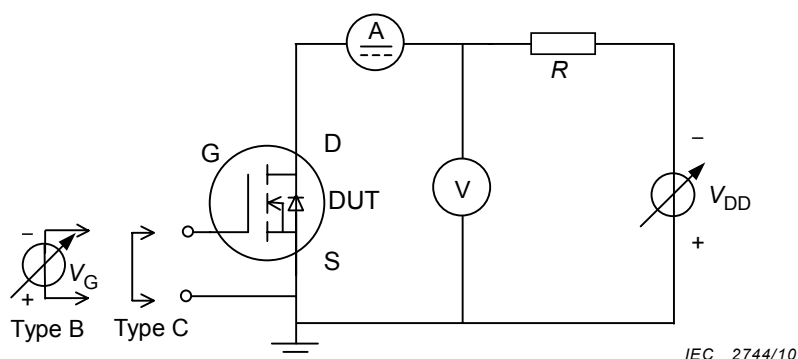


Figure 9 – Basic circuit for the testing of reverse drain current of MOSFETs

– Circuit description and requirements

V_{DD} is the d.c. voltage supply. R is a protective resistor.

– Testing procedure

Gate-source terminals are shorted (C-type) or supplied with an off-bias (B-type). Temperature (T_a or T_c or T_{vj}) is set and kept to the specified value under specified conditions. Reverse drain current is conducted to DUT with MOSFET in off-state. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– Specified conditions

- MOSFET in off-state: the gate condition of B type is set to be kept in the off-state.
- Reference point or junction temperature T_{vj}
- Protective resistor R
- Reverse drain current I_{DR}

6.2.1.7 Peak reverse drain current (I_{DRM})

– Purpose

To verify peak reverse drain current under specified conditions.

– Circuit diagram

See Figure 10 below.

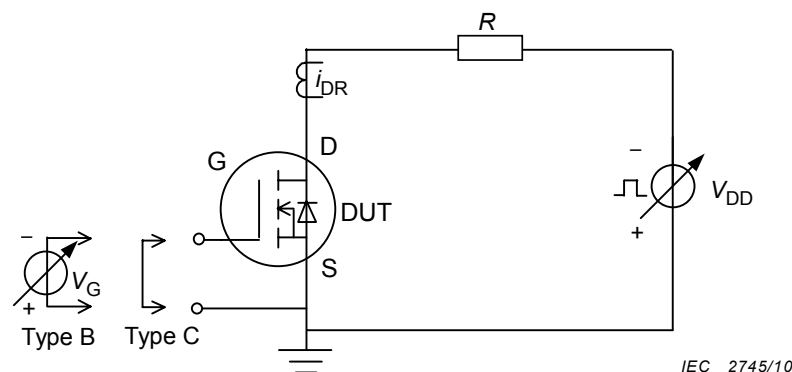


Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs

– Circuit description and requirements

V_{DD} is a pulse voltage source with adjustable pulse width and duty cycle control. R is a protective resistor.

– Testing procedure

Gate-source terminals are connected as specified. The temperature (T_a or T_c or T_{vj}) is set and kept to the specified value. Peak reverse drain current is conducted to DUT by turning on the V_{DD} with MOSFET in off-state. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– Specified conditions

- MOSFET in off-state
- Reference point or junction temperature T_{vj}
- Pulse width and duty cycle; setting up by the pulse switching unit
- Peak reverse drain current I_{DRM}

6.2.2 Safe operating area

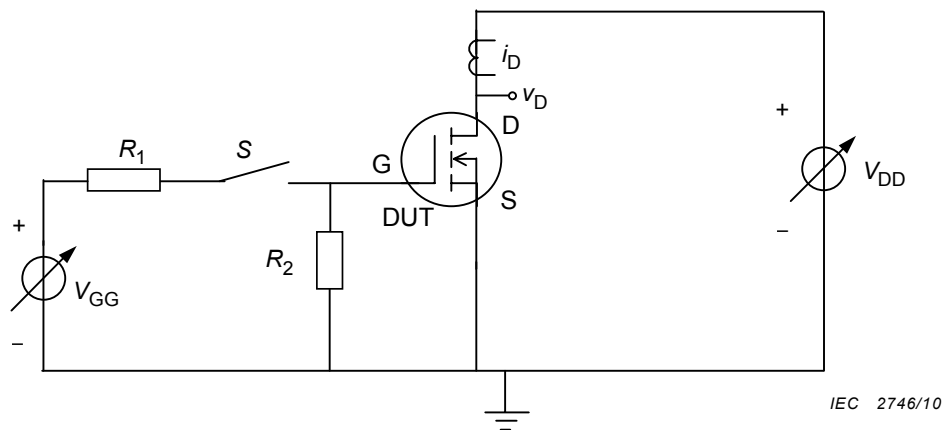
6.2.2.1 Forward-bias safe operating area (FBSOA)

– Purpose

To verify the forward-bias safe operating area of a case-rated power field-effect transistor under specified conditions with non-inductive load.

– Circuit diagram

See Figure 11 below.



DUT = transistor being measured (MOSFET or JFET)

Figure 11 – Circuit diagram for verifying FBSOA

– Circuit description and requirements

V_{GG} , V_{DD} = adjustable voltage sources

R_1 , R_2 = 10 k Ω or as specified

S = switch to obtain the specified sequence of current pulse

– Testing procedure

The case temperature is set to the specified value. The device is switched on and off with the specified pulse duration and duty cycle. V_{DS} and I_D are monitored. V_{GG} and/or V_{DD} are increased until the specified pulse values for V_{DS} and I_D are reached. Under these operating conditions, the device being measured is operated for the specified duration of the test, or for the specified number of pulses, as appropriate. Verification of the FBSOA rating is obtained from the post-test measurements. After the above test, confirm the acceptance-defining characteristics of DUT being normal by the criteria of Table 2.

– Specified conditions

- Case temperature T_c
- Drain-source voltage V_{DS}
- Drain current I_D
- As specified, either d.c. operation or repetitive pulse operation, or a combination of these conditions
- Pulse duration t_p and duty factor δ as appropriate
- As specified, either duration of the test or number of test pulses
- R_1 , R_2 if other than 10 k Ω

- Post-test measurement limits

6.2.2.2 Reverse-bias safe operation area (RBSOA)

– Purpose

To verify the reverse-bias safe operation area under specified conditions with inductive load.

– Circuit diagram and test waveforms

See Figure 12 and Figure 13 below.

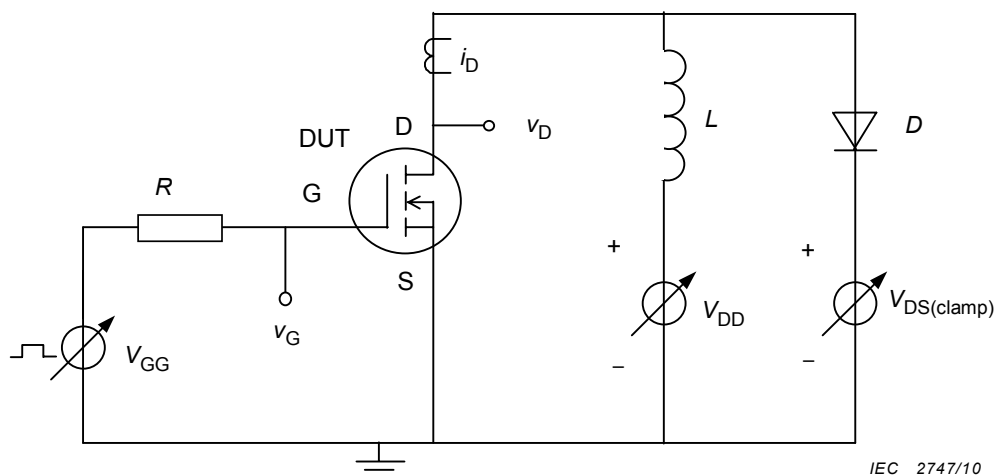


Figure 12 – Circuit diagram for verifying RBSOA

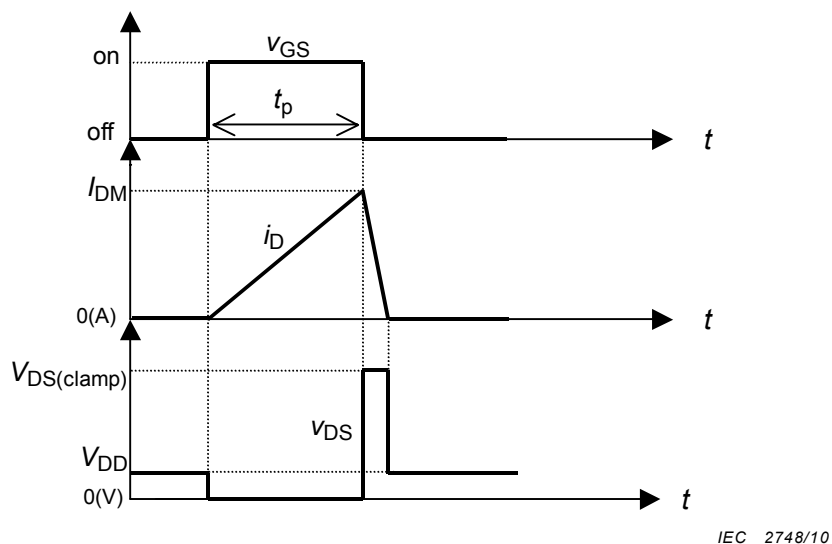


Figure 13 – Test waveforms for verifying RBSOA

– Circuit description and requirements

D = clamping diode

L = inductive load

V_{DD} = adjustable voltage sources

$V_{DS(clamp)}$ = adjustable voltage source for the clamping voltage

t_p = gate-source voltage pulse width

V_{GG} = gate pulse generator

R = gate resistor

– Testing procedure

DUT is turned off at specified I_D . V_{DS} and I_S (I_D) are monitored. The DUT has to turn off I_D and withstand $V_{DS} = V_{DS(\text{clamp})}$.

NOTE Drain-source peak voltage $V_{DSM} < V_{(BR)DS+}$.

The temperature (*reference point temperature* or T_{vj}) is set and kept to a specified value. Under these operating conditions, DUT is operated for the specified duration of the test, or for the specified number of pulses, as appropriate. Verification of the RBSOA rating is obtained from the post-test measurements. After the above test, confirm the acceptance defining characteristics of DUT being normal by the criteria of Table 2. The device is considered defective if, at any instant during the test, the drain-source voltage collapses or oscillates during the fall of the current pulses.

– Specified conditions

- Drain current I_D
- Gate reverse voltage $-V_{GS}$ before and after turn-off
- Drain-source voltage $V_{DS(\text{clamp})}$
- Number of pulses, if greater than one, and pulse width and duty cycle
- Inductance L
- Reference point or virtual junction temperature T_{vj}

– Gate resistor R_G

6.2.2.3 Short-circuit safe operating area (SCSOA)

– Purpose

This test is to verify that the MOSFET operates reliably without failure under load-short-circuited conditions. A short-circuit can occur when the MOSFET is already conducting, or the MOSFET is turned into a short-circuit condition. A test for the latter case is described in the following.

– Circuit diagram and waveforms

See Figure 14 and Figure 15 below.

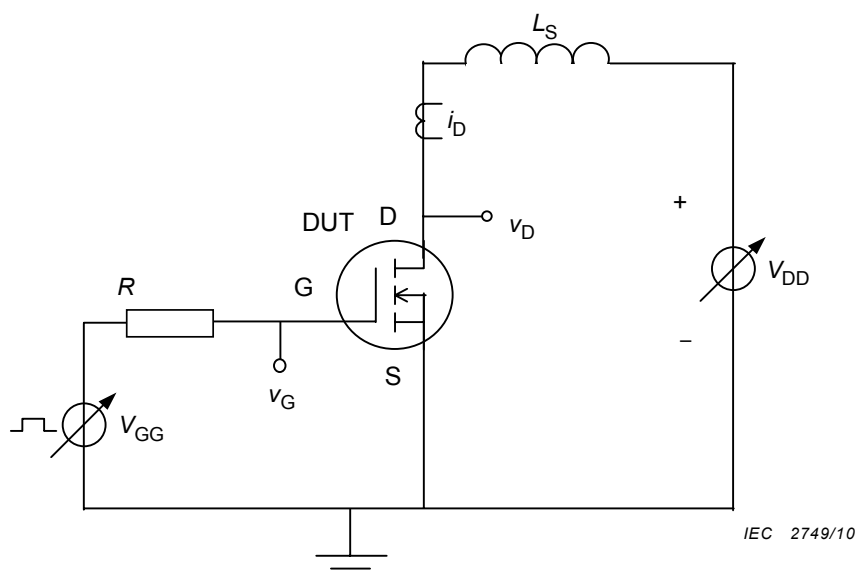


Figure 14 – Circuit for testing safe operating pulse duration at load short

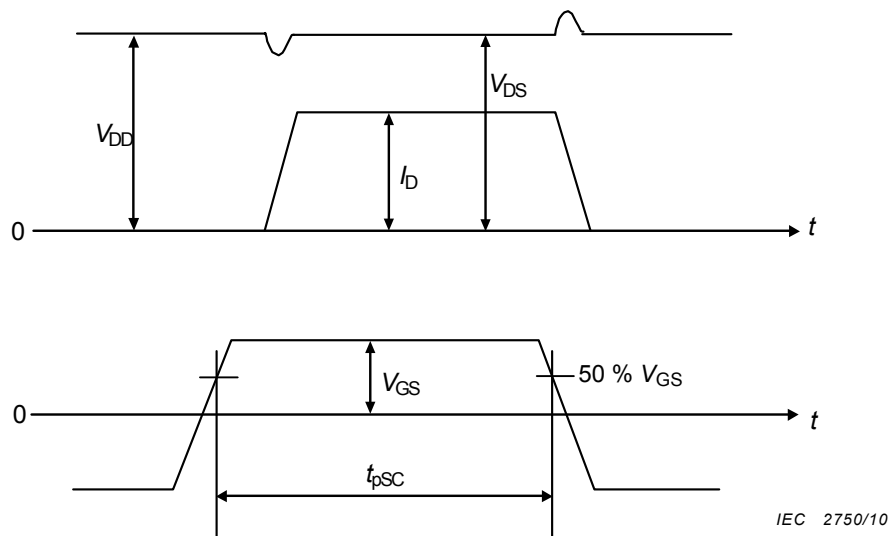


Figure 15 – Waveforms of gate-source voltage V_{GS} , drain current I_D and voltage V_{DS} during load short circuit condition SCSOA

– Circuit descriptions and requirements

L_S represents the maximum permitted stray inductance; it must be low enough to ensure that the maximum short circuit current is reached within the first 25% of the gate pulse duration t_{pSC} .

L_S = stray inductance

V_{DD} = adjustable voltage sources

t_{pSC} = gate-source voltage pulse width

V_{GG} = gate pulse generator

R = gate resistor as specified

– Testing procedure

Temperature is set to the specified value. Gate-source voltage V_{GS} and pulse duration is set to specified values. Drain-source voltage V_{DS} is set to a specified value. The drain currents I_D and V_{DS} are monitored in order to see whether the MOSFET turns on and turns off correctly. After the above test, confirm the acceptance defining characteristics of DUT being normal by the criteria of Table 2.

– Specified conditions

- Drain-source voltage $V_{DS} = V_{DD}$
- On and off-state gate source voltages
- Gate pulse duration t_{pSC}
- Gate resistor R
- Value of stray inductance L_S
- Reference point or virtual junction temperature T_{vj}

6.2.3 Avalanche energy

6.2.3.1 Repetitive avalanche energy (E_{AR})

– Purpose

To verify the repetitive avalanche energy capability in an unclamped inductive switching circuit.

– Circuit diagram and waveforms

See Figure 16 and Figure 17 below.

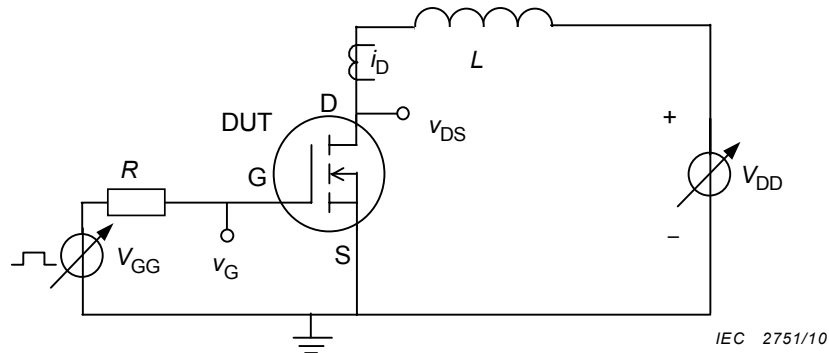


Figure 16 – Circuit for the inductive avalanche switching

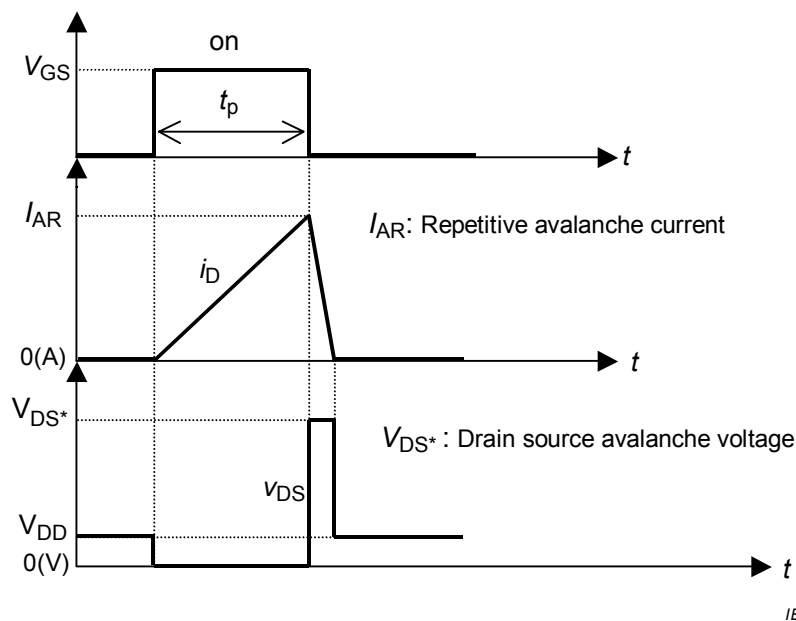


Figure 17 – Waveforms of i_D , v_{DS} and V_{GS} during unclamped inductive switching

– Circuit descriptions and requirements

L = inductive load

V_{DD} = adjustable voltage sources

V_{GG} = gate pulse generator

R = gate resistor as specified

– Test procedure

Temperature is set to the specified value. The supply voltage (V_{DD}) is set to the specified value. The turn-on time of the MOSFET is adjusted in such a way that the specified avalanche current is reached. Under these operating conditions, the DUT is operated with the specified number of pulses and repetition rate. The energy delivered to the DUT can be calculated as follows:

$$E_{AR} = \frac{1}{2} L I_{AR}^2 V_{DS^*} / (V_{DS^*} - V_{DD})$$

After the above test, confirm the acceptance defining characteristics of DUT are normal by the criteria of Table 2. DUT shall be within all specified parameter limits at the completion of the test. The measured value of V_{DS^*} shall be greater than or equal to the minimum breakdown voltage $V_{(BR)DS^*}$ with the permitted avalanche currents I_{AR} .

NOTE When V_{DD} is set to a smaller value compared with V_{DS^*} , E_{AR} is calculated by using the approximate equation of $E_{AR} = \frac{1}{2} L I_{AR}^2$.

– Specified conditions

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DD}
- Gate-source voltage V_{GS}
- Drain current I_D
- Inductance L
- Frequency f

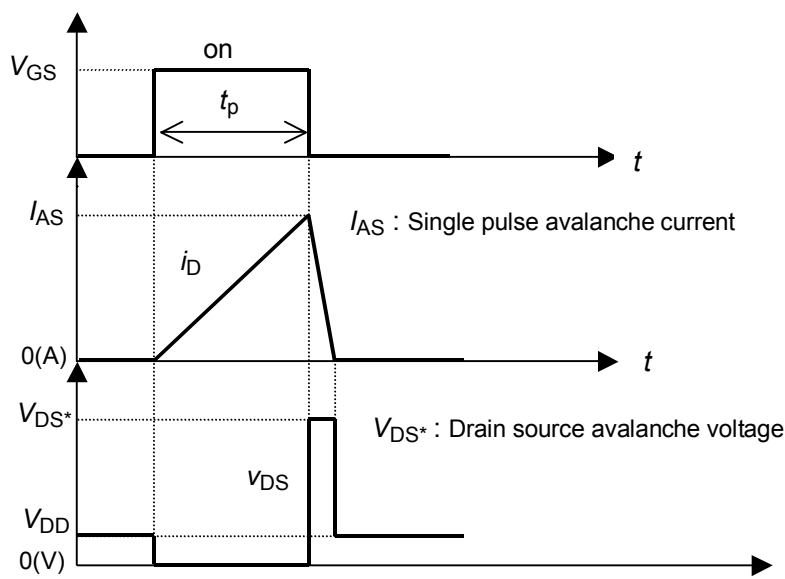
6.2.3.2 Non-repetitive avalanche switching energy (E_{AS})

– Purpose

To verify the non-repetitive avalanche switching energy.

– Circuit diagram and waveforms

See Figure 18 below.



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Figure 18 – Waveforms of I_D , V_{DS} and V_{GS} for the non-repetitive avalanche switching

– Circuit descriptions and requirements

L = inductive load

R_G = gate resistor as specified

Temperature is set to the specified value. The supply voltage (V_{DD}) is set to the specified value. The turn-on time of the MOSFET is adjusted in such a way that the specified avalanche current is reached. Under these operating conditions, the DUT is operated with the single pulse. The energy delivered to the DUT can be calculated as follows:

$$E_{AS} = \frac{1}{2} L I_{AS}^2 V_{DS^*} / (V_{DS^*} - V_{DD})$$

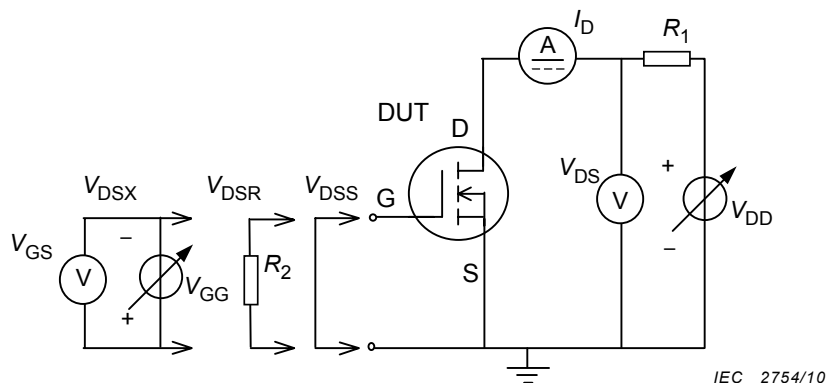
NOTE When V_{DD} is set to a smaller value compared with V_{DS^*} , E_{AS} is calculated by using the approximate equation of $E_{AS} = \frac{1}{2} L I_{AS}^2$.

- Reference point or junction temperature T_{vj}
- Drain-source voltage V_{DD}
- Gate-source voltage V_{GS}
- Drain current I_D
- Inductance L
- Single pulse

6.3.1 Breakdown voltage, drain to source ($V_{(BR)DS^*}$)

To measure the drain to source breakdown voltage under specified conditions.

See Figure 19 below.



- **Circuit description and requirements**

V_{DD} and V_{GG} are the d.c. voltage supply. R_1 is a circuit protection resistor.