

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices –
Part 9: Discrete devices – Insulated-gate bipolar transistors (IGBTs)**

**Dispositifs à semiconducteurs –
Partie 9: Dispositifs discrets – Transistors bipolaires à grille isolée (IGBT)**



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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

ICS 31.080.01; 31.080.30

ISBN 978-2-8322-7530-6

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES –

Part 9: Discrete devices – Insulated-gate bipolar transistors (IGBTs)

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International Standard IEC 60747-9 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition cancels and replaces the second edition published in 2007. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) reverse-blocking IGBT and its related technical contents have been added;
- b) reverse-conducting IGBT and its related technical contents have been added;
- c) some parts of the previous edition have been amended, combined or deleted.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47E/675/FDIS	47E/684/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60747 series, published under the general title: *Semiconductor devices*, can be found on the IEC website.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES –

Part 9: Discrete devices – Insulated-gate bipolar transistors (IGBTs)

1 Scope

This part of IEC 60747 specifies product specific standards for terminology, letter symbols, essential ratings and characteristics, verification of ratings and methods of measurement for insulated-gate bipolar transistors (IGBTs).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*
IEC 60747-1:2006/AMD1:2010

IEC 61340 (all parts), *Electrostatics*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1 General terms

3.1.1

insulated-gate bipolar transistor IGBT

transistor having a conductive channel and one PN junction in the forward direction and another PN junction in the reverse direction, the current flowing through the channel and the junction being controlled by an electric field resulting from a voltage applied between the gate and emitter terminals

Note 1 to entry: With collector-emitter voltage applied, the collector side PN junction is forward biased.

Note 2 to entry: This note applies to the French language only.

3.1.2

N-channel IGBT

IGBT that has one or more N-type conduction channels

[SOURCE: IEC 60050-521:2002, 521-04-56, modified – reworded for IGBT.]

3.1.3

P-channel IGBT

IGBT that has one or more P-type conduction channels

[SOURCE: IEC 60050-521:2002, 521-04-57, modified – reworded for IGBT.]

3.1.4

collector terminal

collector

C

for an N-channel (a P-channel) IGBT, the terminal to (from) which the collector current flows from (to) the external circuit

3.1.5

emitter terminal

emitter

E

for an N-channel (a P-channel) IGBT, terminal from (to) which the collector current flows to (from) the external circuit

3.1.6

gate terminal

gate

G

for an N-channel (a P-channel) IGBT, terminal to which a voltage is applied against the emitter terminal in order to control the collector current

3.1.7

reverse-blocking IGBT

RB-IGBT

IGBT which, for negative collector-emitter voltage, exhibits a reverse blocking state with a monolithic device structure

Note 1 to entry: This note applies to the French language only.

3.1.8

reverse-conducting IGBT

RC-IGBT

IGBT which, for negative collector-emitter voltage, conducts large currents at voltages comparable in magnitude to the forward on-state voltage with monolithic device structure

Note 1 to entry: This note applies to the French language only.

3.2 Terms related to ratings and characteristics, voltages and currents

3.2.1

collector-emitter voltage

voltage between collector and emitter

3.2.2

collector-emitter voltage with gate-emitter short-circuited

V_{CES}

collector-emitter voltage at which the collector current has a specified low (absolute) value with the gate-emitter short-circuited

3.2.3**collector-emitter sustaining voltage** $V_{CE^{*}sus}$

collector-emitter breakdown (self-clamping) voltage at relatively high values of collector current where the voltage is relatively insensitive to changes in collector current, for a specified termination between gate and emitter terminals

Note 1 to entry: The specified termination between gate and emitter terminals is indicated in the letter symbol by the third subscript '*'; see 4.2 of IEC 60747-7:2010.

3.2.4**collector-emitter breakdown voltage** $V_{(BR)CES}$

voltage between collector and emitter above which the collector current rises steeply, with gate to emitter short-circuited

3.2.5**collector-emitter saturation voltage** V_{CEsat}

collector-emitter voltage under conditions of gate-emitter voltage at which the collector current is essentially independent of the gate-emitter voltage

3.2.6**gate-emitter voltage**

voltage between gate and emitter

3.2.7**gate-emitter threshold voltage** $V_{GE(th)}$

gate-emitter voltage at which the collector current has a specified low (absolute) value

3.2.8**electrostatic discharge voltage**

voltage that can be applied to the gate terminal without destruction of the isolation layer

3.2.9**reverse voltage** V_R

<reverse-blocking IGBT> value of the voltage applied to an IGBT in the reverse collector-emitter direction

3.2.10**reverse-conducting voltage** V_{RC}

<reverse-conducting IGBT> value of the voltage which results from the flow of current in the reverse collector-emitter direction

Note 1 to entry: Where no ambiguity arises, V_F or V_{EC} may be used.

3.2.11**collector cut-off current** I_{CE}

collector current at a specific collector-emitter voltage below the breakdown region and gate off-state

3.2.12**collector current** I_C

direct current that is switched (controlled) by the IGBT

3.2.13

tail current

I_{CZ}

collector current during the tail time

3.2.14

gate leakage current

gate-emitter leakage current

I_{GES}

leakage current into the gate terminal at a specified gate-emitter voltage with the collector terminal short-circuited to the emitter terminal

3.2.15

reverse current

I_R

<reverse-blocking IGBT> value of the current flowing through the IGBT when the specified reverse collector-emitter voltage is applied

3.2.16

reverse-conducting current

I_{RC}

<reverse-conducting IGBT> total conductive current flowing through the IGBT when the collector-emitter reverse voltage is applied

Note 1 to entry: Where no ambiguity arises, I_F or I_E may be used.

3.2.17

reverse recovery current

I_{rr}

<reverse-blocking IGBT> reverse current that occurs during the reverse recovery time

Note 1 to entry: For the peak value of the reverse recovery current during the reverse recovery time, only the letter symbol I_{rrm} may be used.

3.2.18

forward recovery current

I_{fr}

<reverse-conducting IGBT> forward current that occurs during the forward recovery time

Note 1 to entry: For the peak value of the forward recovery current during the forward recovery time, only the letter symbol I_{frm} may be used.

3.2.19

safe operating area

SOA

collector current versus collector-emitter voltage where the IGBT is able to turn-on and turn-off without failure

Note 1 to entry: This note applies to the French language only.

3.2.19.1

forward bias safe operating area

FBSOA

collector current versus collector-emitter voltage where the IGBT is able to turn-on and is able to be on-state without failure

Note 1 to entry: This note applies to the French language only.

3.2.19.2**reverse bias safe operating area****RBSOA**

collector current versus collector-emitter voltage where the IGBT is able to turn-off without failure

Note 1 to entry: RBSOA is not only for repetitive peak collector current but also for short-circuit conditions.

Note 2 to entry: This note applies to the French language only.

3.2.19.3**short-circuit safe operating area****SCSOA**

short-circuit duration and collector-emitter voltage where the IGBT is able to turn-on and turn-off without failure

Note 1 to entry: This note applies to the French language only.

3.3 Terms related to ratings and characteristics**3.3.1****input capacitance** C_{ies}

capacitance between the gate and emitter terminals with the collector terminal short-circuited to the emitter terminal for alternating current

3.3.2**output capacitance** C_{oes}

capacitance between the collector and emitter terminals with the gate terminal short-circuited to the emitter terminal for alternating current

3.3.3**reverse transfer capacitance** C_{res}

capacitance between the collector and gate terminals

3.3.4**gate charge** Q_G

charge required to raise the gate-emitter voltage from a specified low to a specified high level

3.3.5**internal gate resistance** r_g

internal equivalent series resistance between the gate and the gate terminal

Note 1 to entry: Where no ambiguity arises, R_{Gint} may be used.

3.3.6**turn-on energy** E_{on}

energy dissipated inside the IGBT during the turn-on of a single collector current pulse

Note 1 to entry: The corresponding turn-on power dissipation under periodic pulse conditions is obtained by multiplying E_{on} by the pulse frequency.

3.3.7**turn-off energy** E_{off}

energy dissipated inside the IGBT during the turn-off time plus the tail time of a single collector current pulse

Note 1 to entry: The corresponding turn-off power dissipation under periodic pulse conditions is obtained by multiplying E_{off} by the pulse frequency.

3.3.8**reverse recovery energy** E_{rr}

<reverse-blocking IGBT> energy dissipated within the IGBT during a specified integration time of a single collector current pulse, when the IGBT is switched from a specified forward current condition to a specified reverse voltage condition with forward biased gate condition

Note 1 to entry: The corresponding reverse recovery power dissipation under periodic pulse conditions is obtained by multiplying E_{rr} by the pulse frequency.

3.3.9**forward recovery energy** E_{fr}

<reverse-conducting IGBT> energy dissipated within the IGBT during a specified integration time of a single collector current pulse, when the IGBT is switched from a specified reverse-conducting current to a specified collector-emitter voltage condition with short-circuit between gate and emitter, or reverse biased gate condition

Note 1 to entry: The corresponding forward recovery power dissipation under periodic pulse conditions is obtained by multiplying E_{fr} by the pulse frequency.

3.3.10**reverse recovered charge** Q_{rr}

<reverse-blocking IGBT> total charge recovered from the IGBT during a specified integration time of a single collector current pulse, when the IGBT is switched from a specified forward current condition to a specified reverse voltage condition with forward biased gate condition

3.3.11**forward recovered charge** Q_{fr}

<reverse-conducting IGBT> total charge recovered from the IGBT during a specified integration time of a single collector current pulse, when the IGBT is switched from a specified reverse-conducting current condition to a specified collector-emitter voltage condition with short-circuit between gate and emitter, or reverse biased gate condition

3.3.12**turn-on delay time** $t_{\text{d(on)}}$

time interval between the beginning of a voltage pulse across the input terminals which switches the IGBT from the off-state to the on-state and the beginning of the rise of the collector current

Note 1 to entry: Usually the time is measured between points corresponding to 10 % of the input and output pulse amplitudes.

3.3.13**rise time** t_{r}

time interval between the instants at which the rise of the collector current reaches specified low and high values, respectively, when the IGBT is being switched from the off-state to the on-state

Note 1 to entry: Usually the low and high values are 10 % and 90 % of the pulse amplitude.

3.3.14

turn-on time

t_{on}

sum of the turn-on delay time and the rise time

3.3.15

turn-off delay time

$t_{d(off)}$

time interval between the end of the voltage pulse across the input terminals which has held the IGBT in its on-state and the beginning of the fall of the collector current when the IGBT is switched from the on-state to the off-state

Note 1 to entry: Usually the time is measured between points corresponding to 90 % of the input and output pulse amplitudes.

3.3.16

fall time

t_f

time interval between the instants at which the fall of the collector current reaches specified high and low values, respectively, when the IGBT is switched from the on-state to the off-state

Note 1 to entry: Usually the high and low values are 90 % and 10 % of the pulse amplitude.

3.3.17

turn-off time

t_{off}

sum of the turn-off delay time and the fall time

3.3.18

tail time

t_z

time interval from the end of the turn-off time to the instant at which the collector current has fallen to 2 % or lower specified value

Note 1 to entry: Where no ambiguity arises, t_t may be used.

3.3.19

reverse recovery time

t_{rr}

<reverse-blocking IGBT> time interval between the instant when the current passes through zero, when changing from the forward direction to the reverse direction, and the instant when the reverse current is reduced from its peak value I_{rrm} to a specified low value or when the extrapolated reverse current reaches zero

3.3.20

forward recovery time

t_{fr}

<reverse-conducting IGBT> time interval between the instant when the current passes through zero, when changing from the reverse direction to the forward direction, and the instant when the forward current is reduced from its peak value I_{frm} to a specified low value or when the extrapolated reverse current reaches zero

4 Letter symbols

4.1 General

General letter symbols for IGBTs are defined in Clause 4 of IEC 60747-1:2006.

4.2 Graphical symbols

The graphical symbols are shown in Figure 1, and are used in this document. The devices inside the circle are connected monolithically. In the case of Figure 1a) (IGBT), the circle can be omitted.

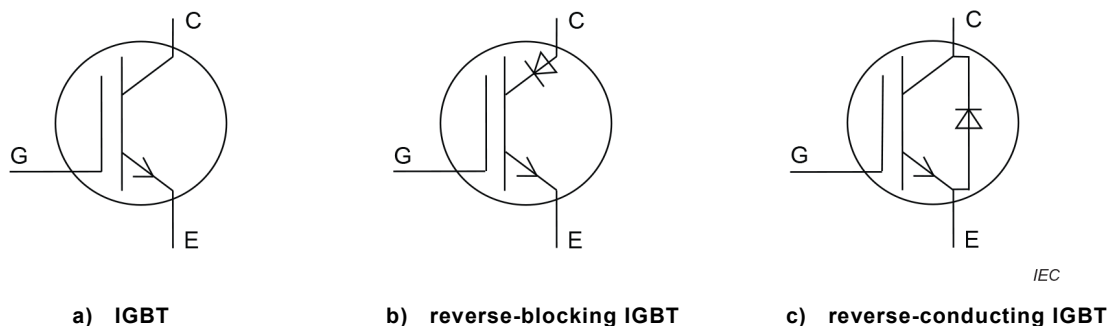


Figure 1 – Graphical symbols

Only the graphical symbols for an N-channel IGBT are used in this document. It equally applies for the measurement of P-channel devices. In the case of P-channel devices, polarity shall be adapted.

4.3 Additional general subscripts

C,c	collector
E,e	emitter
G,g	gate
sat	saturation
th	threshold
Z,z	tail
S	termination with a short-circuit
R	termination with a resistor
X	termination with specified gate-emitter voltage
sus	sustaining
I	IGBT
RC	reverse-conducting

4.4 List of letter symbols

4.4.1 Voltages

Name and designation	Letter symbol
Collector-emitter voltage	V_{CE}
Collector-emitter voltage, gate-emitter short-circuited	V_{CES}
Collector-emitter sustaining voltage	$V_{CE^{*}sus}$
Collector-emitter breakdown voltage, gate-emitter short-circuited	$V_{(BR)CES}$
Collector-emitter saturation voltage	V_{CEsat}
Gate-emitter voltage	V_{GE}
Gate-emitter voltage, collector-emitter short-circuited	V_{GES}
Gate-emitter threshold voltage	$V_{GE(th)}$
Reverse voltage of a reverse-blocking IGBT	$V_{R^{*}}$
Reverse-conducting voltage of a reverse-conducting IGBT	V_{RC} (or V_F or V_{EC})

4.4.2 Currents

Name and designation	Letter symbol
Collector current	I_C
Peak collector current	I_{CM}
Repetitive peak collector current	I_{CRM} (or I_{CP})
Non-repetitive peak collector current	I_{CSM}
Collector-emitter cut-off current, gate-emitter short-circuited	I_{CES}
Tail current	I_{CZ}
Gate current	I_G
Gate leakage current, collector-emitter short-circuited	I_{GES}
Reverse current of a reverse-blocking IGBT	I_{R^*}
Reverse-conducting current of a reverse-conducting IGBT	I_{RC} (or I_F or I_E)
Repetitive peak reverse-conducting current of a reverse-conducting IGBT	I_{RCRM} (or I_{FP})
Non-repetitive peak reverse-conducting current of a reverse-conducting IGBT	I_{RCSM}
Reverse recovery current of a reverse-blocking IGBT	I_{rr}
Forward recovery current of a reverse-conducting IGBT	I_{fr}

4.4.3 Other electrical magnitudes

Name and designation	Letter symbol
Input capacitance	C_{ies}
Output capacitance	C_{oes}
Reverse transfer capacitance	C_{res}
Gate charge	Q_G
Internal gate resistance	r_g
Turn-on power dissipation	P_{on}
Turn-on energy	E_{on}
Turn-off power dissipation	P_{off}
Turn-off energy	E_{off}
Reverse recovery power dissipation of a reverse-blocking IGBT	P_{rr}
Reverse recovery energy of a reverse-blocking IGBT	E_{rr}
Reverse recovered charge of a reverse-blocking IGBT	Q_{rr}
Forward recovery power dissipation of a reverse-conducting IGBT	P_{fr}
Forward recovery energy of a reverse-conducting IGBT	E_{fr}
Forward recovered charge of a reverse-conducting IGBT	Q_{fr}
Conducting state power dissipation	P_{cond}
Conducting state energy	E_{cond}
Total power dissipation (Collector power dissipation)	P_{tot} (P_C)

4.4.4 Time

Name and designation	Letter symbol
Turn-on delay time	$t_{d(on)}$
Rise time	t_r
Turn-on time	t_{on}
Turn-off delay time	$t_{d(off)}$
Fall time	t_f
Turn-off time	t_{off}
Tail time	t_z (or t_t)
Reverse recovery time of a reverse-blocking IGBT	t_{rr}
Forward recovery time of a reverse-conducting IGBT	t_{fr}
Short-circuit withstand pulse duration	t_{psc}

4.4.5 Thermal magnitudes

Name and designation	Letter symbol
Thermal resistance junction to case	$R_{th(j-c)}$
Transient thermal impedance junction to case	$Z_{th(j-c)}$

5 Essential ratings and characteristics

5.1 General

There are several subcategories of RC-IGBTs:

- diode part only suitable for soft commutation;
- diode part suitable for hard switching (most common approach);
- diode characteristics intentionally designed to change with gate voltage (between low conduction voltage drop and low recovery charge).

This document only covers subcategory b) because it is the most commonly used.

5.2 Ratings (limiting values)

5.2.1 General

Ratings shall be valid for the whole range of operating conditions as stated for the particular device, with reference to a curve where appropriate.

5.2.2 Ambient or case or virtual junction operating temperature (T_a or T_c or T_{vj})

Maximum and minimum values.

5.2.3 Storage temperature (T_{stg})

Maximum and minimum values.

5.2.4 Collector-emitter voltage with gate-emitter short-circuited (V_{CES})

Maximum value.

NOTE This rating is less than $V_{(BR)CES}$. (See 5.3.2.)

5.2.5 Gate-emitter voltage with collector-emitter short-circuit (V_{GES})

Maximum positive and negative values.

5.2.6 Continuous (direct) reverse voltage of a reverse-blocking IGBT (V_{R*})

Maximum value.

5.2.7 Continuous (direct) collector current (I_C)

Maximum value.

5.2.8 Repetitive peak collector current (I_{CRM})

Maximum value for rectangular pulses with specified pulse duration and duty cycle.

5.2.9 Non-repetitive peak collector current (I_{CSM})

Maximum value for a rectangular pulse with specified pulse duration.

5.2.10 Continuous (direct) reverse-conducting current of a reverse-conducting IGBT (I_{RC})

Maximum value.

5.2.11 Repetitive peak reverse-conducting current of a reverse-conducting IGBT (I_{RCRM})

Maximum value for rectangular pulses with specified pulse duration and duty cycle.

5.2.12 Non-repetitive peak reverse-conducting current of a reverse-conducting IGBT (I_{RCSM})

Maximum value for a rectangular pulse with specified pulse duration.

5.2.13 Total power dissipation (P_{tot})

Maximum value with a derating curve where appropriate.

5.2.14 Maximum forward biased safe operating area (FBSOA) (where appropriate)

Diagram showing the maximum rated collector current I_C after turn-on, which shall not be exceeded, even under the best cooling conditions, as a function of the collector-emitter voltage V_{CE} before and during turn-on for direct current and various pulse durations at 25 °C case temperature.

NOTE The test method is shown in Annex D.

5.2.15 Maximum reverse biased safe operating area (RBSOA)

Diagram showing the area of collector current I_C and collector-emitter voltage V_{CE} , which the IGBTs will sustain simultaneously for a short period of time during turn-off without failure under the specified conditions.

NOTE The turn-off capability of the collector current for inductive load is different, and its measuring method is shown in Annex C.

5.2.16 Maximum short-circuit safe operating area (SCSOA)

SCSOA is given by a pair of values of short-circuit duration t_{psc} and collector-emitter voltage V_{CE} which shall not be exceeded under the load short-circuit conditions. The device may be turned on and turned off again for shorting a voltage source without failure.

Where no ambiguity arises, t_{sc} may be used instead of t_{psc} .

5.2.17 Maximum terminal current (I_{tRMS}) (where appropriate)

Maximum RMS value of the current through the main terminals.

5.2.18 Mounting force (F)

Maximum and minimum values, where appropriate.

5.2.19 Mounting torque (M)

Maximum and minimum values, where appropriate.

5.3 Characteristics

5.3.1 General

Characteristics shall be given at $T_{vj} = 25\text{ °C}$ except where otherwise stated, and at one other specified temperature.

5.3.2 Collector-emitter breakdown voltage ($V_{(BR)CES}$) (where appropriate)

Minimum value with gate-emitter short-circuited and at specified collector current.

NOTE The measuring method is shown in Annex A.

5.3.3 Collector-emitter sustaining voltage (V_{CE*sus}) (where appropriate)

Minimum value at specified collector current and for a specified termination between gate and emitter conditions.

NOTE The measuring method is shown in Annex B.

5.3.4 Collector-emitter saturation voltage (V_{CEsat})

Maximum value at specified gate voltage and collector current.

5.3.5 Gate-emitter threshold voltage ($V_{GE(th)}$)

Minimum and maximum values at specified collector-emitter voltage and collector current.

5.3.6 Reverse-conducting voltage of a reverse-conducting IGBT (V_{RC})

Maximum value at specified reverse-conducting current.

5.3.7 Collector-emitter cut-off current (I_{CE*})

Maximum value at specified high collector-emitter voltage and for a specified termination between gate and emitter terminals.

5.3.8 Gate leakage current (I_{GES})

Maximum value at the maximum rated gate-emitter voltage.

5.3.9 Reverse current of a reverse-blocking IGBT (I_{R*})

Maximum value at specified high reverse collector-emitter voltage and for a specified termination between gate and emitter terminals.

5.3.10 Capacitances

5.3.10.1 General

Typical values of the following, at specified collector-emitter voltage and test frequency.

5.3.10.2 Input capacitance (C_{ies})

Typical input capacitance as small-signal value, in common-emitter configuration, under specified collector-emitter voltage and gate-emitter voltage conditions and specified frequency, with the output short-circuited to alternating current.

5.3.10.3 Output capacitance (C_{oes})

Typical output capacitance as small-signal value, in common-emitter configuration, under specified collector-emitter voltage and gate-emitter voltage conditions and specified frequency, with the input short-circuited to alternating current.

5.3.10.4 Reverse transfer capacitance (C_{res})

Typical reverse transfer capacitance as small-signal value, in common-emitter configuration, under specified collector-emitter voltage and gate-emitter voltage conditions and specified frequency.

5.3.11 Gate charge (Q_G)

Typical value at specified values of gate-emitter voltage, collector-emitter voltage before turn-on and collector current after turn-on.

5.3.12 Internal gate resistance (r_g)

Maximum and/or typical value.

5.3.13 Switching characteristics

5.3.13.1 Turn-on delay time ($t_{d(on)}$), rise time (t_r) and turn-on energy (E_{on})

Maximum and/or typical value per pulse under the following specified conditions:

- collector-emitter voltage before turn-on;
- collector current after turn-on;
- load conditions;
- gate-emitter voltage;
- resistance in the gate-emitter circuit;
- unclamped stray inductance of main circuit;
- case or ambient temperature or virtual junction temperature.

5.3.13.2 Turn-off delay time ($t_{d(off)}$), fall time (t_f), tail time (t_z) and turn-off energy (E_{off})

Maximum and/or typical value per pulse under the following specified conditions:

- collector current before turn-off;
- collector-emitter voltage after turn-off;

- load conditions;
- gate-emitter voltage;
- resistance in the gate-emitter circuit;
- unclamped stray inductance of main circuit;
- case or ambient temperature or virtual junction temperature.

5.3.13.3 Peak reverse recovery current (I_{rrm}), reverse recovery time (t_{rr}), reverse recovery energy (E_{rr}) and reverse recovered charge (Q_{rr}) of a reverse-blocking IGBT

Maximum and/or typical value per pulse under the following specified conditions:

- collector current before switching to reverse direction with positive gate bias;
- decay rate of collector current di_C/dt ;
- reverse collector-emitter voltage after switching to reverse direction;
- load conditions;
- unclamped stray inductance of main circuit;
- case or ambient temperature or virtual junction temperature.

5.3.13.4 Peak forward recovery current (I_{frm}), forward recovery time (t_{fr}), forward recovery energy (E_{fr}) and forward recovered charge (Q_{fr}) of a reverse-conducting IGBT

Maximum and/or typical value per pulse under the following specified conditions:

- reverse-conducting current before switching to forward direction with short-circuit between gate and emitter, or reverse biased gate condition;
- decay rate of reverse-conducting current di_{RC}/dt ;
- collector-emitter voltage after switching to forward direction;
- load conditions;
- unclamped stray inductance of main circuit;
- case or ambient temperature or virtual junction temperature.

5.3.14 Thermal resistance junction to case ($R_{th(j-c)}$)

Maximum value for case-rated IGBTs.

NOTE For reverse conducting IGBTs, thermal resistance for the forward (IGBT) and reverse (diode) direction is provided separately as $R_{th(j-a)I}$ and $R_{th(j-c)RC}$ in case of different values for both.

5.3.15 Thermal resistance junction to ambient ($R_{th(j-a)}$)

Maximum value for ambient-rated IGBTs.

NOTE For reverse conducting IGBTs, thermal resistance for the forward (IGBT) and reverse (diode) direction is provided separately as $R_{th(j-a)I}$ and $R_{th(j-a)RC}$ in case of different values for both.

5.3.16 Transient thermal impedance junction to case ($Z_{th(j-c)}$)

For case-rated IGBTs, diagram showing the maximum values against the time elapsed after a step change in power dissipation, or analytical elements.

NOTE For reverse conducting IGBTs, thermal impedance for the forward (IGBT) and reverse (diode) direction is provided separately as $Z_{th(j-c)I}$ and $Z_{th(j-c)RC}$ in case of different values for both.

5.3.17 Transient thermal impedance junction to ambient ($Z_{th(j-a)}$)

For ambient-rated IGBTs, diagram showing the maximum values against the time elapsed after a step change in power dissipation.

NOTE For reverse conducting IGBTs, thermal impedance for the forward (IGBT) and reverse (diode) direction is provided separately as $Z_{th(j-a)I}$ and $Z_{th(j-a)RC}$ in case of different values for both.

6 Measuring methods

6.1 General

The polarities shown in these circuits are applicable to N-channel devices. The circuits can be adapted for P-channel devices by inverting the polarities of the meters, generators and power supplies. The handling precautions given in IEC 61340 (all parts) and the measuring method procedures given in IEC 60747-1 apply.

6.2 Verification of ratings (limiting values)

6.2.1 General

After the following test, confirm the IGBT characteristics specified in Table 1.

Table 1 – Acceptance defining characteristics

Characteristics	Acceptance criteria
I_{CES}	$I_{CES} < USL$
I_{GES}	$I_{GES} < USL$
I_R (RB-IGBT)	$I_R < USL$
V_{CEsat}	$V_{CEsat} < USL$
$V_{GE(th)}$	$LSL < V_{GE(th)} < USL$
V_{RC} (RC-IGBT)	$V_{RC} < USL$
USL: upper specification limit LSL: lower specification limit	

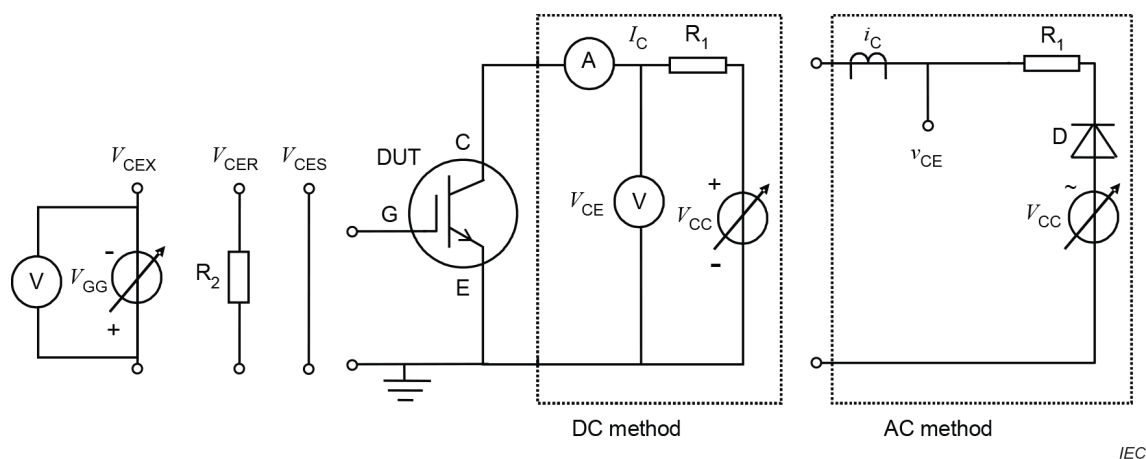
6.2.2 Collector-emitter voltages (V_{CES} , V_{CER} , V_{CEX})

6.2.2.1 Purpose

To verify that an IGBT withstands the rated collector-emitter voltages V_{CES} , V_{CER} or V_{CEX} under specified conditions.

6.2.2.2 Circuit diagram

The circuit diagram is shown in Figure 2.



Key

DUT device under test

D diode for rectifying

Figure 2 – Circuit for testing the collector-emitter voltages V_{CES} , V_{CER} , V_{CEX}

6.2.2.3 Circuit description

V_{CC} and V_{GG} are the voltage sources. R_1 is a circuit protection resistor. R_2 is a resistor connected between the gate and emitter.

6.2.2.4 Test procedure

There are two methods, i.e. the DC method and the AC method with circuits according to Figure 2.

The temperature is set to the specified value. The specified condition between the gate and emitter is applied. The collector-emitter voltage is increased until the specified value and the current I_{CES} , I_{CER} or I_{CEX} is measured with reference to the applied gate conditions.

6.2.2.5 Specified conditions

- Collector-emitter voltage V_{CE} .
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- V_{CEX} : gate-emitter voltage $-V_{GG}$.
- V_{CER} : resistor connected between gate and emitter.
- V_{CES} : short-circuit between gate and emitter.

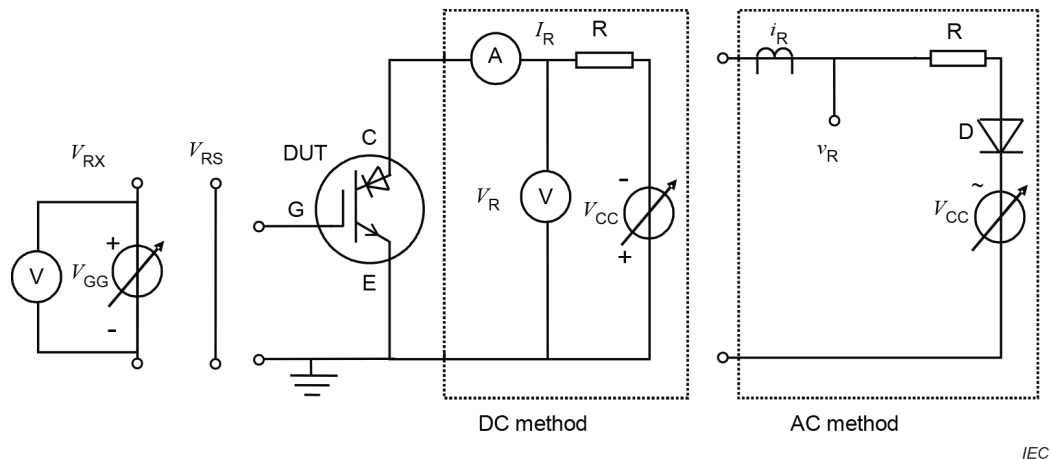
6.2.3 Reverse voltage of a reverse-blocking IGBT (V_{RS} , V_{RX})

6.2.3.1 Purpose

To verify that a reverse-blocking IGBT withstands the rated reverse collector-emitter voltages V_{RS} or V_{RX} under specified conditions.

6.2.3.2 Circuit diagram

The circuit diagram is shown in Figure 3.

**Key**

DUT device under test

D diode for rectifying

Figure 3 – Circuit for testing the reverse voltages V_{RS} , V_{RX} **6.2.3.3 Circuit description**

V_{CC} and V_{GG} are the voltage sources. R is a circuit protection resistor.

6.2.3.4 Test procedure

There are two methods, i.e. the DC method and the AC method with circuits according to Figure 3.

The temperature is set to the specified value. The specified condition between gate and emitter is applied. The reverse collector-emitter voltage is increased until the specified value and the current I_{RS} or I_{RX} is measured with reference to the applied gate conditions.

6.2.3.5 Specified conditions

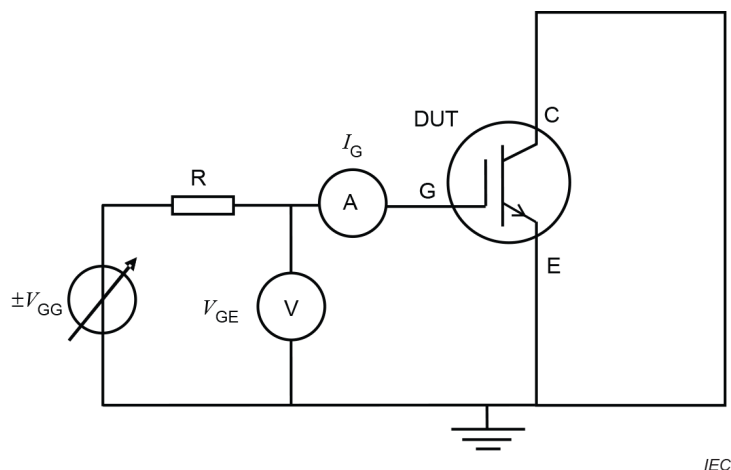
- Reverse collector-emitter voltage V_R .
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- V_{RS} : short-circuit between gate and emitter.
- V_{RX} : gate-emitter voltage V_{GG} .

6.2.4 Gate-emitter voltage with collector-emitter short-circuit ($\pm V_{GES}$)**6.2.4.1 Purpose**

To verify that an IGBT withstands the rated gate-emitter voltage $\pm V_{GE}$ under specified conditions.

6.2.4.2 Circuit diagram

The circuit diagram is shown in Figure 4.



Key

DUT device under test

Figure 4 – Circuit for testing the gate-emitter voltage $\pm V_{GES}$

6.2.4.3 Circuit description

V_{GG} is the voltage source. R is a circuit protection resistor.

6.2.4.4 Test procedure

The gate-emitter voltage V_{GE} is set to the specified value. A protective resistor R is to be provided.

6.2.4.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Gate-emitter leakage current I_{GES} .
- Short-circuit between collector and emitter.

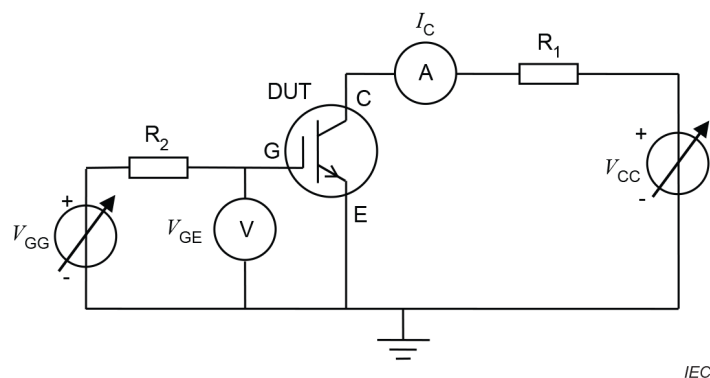
6.2.5 Continuous (direct) collector current (I_C)

6.2.5.1 Purpose

To verify that the collector current capability of an IGBT is not less than the maximum rated value I_C under specified conditions.

6.2.5.2 Circuit diagram

The circuit diagram is shown in Figure 5.

**Key**

DUT device under test

Figure 5 – Circuit for testing collector current**6.2.5.3 Circuit description**

V_{CC} and V_{GG} are the voltage sources. R_1 and R_2 are circuit protection resistors.

6.2.5.4 Test procedure

The temperature (T_a or T_c or T_{vj}) and the gate-emitter voltage are set and kept to the specified values. The supply voltage (V_{CC}) is increased until I_C reaches the specified value. The thermal equilibrium might be reached.

6.2.5.5 Specified conditions

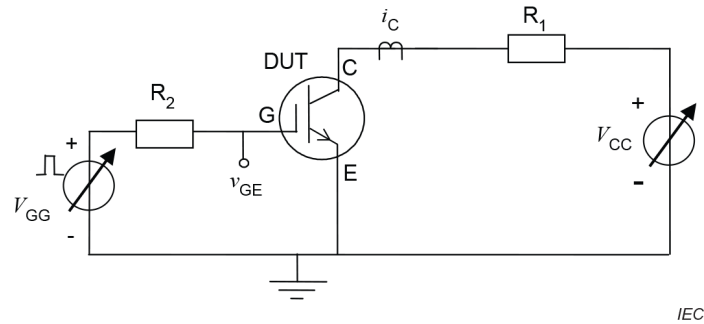
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector current I_C .
- Gate-emitter voltage V_{GE} .

6.2.6 Maximum peak collector current (I_{CRM} and I_{CSM})**6.2.6.1 Purpose**

To verify that the peak collector current capability of an IGBT is not less than the maximum rated value I_{CM} under specified conditions.

6.2.6.2 Circuit diagram

The circuit diagram is shown in Figure 6.



Key

DUT device under test

Figure 6 – Circuit for testing peak collector current

6.2.6.3 Circuit description

V_{CC} is the voltage source and V_{GG} is the gate pulse generator. R_1 and R_2 are circuit protection resistors.

6.2.6.4 Test procedure

The temperature (T_a or T_c or T_{vj}) and the gate-emitter voltage are set and kept at the specified values. The supply voltage (V_{CC}) is increased until I_C reaches the specified value.

6.2.6.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector current I_{CM} .
- Gate-emitter voltage, pulse width and duty cycle for I_{CRM} , pulse width for I_{CSM} .

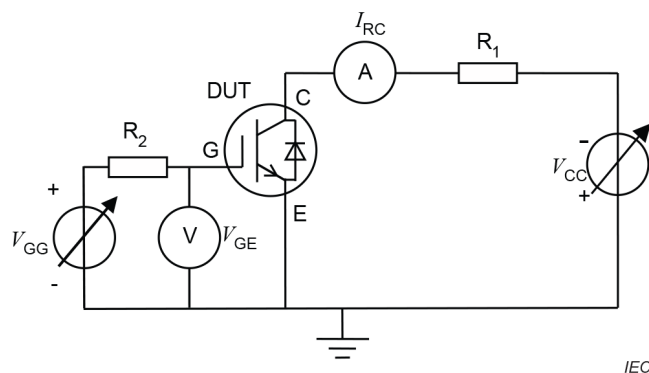
6.2.7 Continuous (direct) reverse-conducting current of a reverse-conducting IGBT (I_{RC})

6.2.7.1 Purpose

To verify that the reverse-conducting current capability of a reverse-conducting IGBT is not less than the maximum rated value I_{RC} under specified conditions.

6.2.7.2 Circuit diagram

The circuit diagram is shown in Figure 7.



Key

DUT device under test

Figure 7 – Circuit for testing reverse-conducting current

6.2.7.3 Circuit description

V_{GG} is the voltage source. The voltage source V_{CC} provides reverse-conducting current. R_1 and R_2 are circuit protection resistors.

6.2.7.4 Test procedure

The temperature (T_a or T_c or T_{vj}) is set and kept to the specified values. The supply voltage (V_{GG}) is set and kept to the specified V_{GE} . The supply voltage (V_{CC}) is increased until I_{RC} reaches the specified value. The thermal equilibrium might be reached.

6.2.7.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Gate-emitter voltage V_{GE} , or short-circuit between gate and emitter ($V_{GE} = 0$ V).
- Reverse-conducting current I_{RC} .

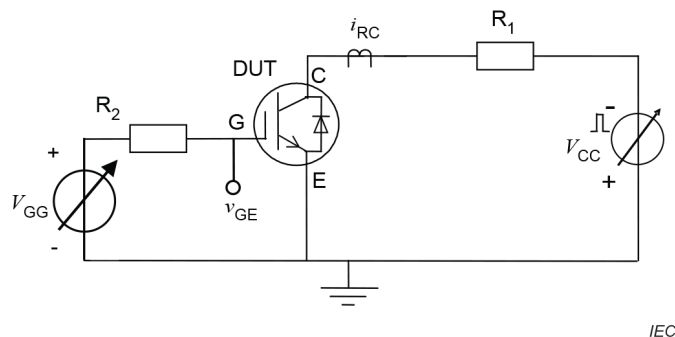
6.2.8 Maximum peak reverse-conducting current of a reverse-conducting IGBT (I_{RCRM} and I_{RCSM})

6.2.8.1 Purpose

To verify that the peak reverse-conducting current capability of a reverse-conducting IGBT is not less than the maximum rated value I_{RCM} under specified conditions.

6.2.8.2 Circuit diagram

The circuit diagram is shown in Figure 8.



Key

DUT device under test

Figure 8 – Circuit for testing peak reverse-conducting current

6.2.8.3 Circuit description

V_{GG} is the voltage source. V_{CC} is the pulse voltage source. R_1 and R_2 are circuit protection resistors.

6.2.8.4 Test procedure

The temperature (T_a or T_c or T_{vj}) is set and kept at the specified values. The supply voltage (V_{GG}) is set and kept to the specified V_{GE} . The supply voltage (V_{CC}) is increased until I_{RCM} reaches the specified value.

6.2.8.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

- Gate-emitter voltage V_{GE} , or short-circuit between gate and emitter ($V_{GE} = 0$ V).
- Peak reverse-conducting current I_{RCM} .
- Pulse width and duty cycle for I_{RCRM} , pulse width for I_{RCSM} .

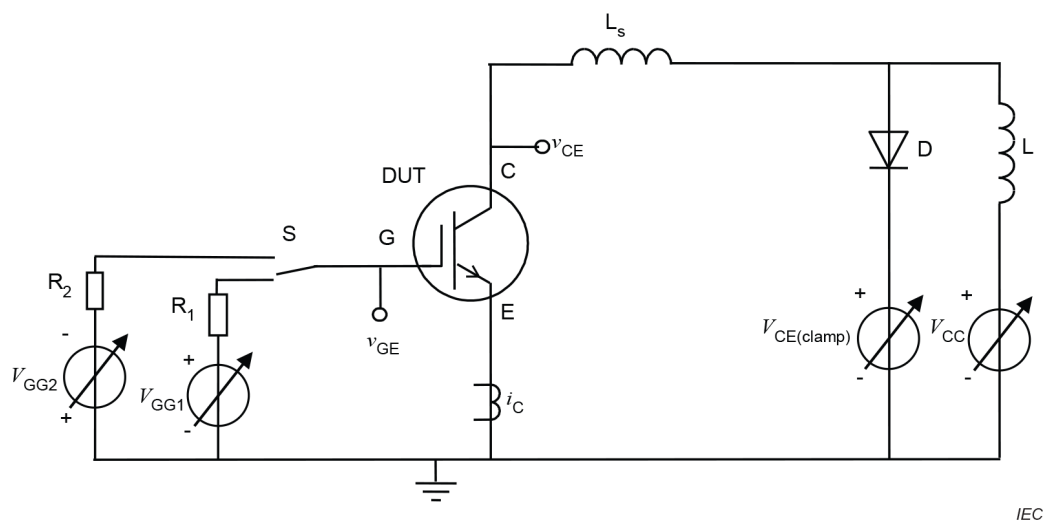
6.2.9 Maximum reverse biased safe operating area (RBSOA)

6.2.9.1 Purpose

To verify that the IGBT operates reliably without failure in RBSOA.

6.2.9.2 Circuit diagram and waveforms

The circuit diagram is shown in Figure 9, and the waveforms are shown in Figure 10.



Key

DUT device under test

D diode for clamping

Figure 9 – Circuit for testing reverse biased safe operating area (RBSOA)

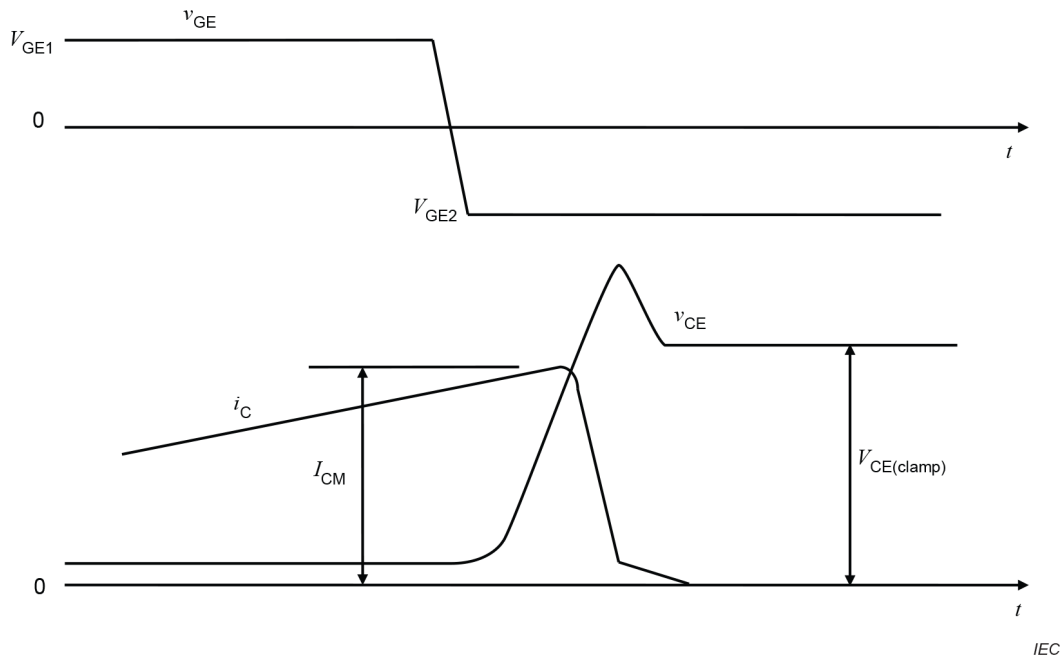


Figure 10 – Waveforms of gate-emitter voltage V_{GE} and collector current I_C during turn-off

6.2.9.3 Circuit description and requirements

The value of load inductance L shall be high enough to maintain the specified $V_{CE(clamp)}$ to the DUT for at least the whole duration of the fall and tail time. V_{CC} is a low voltage to supply the on-state collector current I_C . $V_{CE(clamp)}$ shall be capable of carrying a reverse current equal to I_C , while maintaining the specified voltage. V_{GG1} and V_{GG2} are DC voltage sources. R_1 and R_2 are gate resistors. S is the switch for forward or reverse gate bias. L_s is an inductor representing the maximum permitted unclamped stray inductance.

6.2.9.4 Test procedure

The DUT is turned off at the specified I_C .

V_{CE} and I_C are monitored. The DUT has to turn off I_C and withstand $V_{CE} = V_{CE(clamp)}$.

NOTE Collector-emitter peak voltage $V_{CEM} < V_{(BR)CE^{**}}$.

6.2.9.5 Specified conditions

- Collector current I_C .
- Gate-emitter voltage V_{GE1} and V_{GE2} .
- Collector-emitter voltage $V_{CE(clamp)}$.
- Single-pulse or repetition rate.
- Inductance L .
- Value of unclamped stray inductance L_s .
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Gate resistors R_1 , R_2 .

6.2.10 Maximum short-circuit safe operating area (SCSOA)

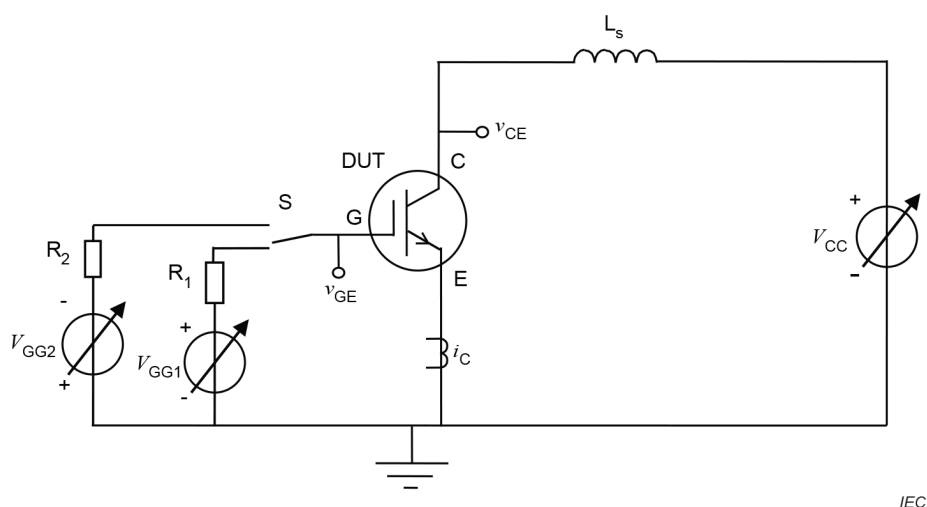
6.2.10.1 Purpose

To verify that the IGBT operates reliably without failure during a load short-circuit condition. Two types of load short-circuit can occur. The first one is to switch the IGBT on to an existing load short-circuit. Another one is when the IGBT is already in the on-state $V_{CE} = V_{CEsat}$, and then the load short-circuit occurs. Both methods shall be applied.

6.2.10.2 Maximum short-circuit safe operating area 1 (SCSOA1)

6.2.10.2.1 Circuit diagram and waveforms

The circuit diagram is shown in Figure 11, and the waveforms are shown in Figure 12.



Key

DUT device under test

Figure 11 – Circuit for testing safe operating pulse width at load short-circuit (SCSOA1)

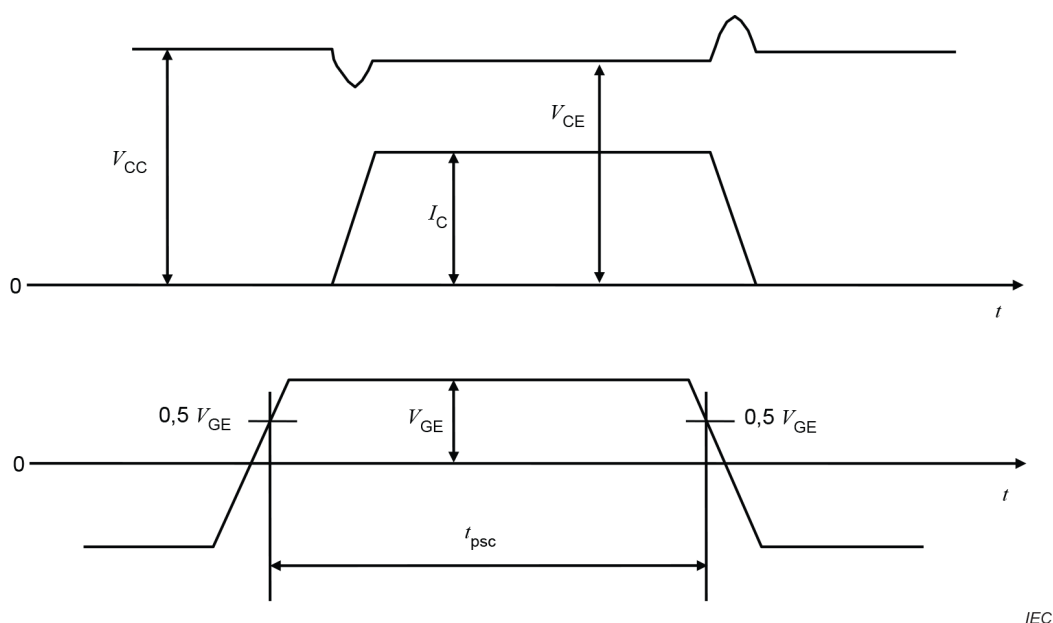


Figure 12 – Waveforms of gate-emitter voltage V_{GE} , collector current I_C and collector-emitter voltage V_{CE} during load short-circuit condition SCSOA1

6.2.10.2.2 Circuit description

V_{CC} is the DC voltage source. V_{GG} is the gate pulse generator. R_1 and R_2 are the gate resistors. L_s represents the maximum permitted stray inductance that shall be low enough to ensure that maximum short-circuit current is reached within the first 25 % of the gate pulse width t_{psc} .

6.2.10.2.3 Test procedure

Set the temperature to the specified value. Apply the specified off-state gate-emitter voltage. Set the collector-emitter voltage to the specified value. Apply the specified gate-emitter on-state pulse. I_C , V_{CE} and V_{GE} are monitored in order to see whether the IGBT turns on and off correctly.

6.2.10.2.4 Specified conditions

- Collector-emitter voltage V_{CE} .
- On- and off-state gate-emitter voltage V_{GE} .
- Gate pulse width t_{psc} .
- Gate resistors R_1 , R_2 .
- Value of stray inductance L_s .
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

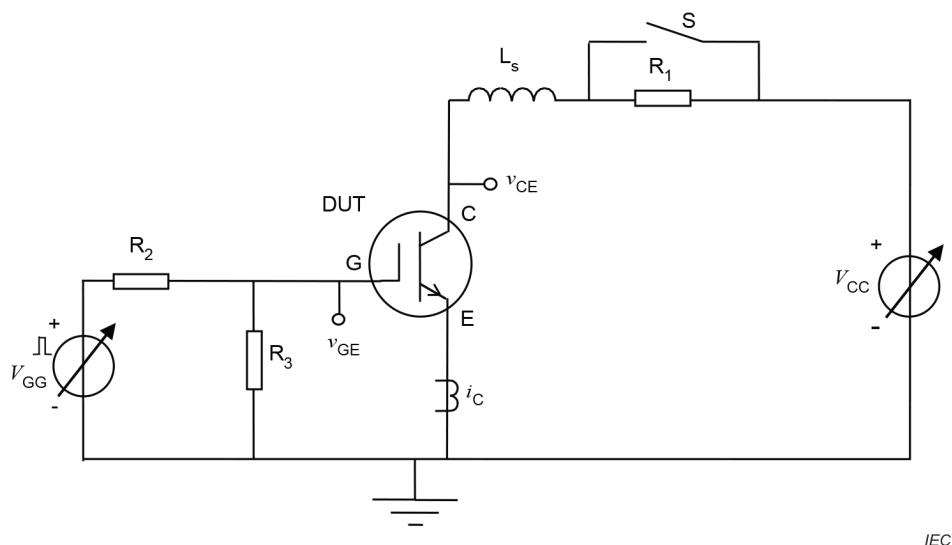
6.2.10.3 Maximum short-circuit safe operating area 2 (SCSOA2)

6.2.10.3.1 Features of the operation

The gate voltage increases from the gate-emitter voltage V_{GE} by the dv_{CE}/dt of the collector-emitter voltage V_{CE} . It induces a fast increase of the collector current and high peak energy, as shown in Figure 14.

6.2.10.3.2 Circuit diagram and operating waveforms

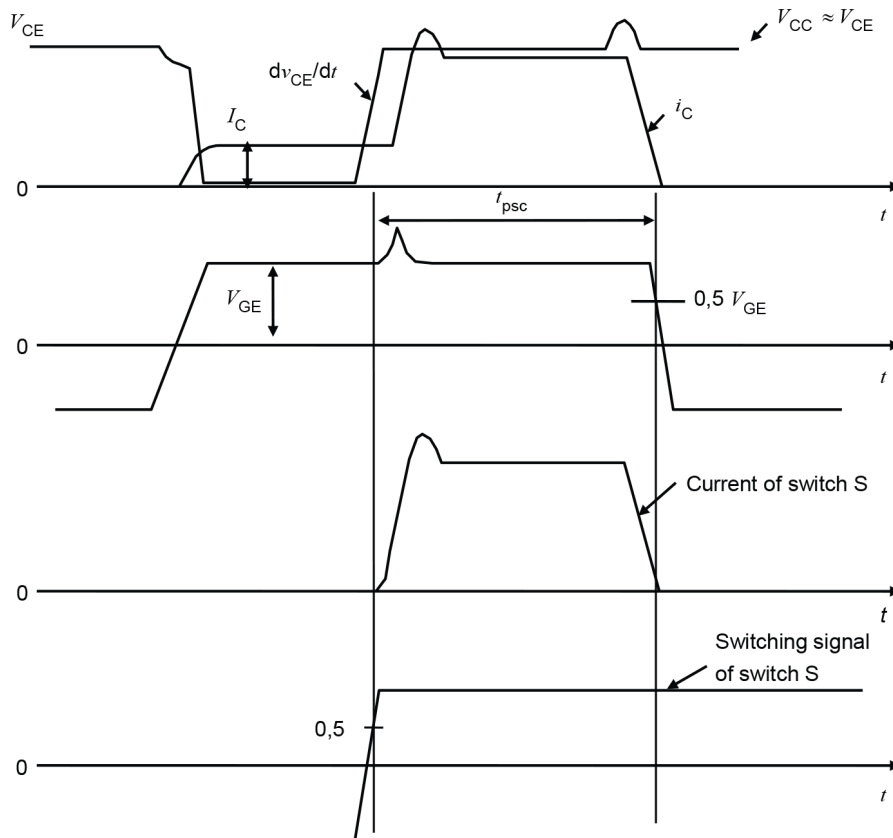
The circuit diagram is shown in Figure 13, and the waveforms are shown in Figure 14.



Key

DUT device under test

Figure 13 – Circuit for testing short-circuit safe operating area 2 (SCSOA2)



IEC

Figure 14 – Waveforms during SCSOA2

6.2.10.3.3 Circuit description

V_{CC} is the DC voltage source. V_{GG} is the gate pulse generator. R_1 is a resistor for the defining collector current prior to short-circuit. R_2 and R_3 are gate resistors. L_s is an inductor representing the maximum permitted unclamped stray inductance. Switch S in the circuit should have much lower impedance compared to the device under test (DUT). The type name or characteristics of switch S should be specified. The current capability of switch S should be substantially larger than the expected short-circuit current of the DUT.

6.2.10.3.4 Test procedure

Set the temperature to the specified value. Apply the specified off-state gate-emitter voltage. Set the collector-emitter voltage to the specified value. Apply the specified gate-emitter on-state pulse. S is opened until the DUT is turned-on and is closed after a steady state collector current I_C is reached. I_C , V_{CE} , V_{GE} and the switching signal of the switch S are monitored in order to see whether the IGBT turns on and off correctly.

6.2.10.3.5 Specified conditions

- Collector current prior to short-circuit $I_C (= V_{CC} / R_1)$.
- Collector-emitter voltage $V_{CE} \approx V_{CC}$.
- On- and off-state gate-emitter voltage V_{GE} .
- Time between turning-on of S and turning-off of V_{GE} t_{psc} .
- Gate resistors R_2 , R_3 .
- Value of unclamped stray inductance L_s .
- Type name or characteristics of switch S, if restrictive.

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

6.3 Methods of measurement

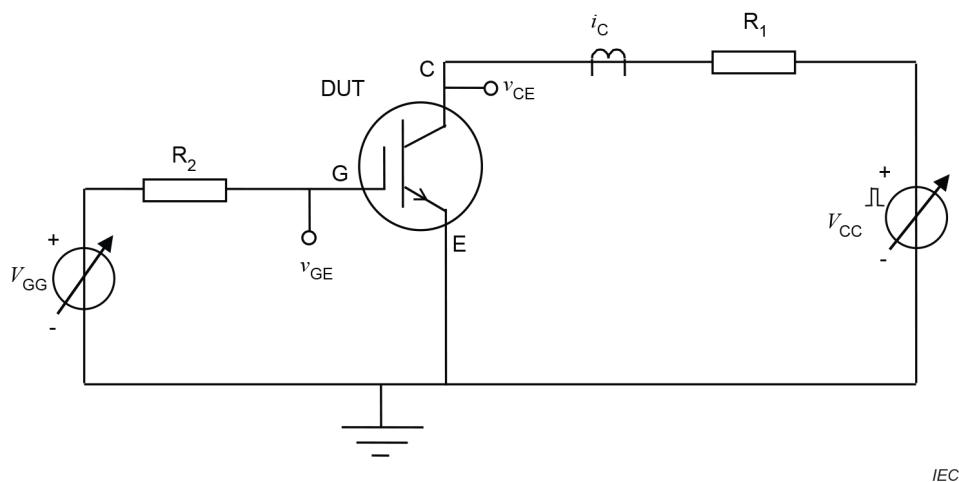
6.3.1 Collector-emitter saturation voltage (V_{CEsat})

6.3.1.1 Purpose

To measure the collector-emitter saturation voltage of an IGBT under specified conditions.

6.3.1.2 Circuit diagram

The circuit diagram is shown in Figure 15.



Key

DUT device under test

Figure 15 – Circuit for measuring the collector-emitter saturation voltage V_{CEsat}

6.3.1.3 Circuit description

V_{GG} is the gate voltage source. The voltage source V_{CC} in combination with R_1 provides constant collector current pulses, which are long enough that complete saturation of the DUT is reached. R_1 and R_2 are circuit protection resistors.

6.3.1.4 Precautions

No significant heat dissipation shall occur in the IGBT during the measurement.

6.3.1.5 Measurement procedure

The temperature is set to the specified value, adapted to the specified values in the gate-emitter voltage and the collector current. The collector-emitter saturation voltage $V_{CE} = V_{CEsat}$ is measured.

6.3.1.6 Specified conditions

- Virtual junction temperature T_{vj} .
- Gate-emitter voltage V_{GE} .
- Collector current I_C .

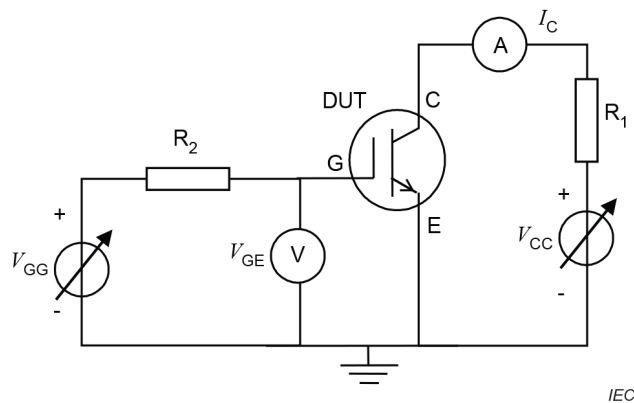
6.3.2 Gate-emitter threshold voltage ($V_{GE(th)}$)

6.3.2.1 Purpose

To measure the gate-emitter threshold voltage of an IGBT under specified conditions.

6.3.2.2 Circuit diagram

The circuit diagram is shown in Figure 16.



Key

DUT device under test

Figure 16 – Circuit for measuring the gate-emitter threshold voltage

6.3.2.3 Circuit description

V_{CC} and V_{GG} are the voltage sources. R_1 and R_2 are circuit protection resistors.

6.3.2.4 Measurement procedure

The device temperature and the collector-emitter voltage are set to the specified value. The gate-emitter voltage V_{GE} is increased until the specified collector current I_C is reached. The gate-emitter voltage at this current is measured.

6.3.2.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector-emitter voltage V_{CE} .
- Collector current I_C .

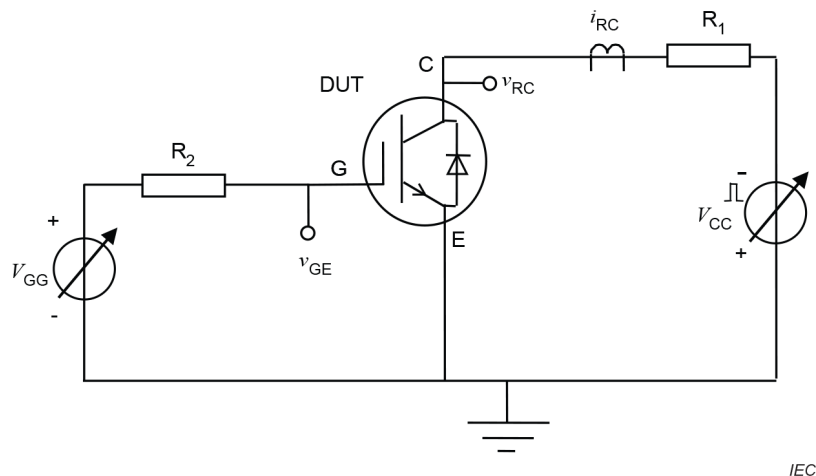
6.3.3 Reverse-conducting voltage of a reverse-conducting IGBT (V_{RC})

6.3.3.1 Purpose

To measure the reverse-conducting voltage of a reverse-conducting IGBT under specified conditions.

6.3.3.2 Circuit diagram

The circuit diagram is shown in Figure 17.

**Key**

DUT device under test

Figure 17 – Circuit for measuring the reverse-conducting voltage V_{RC} **6.3.3.3 Circuit description**

V_{GG} is the gate voltage source. The voltage source V_{CC} in combination with R_1 provides constant collector current pulses, which are long enough that complete saturation of the DUT is reached. R_1 and R_2 are circuit protection resistors.

6.3.3.4 Precautions

No significant heat dissipation shall occur in the reverse-conducting IGBT during the measurement.

6.3.3.5 Measurement procedure

The temperature is set to the specified value, adapted to the specified values in the gate-emitter voltage and the reverse-conducting current. The reverse-conducting voltage V_{RC} is measured.

6.3.3.6 Specified conditions

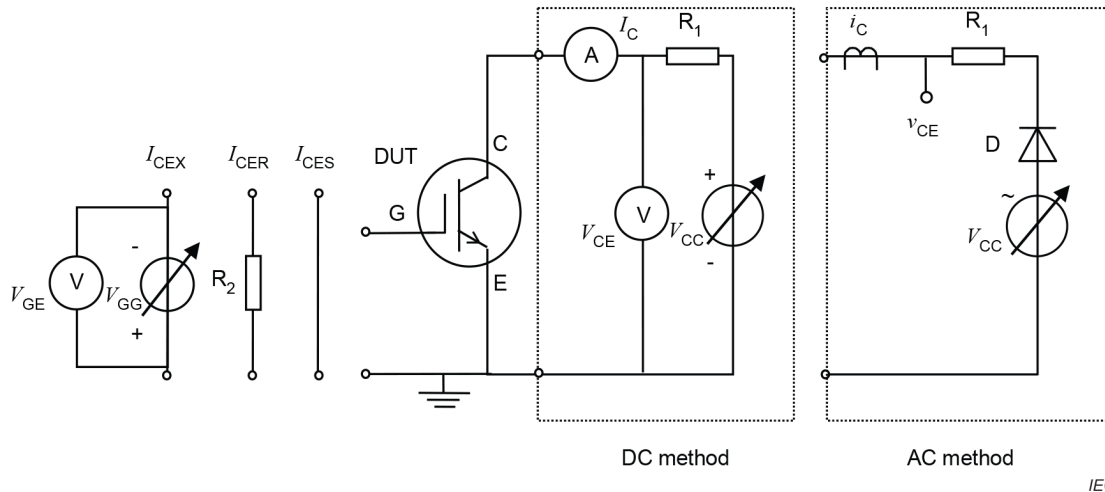
- Virtual junction temperature T_{vj} .
- Gate-emitter voltage V_{GE} , or short-circuit between gate and emitter ($V_{GE} = 0$ V).
- Reverse-conducting current I_{RC} .

6.3.4 Collector cut-off current (I_{CES} , I_{CER} , I_{CEX})**6.3.4.1 Purpose**

To measure the collector cut-off current of an IGBT under specified conditions.

6.3.4.2 Circuit diagram

The circuit diagram is shown in Figure 18.



Key

DUT device under test

D diode for rectifying

Figure 18 – Circuit for measuring the collector cut-off current

6.3.4.3 Circuit description

V_{CC} and V_{GG} are the voltage sources. R_1 is a circuit protection resistor. R_2 is a resistor connected between gate and emitter.

6.3.4.4 Measurement procedure

There are two methods, i.e. the DC method and the AC method, as shown in Figure 18. The temperature is set to the specified value. The voltage V_{CE} is increased until it reaches the specified value. The cut-off currents I_{CEX} , I_{CER} , I_{CES} are read on the ampere meter or the current probe.

6.3.4.5 Specified conditions

- V_{CC} in the AC method with a frequency of 50 Hz or 60 Hz unless otherwise specified.
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector-emitter voltage V_{CE} .
- I_{CER} : resistor R_2 connected between gate and emitter.
- I_{CES} : short-circuit between gate and emitter.
- I_{CEX} : gate-emitter voltage.

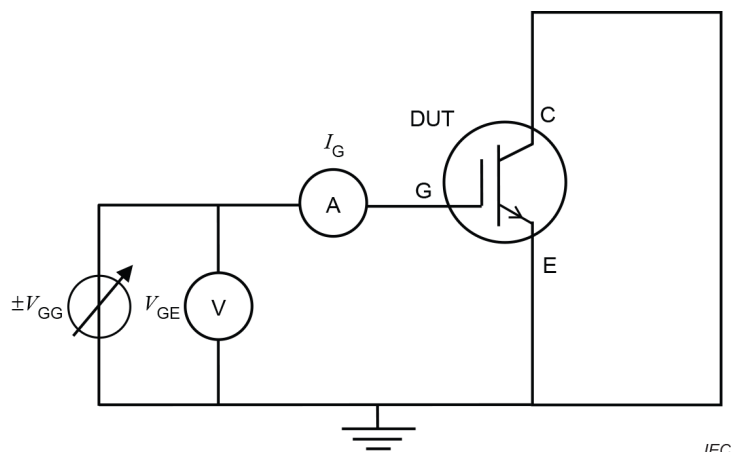
6.3.5 Gate leakage current (I_{GES})

6.3.5.1 Purpose

To measure the gate-emitter leakage current of an IGBT with the collector-emitter short-circuited.

6.3.5.2 Circuit diagram

The circuit diagram is shown in Figure 19.

**Key**

DUT device under test

Figure 19 – Circuit for measuring the gate leakage current

6.3.5.3 Circuit description

V_{GG} is the voltage source.

6.3.5.4 Measurement procedure

The collector and emitter terminals are shorted. The gate-emitter voltage is set to the specified value. The gate-emitter leakage current is measured.

6.3.5.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Gate-emitter voltage V_{GE} .

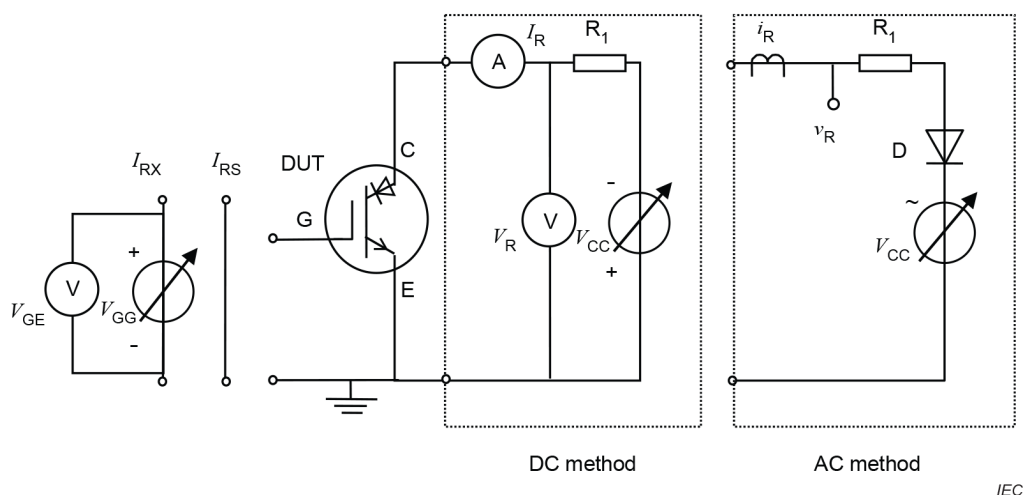
6.3.6 Reverse current of a reverse-blocking IGBT (I_{RS} , I_{RX})

6.3.6.1 Purpose

To measure the reverse current of a reverse-blocking IGBT under specified conditions.

6.3.6.2 Circuit diagram

The circuit diagram is shown in Figure 20.



Key

DUT device under test

D diode for rectifying

Figure 20 – Circuit for measuring the reverse current

6.3.6.3 Circuit description

V_{CC} and V_{GG} are the voltage sources. R_1 is a circuit protection resistor.

6.3.6.4 Measurement procedure

There are two methods, i.e. the DC method and the AC method, as shown in Figure 20. The temperature is set to the specified value. The voltage V_R is increased until it reaches the specified value. The reverse currents I_{RS} , I_{RX} are read on the ampere meter or the current probe.

6.3.6.5 Specified conditions

- V_{CC} in the AC method with a frequency of 50 Hz or 60 Hz unless otherwise specified.
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Reverse collector-emitter voltage V_R .
- I_{RS} : short-circuit between gate and emitter.
- I_{RX} : gate-emitter voltage V_{GG} .

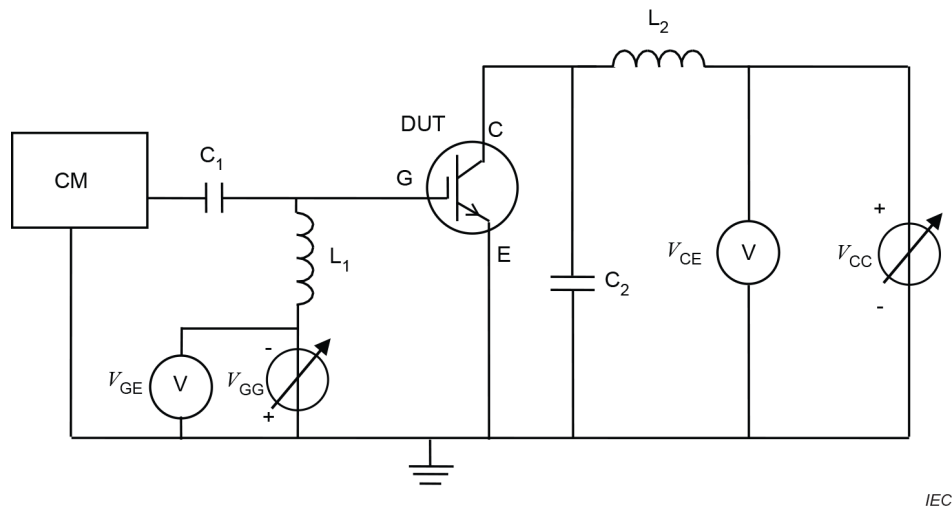
6.3.7 Input capacitance (C_{ies})

6.3.7.1 Purpose

To measure the input capacitance of an IGBT under specified conditions.

6.3.7.2 Circuit diagram

The circuit diagram is shown in Figure 21.

**Key**

DUT device under test

Figure 21 – Circuit for measuring the input capacitance**6.3.7.3 Circuit description and requirements**

CM is a capacitance meter. V_{CC} and V_{GG} are adjustable DC voltage sources. Capacitances C_1 and C_2 should present a short-circuit at the measurement frequency, and inductance L_1 and L_2 are to decouple the measurement signal from the DC voltage sources, satisfying the following conditions:

$$1/\omega L_1 \ll |y_{ie}| \text{ and } \omega C_1 \gg |y_{ie}|$$

$$1/\omega L_2 \ll |y_{oe}| \text{ and } \omega C_2 \gg |y_{oe}|$$

NOTE 1 $|y_{ie}|$ is the small-signal value of the short-circuit input admittance in common-emitter configuration.

NOTE 2 $|y_{oe}|$ is the small-signal value of the short-circuit output admittance in common-emitter configuration.

6.3.7.4 Measurement procedure

The CM is set to the specified frequency without the IGBT. The IGBT is inserted into the test socket. The temperature is set to the specified value. The gate-emitter voltage V_{GE} and the collector-emitter voltage V_{CE} are set to their specified values. Capacitance C_{ies} can be read on the CM.

6.3.7.5 Specified conditions

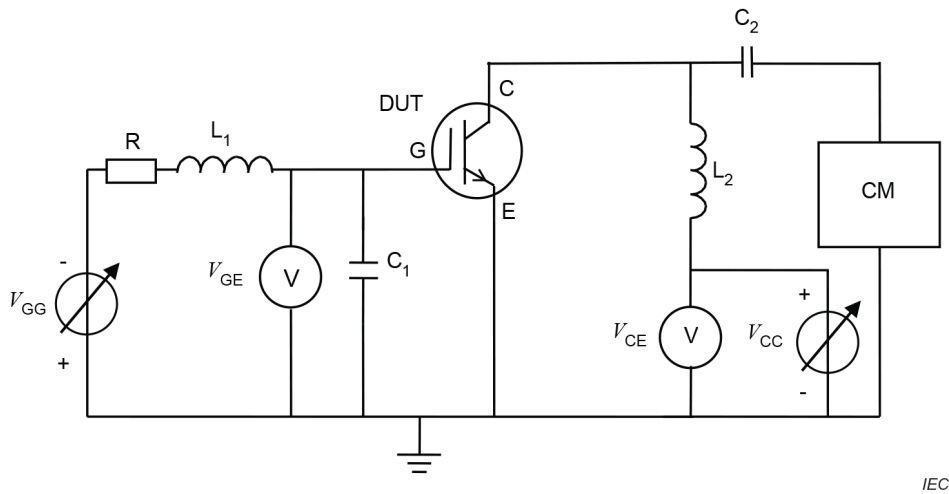
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector-emitter voltage V_{CE} .
- Gate-emitter voltage V_{GE} .
- Measurement frequency f .

6.3.8 Output capacitance (C_{oes})**6.3.8.1 Purpose**

To measure the output capacitance of an IGBT under specified conditions.

6.3.8.2 Circuit diagram

The circuit diagram is shown in Figure 22.



Key

DUT device under test

Figure 22 – Circuit for measuring the output capacitance

6.3.8.3 Circuit description and requirement

CM is a capacitance meter. V_{CC} and V_{GG} are adjustable DC voltage sources. R shall not be too high. Capacitances C_1 and C_2 should present short-circuit at the measurement frequency, inductance L_1 and L_2 are to decouple the measurement signal from the DC voltage sources, satisfying the following conditions:

$$1/\omega L_1 \ll |y_{ie}| \text{ and } \omega C_1 \gg |y_{ie}|$$

$$1/\omega L_2 \ll |y_{oe}| \text{ and } \omega C_2 \gg |y_{oe}|$$

NOTE 1 $|y_{ie}|$ is small-signal value of the short-circuit input admittance in the common-emitter configuration.

NOTE 2 $|y_{oe}|$ is small-signal value of the short-circuit output admittance in the common-emitter configuration.

6.3.8.4 Measurement procedure

The CM is set to the specified frequency without the IGBT. The IGBT is inserted into the test socket. The temperature is set to the specified value. The gate-emitter voltage V_{GE} and the collector-emitter voltage V_{CE} are set to their specified values respectively. Capacitance C_{oes} can be read on the CM.

6.3.8.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector-emitter voltage V_{CE} .
- Gate-emitter voltage V_{GE} .
- Measurement frequency f .

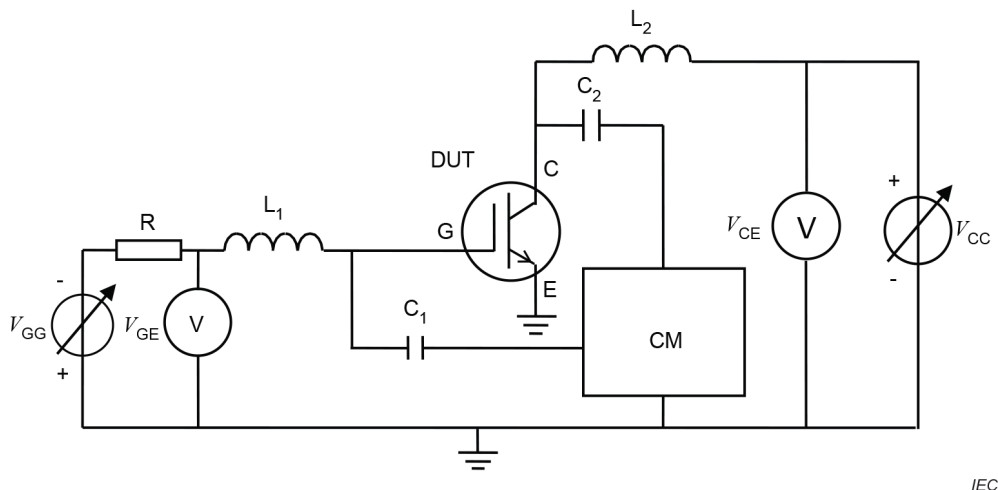
6.3.9 Reverse transfer capacitance (C_{res})

6.3.9.1 Purpose

To measure the reverse transfer capacitance of an IGBT under specified conditions.

6.3.9.2 Circuit diagram

The circuit diagram is shown in Figure 23.



Key

DUT device under test

Figure 23 – Circuit for measuring the reverse transfer capacitance

6.3.9.3 Circuit description and requirement

CM is a capacitance meter. Capacitances C_1 and C_2 shall form an adequate short-circuit for the test frequency. R shall not be too high. Inductance L_1 and L_2 are to decouple the measurement signal from the DC voltage sources. V_{GG} and V_{CC} are adjustable DC voltage sources.

6.3.9.4 Measurement procedure

The CM is set to the specified frequency without the IGBT. The IGBT is inserted into the test socket. The temperature is set to the specified value. The gate-emitter voltage V_{GE} and the collector-emitter voltage V_{CE} are set to their specified value. Capacitance C_{res} can be read on the CM.

6.3.9.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector-emitter voltage V_{CE} .
- Gate-emitter voltage V_{GE} .
- Measurement frequency f .

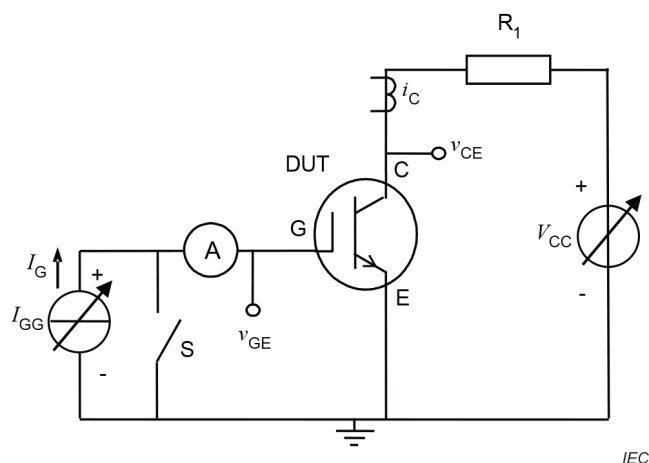
6.3.10 Gate charge (Q_G)

6.3.10.1 Purpose

To measure the gate charge of an IGBT under specified conditions.

6.3.10.2 Circuit diagram and waveforms

The circuit diagram is shown in Figure 24, and the waveforms are shown in Figure 25.



Key

DUT device under test

S switch

Figure 24 – Circuit for measuring the gate charge

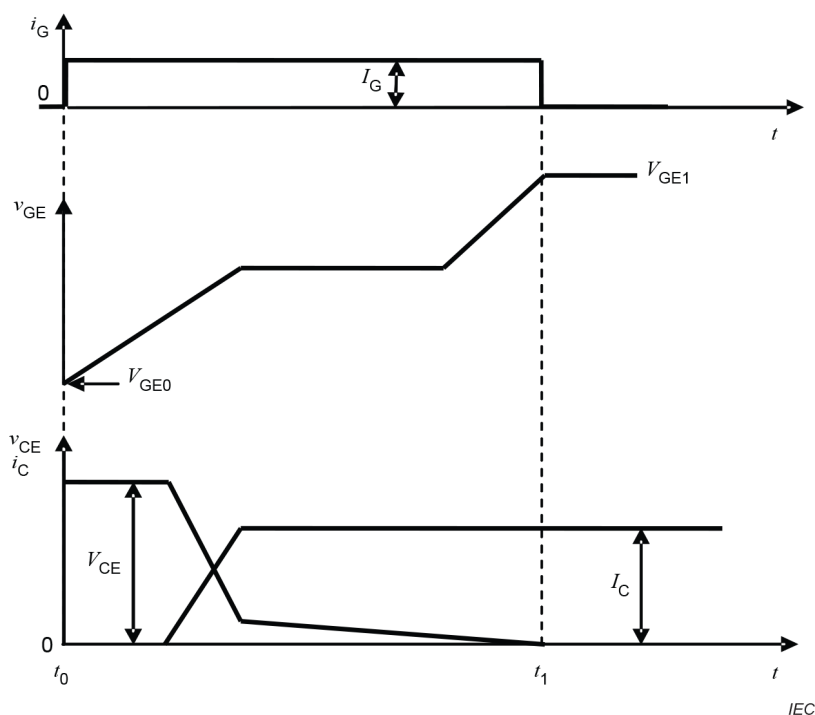


Figure 25 – Basic gate charge waveform

6.3.10.3 Circuit description

V_{CC} is the voltage source. I_{GG} is the current source. R_1 is a circuit protection resistor.

6.3.10.4 Measurement procedure

The gate is fed with a constant current I_G until the specified gate-emitter voltage is reached. V_{CE} and V_{GE} are monitored from zero t_0 to t_1 . Then, the total gate charge can be calculated as follows:

$$Q_G = \int_{t_0}^{t_1} i_G(t) dt = I_G \times (t_1 - t_0)$$

6.3.10.5 Specified conditions

- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .
- Collector current I_C .
- Collector-emitter voltage V_{CE} .
- V_{GE0} at t_0 and V_{GE1} at t_1 .

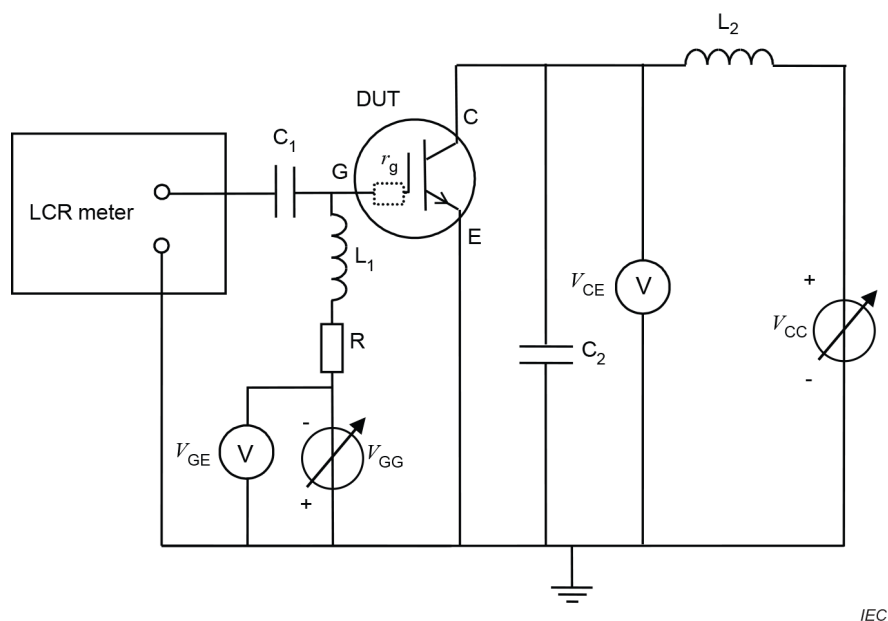
6.3.11 Internal gate resistance (r_g)

6.3.11.1 Purpose

To measure the internal gate resistance of an IGBT, under specified conditions.

6.3.11.2 Circuit diagram

The circuit diagram is shown in Figure 26.



Key

DUT device under test

Figure 26 – Circuit for measuring the internal gate resistance

6.3.11.3 Circuit description and requirements

V_{CC} and V_{GG} are adjustable DC voltage sources. R is an external gate resistor. An LCR meter is used. Capacitances C_1 and C_2 should present a short-circuit at the measurement frequency, and inductance L_1 and L_2 are to decouple the measurement signal from the DC voltage sources, satisfying the following conditions:

$$1/\omega L_1 \ll |y_{ie}| \text{ and } \omega C_1 \gg |y_{ie}|$$

$$1/\omega L_2 \ll |y_{oe}| \text{ and } \omega C_2 \gg |y_{oe}|$$

NOTE 1 $|y_{ie}|$ is the small-signal value of the short-circuit input admittance in the common-emitter configuration.

NOTE 2 $|y_{oe}|$ is the small-signal value of the short-circuit output admittance in the common-emitter configuration.

6.3.11.4 Measurement procedure

The collector-emitter voltage V_{CE} and gate-emitter voltage V_{GE} of the DUT are set to the specified values and then the internal gate resistance r_g is measured by the LCR meter in series capacitance/resistance mode.

6.3.11.5 Specified conditions

- Collector-emitter voltage V_{CE} .
- Gate-emitter voltage V_{GE} .
- Measuring frequency f .
- Ambient or case or virtual junction temperature T_a or T_c or T_{vj} .

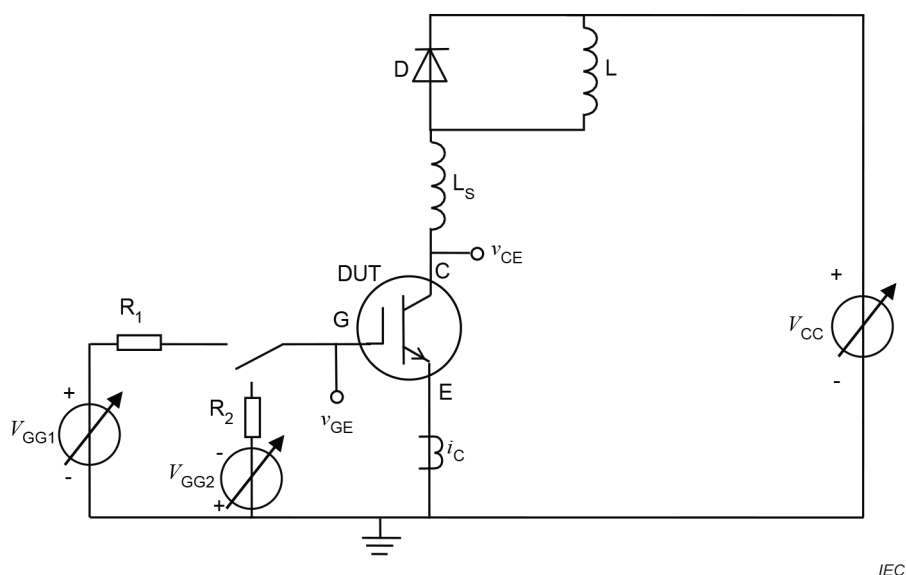
6.3.12 Turn-on times ($t_{d(on)}$, t_r , t_{on}) and turn-on energy (E_{on})

6.3.12.1 Purpose

To measure the turn-on times $t_{d(on)}$, t_r , t_{on} and turn-on energy E_{on} of an IGBT under specified conditions with inductive load.

6.3.12.2 Circuit diagram and waveforms

The circuit diagram is shown in Figure 27, and the waveforms are shown in Figure 28.



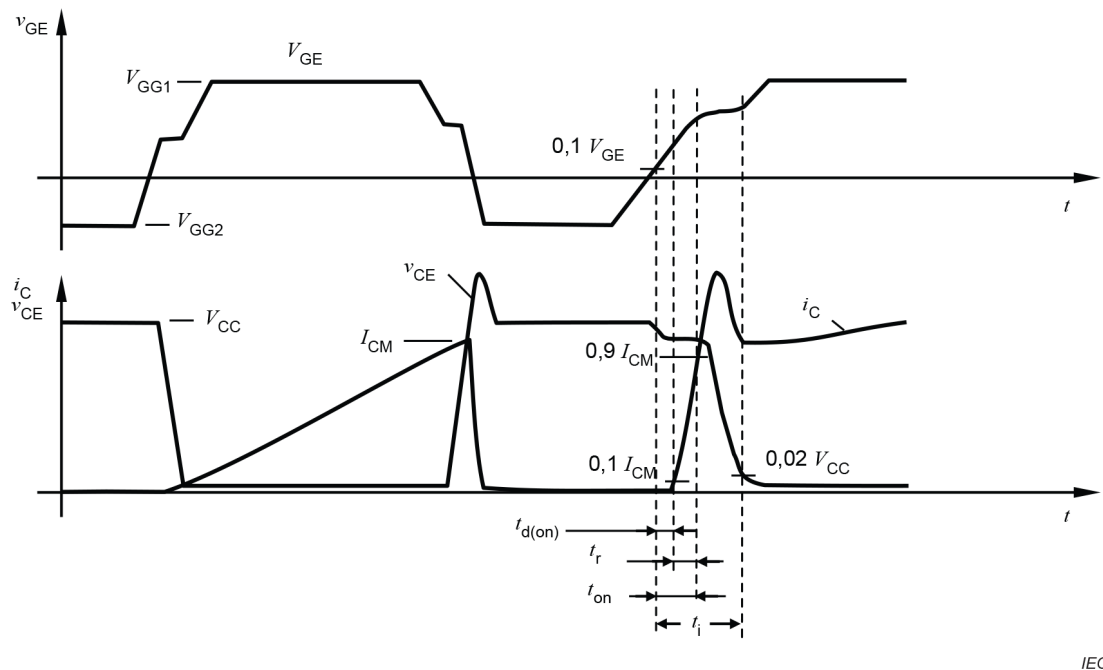
Key

DUT device under test

Figure 27 – Circuit for measuring turn-on times and energy

6.3.12.3 Circuit description and requirements

V_{GG1} , V_{GG2} and V_{CC} are voltage sources. R_1 and R_2 are gate resistors. D is a freewheeling diode for the current in the inductance L.



IEC

Figure 28 – Waveforms during turn-on times

6.3.12.4 Measurement procedure

The gate voltage levels V_{GG1} and V_{GG2} and the supply voltage V_{CC} are set to the specified values. The IGBT is turned on and turned off twice and then the second turn-on is observed. During the first pulse the current is increased to the specified level. The inductance L has to be large enough to keep the current constant during the freewheeling interval. The collector current I_C , the gate voltage V_{GE} and collector-emitter voltage V_{CE} are monitored simultaneously.

E_{on} is the integral of $v_{CE} \times i_C \times dt$. Integral time t_i starts from the 10 % rise point of V_{GE} and ends at the specified low V_{CE} point, the 2 % point of V_{CC} . The turn-on power dissipation is the product of the switching frequency and the turn-on energy per pulse as determined by the integration.

6.3.12.5 Specified conditions

- Ambient or case or virtual junction temperature of the IGBT and the diode T_a or T_c or T_{vj} .
- Collector-emitter voltage V_{CE} (supply voltage V_{CC}).
- Collector current I_C just before 1st turn-off (I_{CM}).
- Gate voltage $-V_{GE}$ (V_{GG2}) before and $+V_{GE}$ (V_{GG1}) after turn-on.
- Gate resistor R_1 ($R_{G(on)}$).
- Value of stray inductance L_s .
- Characteristics of freewheeling diode.

If there is a freewheeling diode in the same package with the IGBT, this type of diode should be used for the measurement.

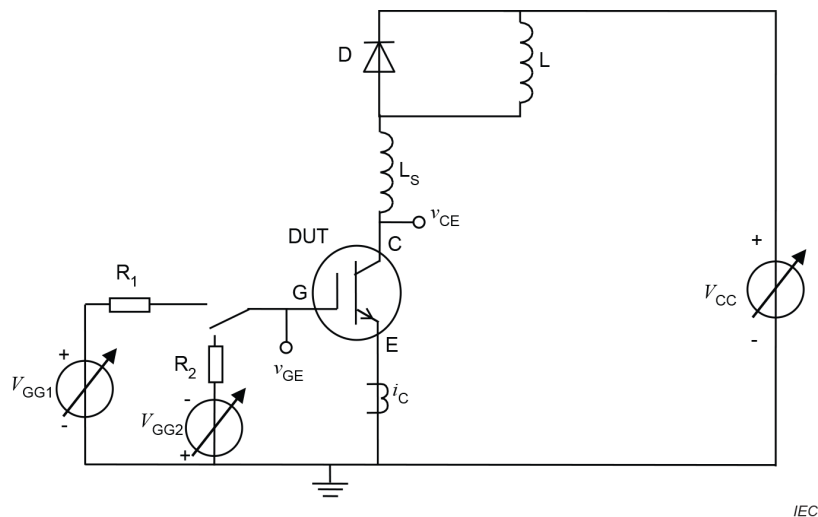
6.3.13 Turn-off times ($t_{d(off)}$, t_f , t_{off} , t_z) and turn-off energy (E_{off})

6.3.13.1 Purpose

To measure the turn-off times $t_{d(off)}$, t_f , t_{off} , t_z and turn-off energy E_{off} of an IGBT under specified conditions with inductive load.

6.3.13.2 Circuit diagram and waveforms

The circuit diagram is shown in Figure 29, and the waveforms are shown in Figure 30.



Key

DUT device under test

Figure 29 – Circuit for measuring turn-off times and energy

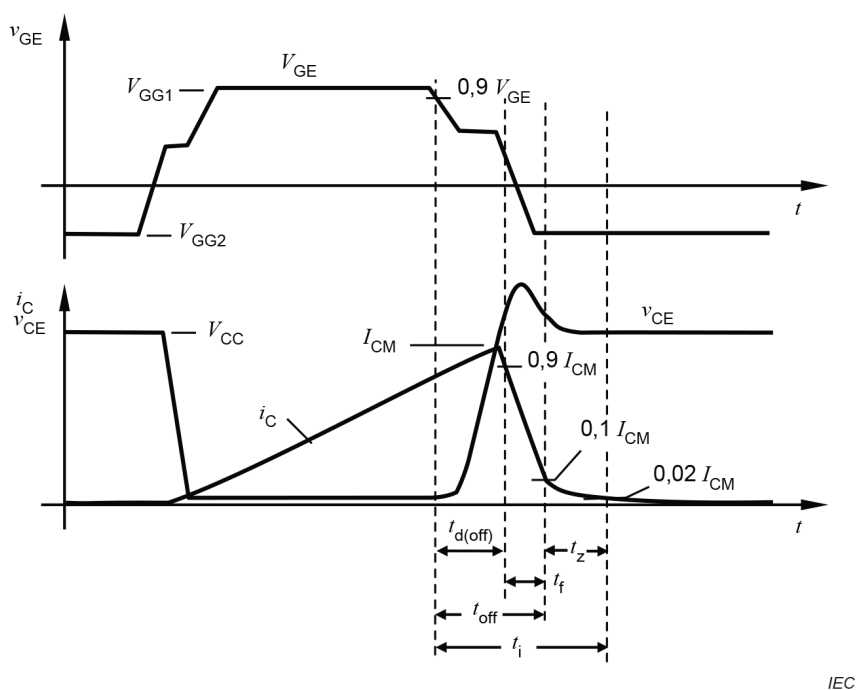


Figure 30 – Waveforms during turn-off times