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NORME INTERNATIONALE

Semiconductor devices – Mechanical and climatic test methods – Part 29: Latch-up test

Dispositifs à semiconducteurs – Méthodes d'essai mécaniques et climatiques – Partie 29: Essai de verrouillage

IEC 60749-29:2011

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

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International Standard IEC 60749-29 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2003 and constitutes a technical revision. The significant changes with respect to the previous edition include:

– a number of minor technical changes;
– the addition of two new annexes covering the testing of special pins and temperature calculations.

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2083/FDIS	47/2090/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

1 Scope and object

This part of IEC 60749 covers the I-test and the overvoltage latch-up testing of integrated circuits.

This test is classified as destructive.

The purpose of this test is to establish a method for determining integrated circuit (IC) latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are used in determining product reliability and minimizing "no trouble found" (NTF) and "electrical overstress" (EOS) failures due to latch-up.

This test method is primarily applicable to CMOS devices. Applicability to other technologies must be established.

The classification of latch-up as a function of temperature is defined in 3.1 and the failure level criteria are defined in 3.2

2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

2.1
cool-down time
period of time between successive applications of trigger pulses or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse (See Figures 4, 5, and 8 and Table 2.)

2.2
device under test
DUT
semiconductor product subjected to latch-up test

2.3
ground
GND
common or zero-potential pin(s) of the DUT

NOTE 1 Ground pins are not latch-up tested.

NOTE 2 A ground pin is sometimes called V_{ss}.

2.4
input pins
all address, data-in control, V_{ref} and similar pins

2.5
I/O (bi-directional) pins
device pins that can be made to operate as an input or output or in a high-impedance state

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2.6
I_{supply}
total supply current in each V_{supply} pin (or pin group) with the DUT biased as indicated in Table 1

2.7
I-test
latch-up test that supplies positive and negative current pulses to the pin under test

2.8
latch-up
state in which a low-impedance path resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition

NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

2.9
logic-high
level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states

NOTE 1 For digital devices, a voltage level equal to V_{supply} is used for latch-up testing, except where otherwise specified in the relevant specification.

NOTE 2 For non-digital devices, V_{supply} voltage level or the maximum operating voltage that can be applied to that pin as defined in the relevant specification may be used for latch-up testing.

2.10
logic-low
level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states

NOTE 1 For digital devices, ground voltage level is used for latch-up testing, except where specified in the relevant specification.

NOTE 2 For non-digital devices, ground voltage level or the minimum operating voltage that can be applied to that pin as defined in the relevant specification may be used for latch-up testing.

2.11
maximum V_{supply}
maximum operating voltage for operation within performance specifications

NOTE 1 The maximum voltage is not the absolute maximum voltage beyond which permanent damage is likely.

NOTE 2 Maximum refers to the magnitude of V_{supply} and can be either positive or negative.

2.12
no connect pin
pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device

NOTE All “no connect” pins should be left in an open (floating) state during latch-up testing.

2.13
nominal I_{supply} (I_{nom})
measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the test temperature as defined in Clause 5 and Table 1

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2.14
output pin
device pin that generates a signal or voltage level as a normal function during the normal operation of the device

NOTE Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

2.15
preconditioned pin
device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT

2.16
testing of dynamic devices
latch-up trigger testing of a device in a known stable state, at the minimum-rated clock frequency applied to the device (see 5.2.3 for specified conditions)

2.17
test condition
test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to the DUT during the latch-up test

2.18
timing-related input pin
pin such as clock crystal oscillator, charge pump circuit, etc., required to place the DUT in a normal operating mode

NOTE Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

2.19
trigger pulse
positive or negative current pulse (I-Test) or voltage pulse (V_{supply} overvoltage test) applied to any pin under test in an attempt to induce latch-up (see Figures 4, 5 and 8)

2.20
trigger duration
duration of an applied pulse from the trigger source (see Figures 4, 5 and 8 and Table 2)

2.21
V_{supply} pin (or pin group)
all DUT power supply and external voltage source pins (excluding ground pins), including both positive- and negative-potential pins

NOTE 1 Generally, it is permissible to treat equal potential voltage source pins as one V_{supply} pin (or pin group) and connect them to one power supply.

NOTE 2 When forming V_{supply} pins (or pin groups), the combination of V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

2.22
V_{supply} overvoltage test
latch-up test that supplies overvoltage pulses or overvoltage d.c. level to the V_{supply} pin under test

2.23
V_{supply} voltage level
applicable voltage level of the V_{supply} pin specified in the relevant specification. The V_{supply} voltage level is used for latch-up testing as the typical logic high level unless otherwise specified (see 2.9)

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2.24
ground voltage level
ground potential used for latch-up testing as the typical logic low level, unless otherwise specified (see 2.10)

3 Classification and levels

3.1 Classification

There are two classes for latch-up testing.

- Class I is for testing at room temperature ambient.
- Class II is for testing at the maximum operating ambient temperature (T_a) or maximum operating case temperature (T_c) or maximum operating junction temperature (T_j) in the detailed specification.

For Class II testing at the maximum operating T_a or T_c, the ambient temperature or case temperature (T_c) shall be established at the required test value. For Class II testing at the maximum operating T_j, the ambient temperature T_a or the case temperature T_c should be selected to achieve a temperature characteristic of the junction temperature for a given device operating mode(s) during latch-up testing. The maximum operating ambient or case temperature during stress may be calculated based on the methods detailed in Annex B.

NOTE Elevated temperature will reduce latch-up resistance, and class II testing is recommended for devices that are required to operate at elevated temperature.

3.2 Levels

Level defines the I-test current injection value used during latch-up testing. Latch-up passing levels are defined as follows:

Level A – The trigger current value in Table 1 shall be +100 mA as defined in Figure 6 and -100 mA as defined in Figure 7. If all pins on the part pass at least the Level A trigger current values, then the part shall be considered a Level A part.

Level B – If any pins on the part do not pass the Level A standard, then the supplier shall determine the minimum passing trigger current requirement for each pin stressed differently than in Level A. The maximum (or highest) passing trigger current value shall be reported in the record for each pin stressed differently than in Level A, and the part shall be considered to be a Level B part, see 5.2.5.

4 Apparatus and material

The apparatus required for this test method includes the following.

4.1 Latch-up tester

4.1.1 General

Test equipment capable of performing the tests as specified in this standard. For devices requiring dynamic testing, the test equipment shall be capable of supplying timing signals and logic setup vectors required to control the I/O pin output states as specified in 5.2.3. The required timing signals and logic vectors may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate.

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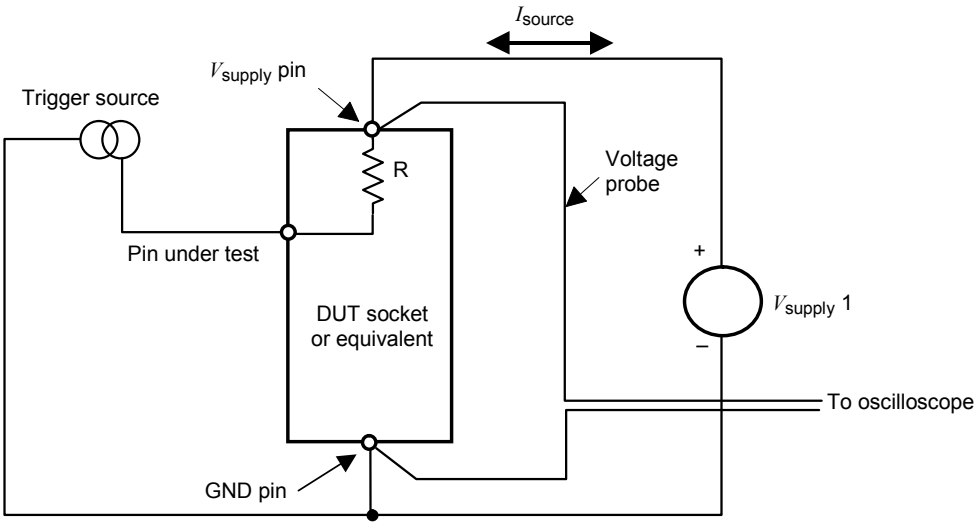
4.1.2 V_{supply} and their qualification method

For the I-test, sink type voltage power supplies shall be connected to all V_{supply} pins as shown in Figure 6 and Figure 7, and the transient characteristics shall be qualified as shown in Figure 1. The qualification steps are as follows:

a) Connect the supply voltage (e.g. 5 V, 3,3 V) to the V_{supply} pin. The value of voltage may be specified in the relevant specification.

b) Apply positive and negative pulses from the 200 mA trigger source, and measure their effect on the voltage waveform shown on the oscilloscope.

c) The voltage measured by the oscilloscope shall be within 90 % to 110 % of the supply voltage.



Value of R (e.g. 50 Ω) is specified in the applicable procurement document.
Input impedance of voltage probe and oscilloscope is over 10 kΩ.

IEC 671/11

Figure 1 – V_{supply} qualification circuit

4.1.3 Trigger source qualification method

The electrical characteristics of the trigger source including its transient characteristics shall be qualified as shown in Figure 2. The qualification steps are as follows:

a) With switch S1 closed, apply positive and negative pulses from the 200 mA trigger source, and measure its current waveform. The current waveform shall satisfy the requirements of Table 1.

b) After setting the voltage clamp level and opening S1, apply positive and negative pulses from the 100 mA trigger source and measure its voltage waveform. The voltage waveform during the working voltage clamp shall be within 90 % to 110 % of the voltage clamp setting level.

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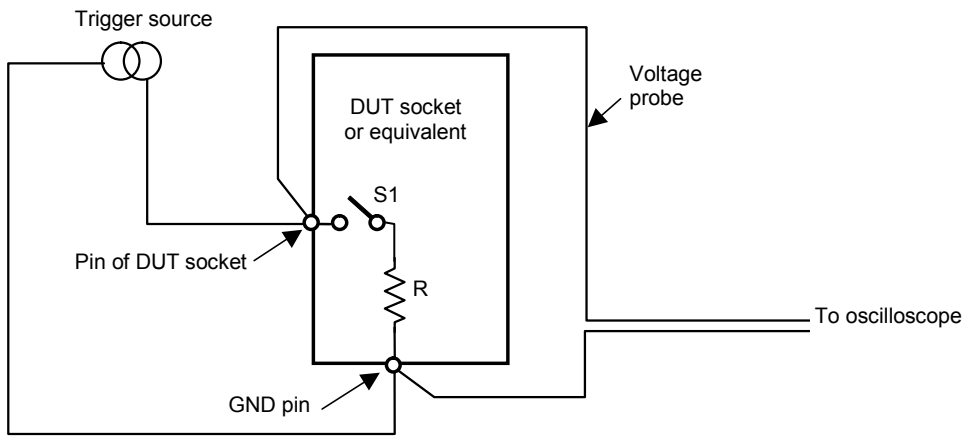

Value of R (e.g. 50 Ω) is specified in the applicable specification.
Input impedance of voltage probe and oscilloscope is over 10 kΩ.

IEC 672/11

Figure 2 – Trigger source qualification circuit

4.2 Automated test equipment (ATE)

A device tester capable of performing full functional and parametric testing of the device specified in the relevant specification.

4.3 Heat source

Equipment capable of heating and maintaining the DUT at the maximum operating temperature specified in the relevant specification during the latch-up test.

5 Procedure

5.1 General latch-up test procedure

Prior to the latch-up test, the device needs to be in a stable state with reproducible I_{nom}. Engineering judgment may be needed to achieve sufficient stability. The supply current should be made as low as practicable. The supply current must be stable enough and low enough to reliably detect the supply current increase if latch-up occurs.

A sample group of devices (e.g. six) shall be subjected to latch-up testing using the I-test and V_{supply} overvoltage test. The use of a new sample group for each latch-up test type (I-test, and/or V_{supply} overvoltage test) is also acceptable. All devices to be latch-up tested shall have passed the specified functional and parametric testing.

Before latch-up testing, the device continuity in the socket should be checked to avoid false latch-up failures. The latch-up test flow shall be as shown in Figure 3. The devices to be tested shall be subjected to the test conditions specified in Table 1 and Table 2. All “no connect” pins on the DUT shall be left open (floating) at all times.

All pins on the DUT, with the exception of “no connect” pins and timing related pins, shall be latch-up tested. The input, output and configurable I/O pins shall be tested with the I-test and the V_{supply} pins tested with the overvoltage test. This includes special pins defined in Annex A. The passing current or voltage values for the special pins can be used for determining the values of the passive-components connected to the pins. I/O pins shall be tested in all possible operating states or the worst case operating state (typically high impedance for configurable I/O pins and output pins).

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Dynamic devices shall be tested according to 5.2.3. When a device is sufficiently complex that testing of all configurable I/O pins in the worst case condition is not practicable, the device should be conditioned with a set of vectors representative of the typical operation of the device as determined by engineering judgement. When an I/O pin cannot be tested in the high impedance state, the I/O shall be tested in a valid logic state. Untested pins and pins that could not be completely tested shall be recorded as specified in 5.2.5 and the user shall be informed of all I/O pins that were not tested or tested in all states. After latch-up testing, all devices shall pass the criteria specified in Clause 6.

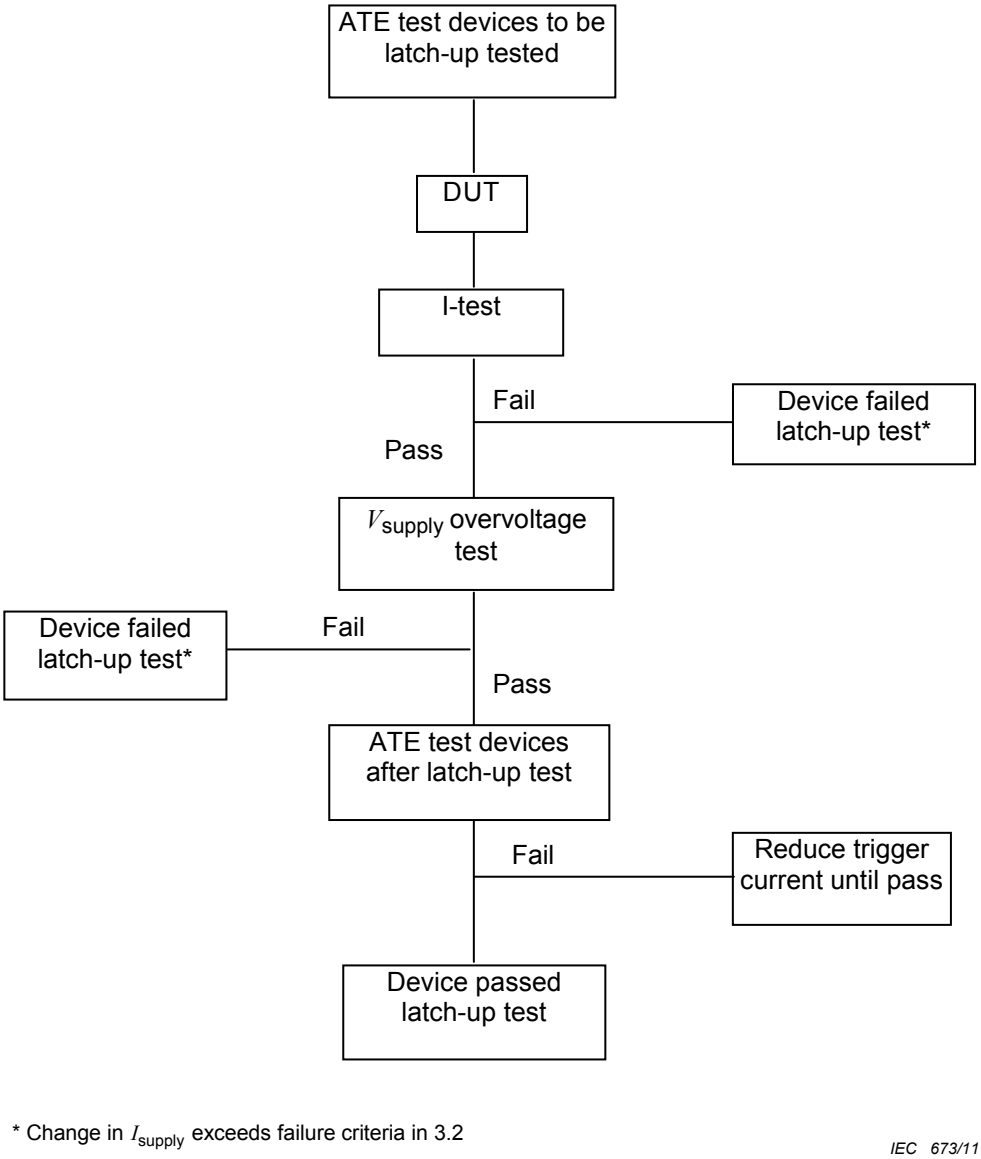

Figure 3 – Latch-up test flow

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Table 1 – Test matrix[a]

Test type	Trigger polarity	Condition of untested input pins[b]	Test temperature (±2°C)	V_{supply} condition	Trigger test conditions[g]	Failure criteria[fg]
I-Test	Positive see Figure 6	Max logic high	Temperature Class I Room temperature	Maximum operating voltage for each V_{supply} pin group according to device specification	According to classification levels in 3.2[d]	If absolute I_{nom} is = < 25 mA, then absolute I_{nom} + 10 mA is used or if absolute I_{nom} is > 25 mA, then > 1,4 X absolute I_{nom} is used
		Min logic low				
	Negative see Figure 7	Max logic high			According to classification levels in 3.2[e]	
		Min logic low				
V_{supply} Over-voltage test	See Figure 9	Logic high			Absolute maximum rating or 1,5 maximum V_{supply} whichever is lower[c]	
		Logic low				
I-Test	Positive see Figure 6	Max logic high	Temperature Class II Maximum ambient operating temperature	Maximum operating voltage for each V_{supply} pin group according to device specification	According to classification levels in 3.2[e]	
		Min logic low				
	Negative see Figure 7	Max logic high			According to classification levels in 3.2[e]	
		Min logic low				
V_{supply} Over-voltage test	See Figure 9	Max logic high			1,5 × max V_{supply}[c]	
		Min logic low				

a The trigger conditions herein are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from this table, the trigger conditions used must be defined in the test results.

b The V_{supply} voltage level and ground voltage level shall be applied as the logic high level and logic low level unless otherwise specified in the relevant specification. In the context of a non-digital device, logic levels shall be interpreted as the most appropriate of V_{supply} voltage, ground voltage or the specified minimum or maximum that may be applied to the pin.

c Current clamped at (I_{nom} + 100 mA) or 1,5 × I_{nom}, whichever is greater (Refer to 2.11 for max V_{supply} definition). The I_{nom} value used for the current clamp calculation relates to the V_{supply} pin (or pin groups) being tested.

d Voltage clamped at V_{max} + 0,5(V_{max} – V_{min}) if V_{min} is > 0. Otherwise, the voltage clamp is 1,5 V_{max}.

e Voltage clamped at V_{max} - 0,5(V_{max} – V_{min}) if V_{min} is > 0. Otherwise, the voltage clamp is -0,5 V_{max}.

f If the trigger test condition reaches the voltage or current clamp limit and latch-up has not occurred, the pin passes the latch-up test. See Clause 6 for complete failure definition.

g The I_{nom} value used for the trigger current calculation relates to the V_{supply} pin (or pin groups) being tested, not just the I_{nom} supply for the pin under test.

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Table 2 – Timing specifications for I-test and V_{supply} overvoltage test

Symbol	Time interval	Parameter	Limits	
			Minimum	Maximum
t_r		Trigger rise time	5 µs	5 ms
t_f		Trigger fall time	5 µs	5 ms
t_{width}	T3 → T4	Trigger duration (width)	2 × t_r	10 ms (I-test) 5 s (V_{supply} overvoltage test)
TOS		Trigger over-shoot	±5 % of pulse voltage	
t_{cool}	T4 → T7	Cool down time	≥t_{width}	
$t_{measure}$[a]	T4 → T5	Waiting time before measuring I_{supply}	3 ms	5s

[a] The wait time should be sufficient to allow for power supply ramp down and stabilization of I_{supply}.

5.2 Detailed latch-up test procedure

5.2.1 I-test

The I-test shall be performed as follows:

a) The devices shall be subjected to the I-test as indicated in Figures 3, 4 and 5 and Tables 1 and 2.

b) Bias the DUT as indicated in Figure 6. All input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins, shall be tied to the V_{supply} voltage level specified. Input pins used for preconditioning shall be tested in their defined state (pins that are tied to a logic-high level to precondition the DUT can only be tested in the logic-high state; pins that are tied to a logic-low level to precondition the DUT can only be tested in the logic-low state). Allow the DUT to stabilize at the test temperature.

c) Put the pin under test in logic-high state. Measure nominal I_{supply} (I_{nom}) for each V_{supply} pin (or pin group, see 2.21). Then, apply the positive current trigger (as specified in Table 1 for a duration as specified in Table 2) to the pin under test.

d) After the trigger source has been removed, return the pin under test to the state it was in before the application of the trigger pulse, and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in definition 3.2, latch-up has occurred and power shall be removed from the DUT. If latch-up has occurred, stop the test; the DUT has failed latch-up testing. Using a new device, return to step a) and continue testing.

e) If latch-up has not occurred, after the necessary cool-down time (see Table 2), repeat steps c) and d) for all pins to be tested (noting the exceptions stated in step b)).

f) Repeat steps b) through e) with all input pins, including bi-directional) I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to ground voltage level.

g) Bias the DUT as indicated in Figure 7. All input pins, (including bi-directional I/O pins in an input state or high impedance state), that are not used for preconditioning the I/O pins shall be tied to V_{supply} voltage level specified in the relevant specification (noting the exceptions stated in step b)).

h) Put the pin under test in logic-low state. Measure nominal I_{supply} (I_{nom}) for each V_{supply} pin (or pin group, see 2.21). Then, apply the negative current trigger source below ground (in accordance with Table 1 for a duration as specified in Table 2) to the pin under test.

i) After the trigger source has been removed, return the pin under test to the state it was in before the application of the trigger pulse and measure the I_{supply} for each V_{supply} pin (or

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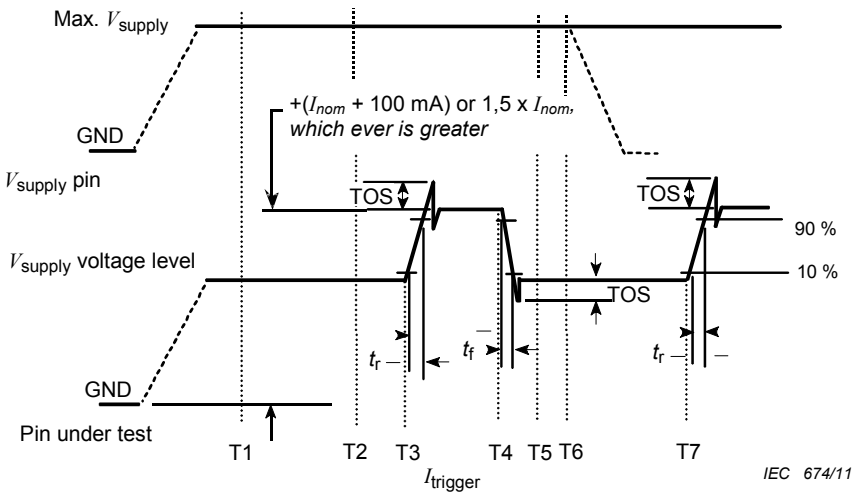
pin group). If any I_{supply} is greater than or equal to the failure criteria specified in definition 3.2, latch-up has occurred and power shall be removed from the DUT. If latch-up has occurred, stop the test; the DUT has failed latch-up testing. Using a new device, return to step a) and continue testing.

j) If latch-up has not occurred, after the necessary cool-down time (see Table 2), repeat steps h) and i) for all pins to be tested.

k) Repeat steps h) through j) with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the ground voltage level (noting the exceptions stated in step b)).

l) The I-test in this sub-clause does not require the removal of power-supply voltage between stresses, i.e., cool-down time. Users should evaluate the risk of leaving the power-supply on.



Time	Operation
T1 → T2	Measure nominal I_{supply} (I_{nom})
T4 → T7	Cool down time (t_{cool})
T4 → T5	Wait time prior to I_{supply} measurement
T5	Measure I_{supply}
T6	If any I_{supply} ≥ the failure criteria defined in 3.2, latch-up has occurred and power must be removed from DUT.

NOTE 1 The wait time is sufficient to allow for power supply ramp down and stabilization of I_{supply}.

NOTE 2 The pin under test should be set to logic high before positive current trigger. It is permissible to start positive current trigger from logic low, but failing results should be confirmed from the logic high state.

Figure 4 – Test waveform for positive I-test

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