IEC 61189-5-502

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INTERNATIONAL STANDARD

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colour inside

Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 5-502: General test methods for materials and assemblies – Surface Insulation Resistance (SIR) testing of assemblies

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles – Partie 5-502: Méthodes d'essai générales pour les matériaux et les ensembles – Essais de résistance d'isolement en surface (RIS) des ensembles

IEC 61189-5-502:2021-02(en-fr)

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARD AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 5-502: General test methods for materials and assemblies – Surface Insulation Resistance (SIR) testing of assemblies

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The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1646/CDV	91/1673/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

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A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed board and other interconnection structures and assemblies*, can be found on the IEC website.

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARD AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 5-502: General test methods for materials and assemblies – Surface Insulation Resistance (SIR) testing of assemblies

1 Scope

This part of IEC 61189 is used for evaluating the changes to the surface insulation resistance of a pre-selected material set on a representative test coupon and quantifies the deleterious effects of improperly used materials and processes that can lead to decreases in electrical resistance.

An assembly process involves a number of different process materials including solder flux, solder paste, solder wire, underfill materials, adhesives, staking compounds, temporary masking materials, cleaning solvents, conformal coatings and more. The test employs two different test conditions of 85 °C and 85 % relative humidity (RH), preferred for a process that includes cleaning, or 40 °C and 90 % relative humidity (RH), preferred for processes where no cleaning is involved.

NOTE 40 °C and 93 % RH can be used as an alternative to 40 °C and 90 % RH. Additional information is provided in 5.4 and A.5.2.

Testing is material (set) and process / equipment specific. Qualifications are to be performed using the production intent equipment, processes and materials.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-1, *Environmental testing – Part 1: General and guidance*

IEC 60068-2-20, *Environmental testing – Part 2-20: Tests – Test T: Test methods for solderability and resistance to soldering heat of devices with leads*

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60068-2-67, *Environmental testing – Part 2-67: Tests – Test Cy: Damp heat, steady state, accelerated test primarily intended for components*

IEC 60068-2-78, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61190-1-3, *Attachment materials for electronic assembly – Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solder for electronic soldering applications*

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3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60068-1, IEC 60068-2-20:2008, IEC 60068-2-58, IEC 60194, and IEC 61190-1-3 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
test coupon
test specimen, test vehicle, test sample

4 Equipment/Apparatus

4.1 Soldering and other production process equipment

All the equipment shall represent the equipment to be used in production.

4.2 Measurement instrument

This shall consist of a measuring device capable of measuring insulation resistance in the range of at least 10^6 Ω to 10^{12} Ω.

It shall be capable of measuring and recording each individual test pattern of an IPC-B-52 test board/assembly. The measurement circuit shall incorporate a 1 MΩ current limiting resistor in each current pathway.

The tolerance of the total measurement system shall be:

- ±5 % up to 10^{10} Ω at 5 V;
- ±10 % between 10^{10} Ω to 10^{11} Ω at 5 V;
- ±20 % above 10^{11} Ω at 5 V.

If a different test voltage is to be used, the measurement circuit shall be assessed at that voltage rather than the 5 V stipulated. See 6.8 and Clause A.12 for additional information on test voltages.

The resistors used to confirm the "total measurement system tolerance" defined above, shall have a purchased tolerance of:

- ±0,1 % up to and including 10^6 Ω;
- ±1 % above 10^6 Ω and up to and including 10^8 Ω;
- ±5 % above 10^8 Ω and up to and including 10^{10} Ω;
- ±10 % above 10^{10} Ω.

The instrument can be used with either an external or internal power supply but shall be capable of delivering a variable voltage from (5 to 100) V DC ±1 % with a 1 MΩ load and a channel to channel isolation resistance of 10^{13} Ω.

The system shall be capable of taking measurements in the time interval required.

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Equipment shall have the measurement capability to repeat the resistance measurement on all channels at least every 20 min.

4.3 Resistor verification coupon

The measurement system measurement performance shall be verified by substituting a resistor verification coupon (see Figure 1) in place of the test coupons while in the chamber at both ambient and elevated conditions.

This coupon should be fitted with at least 4 “known value” resistors. The tolerances for the “known value” resistors shall be as per the purchased tolerances detailed in 4.2.

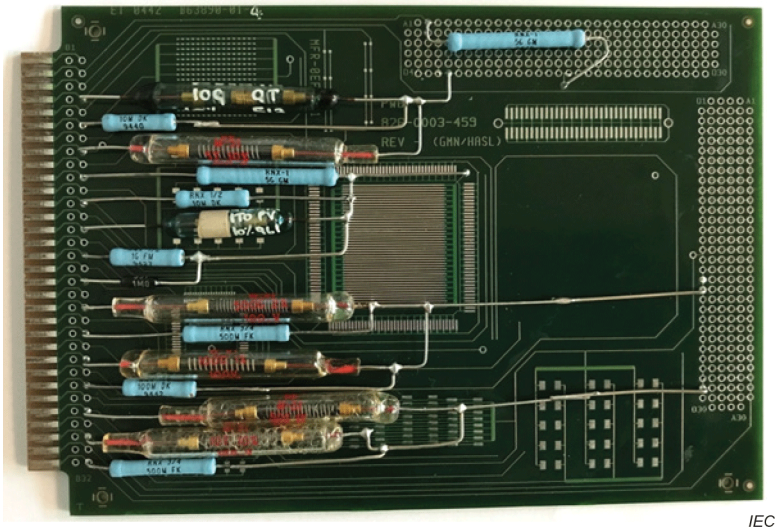

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Figure 1 – Resistor verification coupon using the IPC-B-52 coupon

The resistor verification coupon should have a protective metal (stainless steel) cover attached with stainless hardware to the grounded mounting holes on the coupon to protect the resistors from contamination or damage during handling operations.

Other types of test coupon may be used in place of the IPC-B-52 RVC, as this coupon is used only to verify continuity prior to the commencement of the test.

4.4 Damp heat chamber

A damp heat chamber capable of being adjusted to a temperature of 20 ˚C ± 2 ˚C to 100 ˚C ± 2 °C and of relative humidity between 80 % RH ±3 % RH and 90 % RH ± 3 % RH according to IEC 60068-2-67 and IEC 60068-2-78 shall be used.

If the alternative conditions of 40 °C and 93 % RH are to be used, the damp heat chamber shall be capable of the upper humidity level of 93 % RH ± 3 % RH rather than the 90 % RH ± 3 % RH specified above; see 5.4 and A.5.1 for further information.

The chamber shall be constructed with stainless steel inner surfaces and be well-insulated. The temperature and humidity measurement should be taken using sensors such as dry and wet bulb thermometers or solid-state sensors. The temperature and humidity levels of the test chamber shall be recorded at a minimum of 5 minute intervals throughout the test, preferably with independent control sensors.

The location of the samples within the chamber should ensure that the airflow within is not impeded.

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Adequate mixing of water vapour and air is imperative to ensure condensation does not occur anywhere in the chamber except on/around cooling or dehumidification coils. If any part of interior of the chamber is below the dew point, possibly due to insulation or control issues, condensation will occur. The samples should be kept above the dew point and be shielded from dripping or flying condensate.

Prior to every test, the chamber interior shall be wiped down with a mixture of 50 % propan-2-ol and 50 % deionized water. The chamber shall be free from any unwanted residues from previous tests. The chamber should have been dedicated to heat and humidity testing only and not used for tests such as salt fog, salt mist or salt spray.

4.5 Magnifiers (10x – 30x)

To assist in post-test inspection, it is recommended that the user has a magnifier of not less than 10x to a maximum 30x magnification.

4.6 Camera

It is recommended the user has a suitable camera available to photograph test coupons that exhibit electrochemical migration or intermetallic dendritic growth.

4.7 Cleaning solvent

Removal of flux residues by a cleaning solvent should replicate the processes intended for production hardware.

4.8 Interconnecting cable

A PTFE insulated wire or ribbon cable should be used to connect the test coupon to the measurement system. This cable should be shielded using a suitable metallised cable mesh to minimise the risk of tribo-electrical interference and electrical noise.

4.9 Connector rack

The connector rack should employ a connector (edge card or hard solder connection) suitable to withstand the test environment. For edge card connection, use of gold-plated mating parts is recommended.

4.10 Solder flux

Preferably use a fluxless solder wire. Alternatively, a flux-cored solder wire that conforms to IEC 61190-1-3.

5 Test coupon

5.1 Test coupon artwork

5.1.1 General

The test coupon shall be the IPC-B-52 as shown in Figure 2 and Figure 3. The necessary manufacturing data and artwork for this test coupon can be acquired from the IPC online store under the reference: IPC-A-52-English-D.

The test board shall be prepared by the preferred board supplier, using the same processes as those intended for the user's end-product.

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5.1.2 Test coupon

The IPC B-52 printed circuit assembly consists of several components having test patterns adjacent to, and beneath, the components. Prior to being subjected to conditioning the components are soldered onto the board, using methodologies replicating as closely as possible the proposed production techniques. See A.1.3 for additional information.

5.1.3 Laminate

The test coupon laminate should represent the substrate to be used in production.

5.1.4 Surface finish

The test coupon shall be finished with the same surface finish intended for the end-product.

When multiple surface finishes are used on end-products, the manufacturer shall have objective evidence that the worst-case (from a residue standpoint) surface finish was tested.

5.1.5 Solder mask

The test coupon shall be finished with the same solder mask intended for the end-product.

5.1.6 Quality

The test coupons should be manufactured by the preferred supplier(s) to avoid compromising the validity of the test. Bought-in coupons from an independent source should not be used as these may feature:

- inappropriate laminate;
- indeterminant age and condition;
- indeterminate solder mask;
- inappropriate surface finish.

5.2 Components (bill of materials)

Comb patterns: the test coupon IPC B-52, as shown in Figure 2 and Figure 3, comprises the following bill of materials (BOM) as shown in Table 1.

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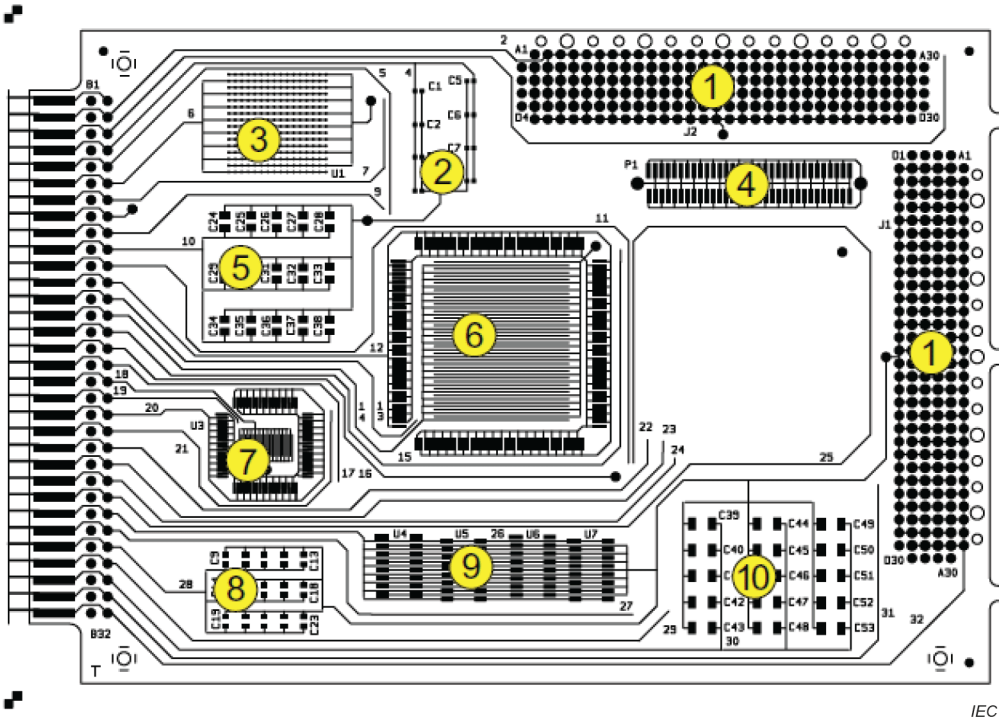
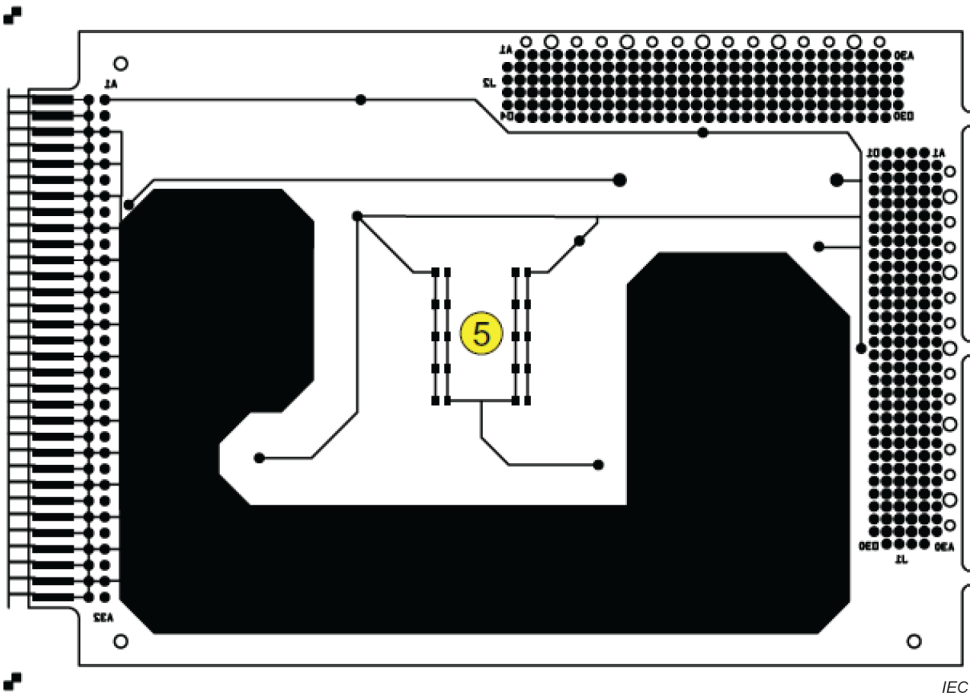


A list of all the components shown in Figure 2 is provided in Table 1.

Figure 2 – IPC B-52 Rev B top side



A list of all the components shown in Figure 3 is provided in Table 1.

Figure 3 – IPC B-52 Rev B bottom side

Apart from the chip resistors or capacitors, all the components used in this test shall be true "dummy" components designed specifically for SIR testing. Scrap devices or devices with any form of internal die shall not be used as these will compromise test results.

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Table 1 – IPC B-52 bill of materials (BOM)

ID	Component/Pattern	Qty	Component Details
1	TH connector 4 × 24 pins	2	AMP part 536501-3 or equivalent.
2	Capacitor, 1 pF to 10 pF, 0402 package	8	Surface mount ceramic capacitor, 0402 body, 1 pF to 10 pF, DC 50 V , 5 % tolerance. AVX part 04025A100JAT2A or equivalent.
3	BGA, 256 IO, 1 mm pitch, isolated	1	Dummy component, no internal die or wires BGA, 256 I/O, full 16 x 16 array, 1,0 mm pitch, 17 mm body size.
4	SM connector IEEE 1386, 2 x 16 pins	1	Molex Waldom part 71436-2164 or equivalent.
5	Capacitor, 1 pF to 10 pF, 0805 package	25	Surface mount ceramic capacitor, 0805 body, 1 pF to 10pF, DC 100 V , 5 % tolerance. AVX part 08051A100JAT9A or equivalent.
6	QFP160 0,65 mm pitch, isolated	1	Dummy component, no internal die or wires, quad flat pack, 160 I/O, 28 mm square body, 0,65 mm pitch.
7	QFP80 0,5 mm pitch, isolated	1	Dummy component, no internal die or wires, quad flat pack, 80 I/O, 12mm square body, 0,5 mm pitch, 2 mm lead footprint.
8	Capacitor, 1 pF to 10 pF, 0603 package	15	Surface mount ceramic capacitor, 0603 body, 1 pF to 10 pF, DC 50 V , 5 % tolerance. AVX part 0603A100JAT2A or equivalent.
9	SOIC16, 1,27 mm pitch, isolated	4	Dummy component, no internal die or wires, small outline integrated circuit, 16 I/O, 1,27 mm pitch leads, 3,8 mm body.
10	Capacitor, 1 pF to 10 pF, 1206 package	15	Surface mount ceramic capacitor, 1206 body, 1 pF to 10 pF, DC 100 V, 5 % tolerance. AVX part 12062A100JAT92 or equivalent.

The design of this test coupon and the components listed in Table 1, are representative of those presenting challenges for material and process compatibility as occurs in the assembly production process. However, QFNs might represent the greatest challenge for material residue accumulation – B-52 has a representative cross-section of component shapes used in the industry, but users should employ their own components if they have a different form factor, like QFN.

5.3 Number of test coupons

A minimum of 3 B-52 test coupons shall be tested for each material/process combination. When conducting a process qualification, a sample size of 10 shall be used.

With every test, additional unprocessed coupons should be included in the test as controls.

5.4 Test conditions

All specimens shall be tested at 40 °C ± 2 °C and 90 % RH ± 3 % RH (according to IEC 60068-2-78) or 85 °C ± 2 °C and 85 % RH ± 3 % RH (according to IEC 60068-2-67).

No-clean processes are recommended to be tested using 40 °C in a 90 % RH environment.

As an alternative to 40 °C ± 2 °C and 90 % RH ± 3 % RH, it is acceptable to use 40 °C ± 2°C and 93 % RH ± 3 %. If 93 % RH is desired to be used instead of 90 % RH (at 40 °C), this shall be agreed between user and supplier prior to use. Using 93 % RH could lead to different results when compared to using 90 % RH. See A.5.1 for additional information.

Refer to Clause A.1 for general information.

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5.5 Coupon identification

Test coupons should be identified using the production process. Use of marking pens should be avoided.

6 Procedure

6.1 Test coupon preparation

The test coupon shall represent the substrate materials, assembly material set and fabrication processes used in production. The test coupon circuitry shall provide for SIR testing as shown in Figure 2 and Figure 3. Components of the type to be soldered in production are representative of the hardest to clean configurations (in terms of "shadowing" of the solder joints by component bodies and component-to-substrate spacing) as shown in Table 1 BOM. As the test pattern is used to monitor the effect of printed board assembly processing, they shall be exposed to all printed board assembly processes (i.e., the test pattern shall not be covered by permanent solder mask).

6.2 Cleaning

Fluxes that require cleaning should be cleaned as per the intended production process.

Details of the cleaning procedure used on the coupons should be included in the test report.

6.3 Manufacturing process replication

The coupon manufacturing process used in this method is assumed to replicate the process intended for production hardware. In cases where the assembly process involves multiple solder operations (for example, surface mount reflow, wave solder, rework, hand solder, or conformal coating if used), all these processes shall be carried out on the assembled test coupon. This would be necessary even in cases where only one of the soldering processes is being changed since residues from one process can interact with residues from a prior or following process. It is the total of all these processes which would be shipped, and thus it is their total that shall be tested and qualified. Refer to IPC 9203 and IPC 9201 for additional information.

For those coupons involving a “no-clean” process, no cleaning prior to assembly shall be carried out.

6.4 Preparation of samples for chamber

Test patterns should be tested for electrical shorts prior to testing. Excessive solder should be removed from the test samples using approved manufacturing rework processes.

Assembled coupons should be connected by either a connector system or by hard wiring. See Clause A.8 for additional information.

It is recommended that the physical pre-test appearance be photographically documented, and any physical anomalies recorded.

6.5 Connector system – High-resistance measurement verification

Prior to connecting test coupons to the measurement system, each cable assembly shall be connected to the resistor verification coupon inside the humidity chamber at ambient conditions and a measurement taken, see 4.3. Any cable that does not read within the tolerance value of the total measurement system defined in 4.2 shall be reworked, replaced, or not used.

Documents
Document Sharing Hub
Full document details: IEC 61189-5-502-2021