

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Components for low-voltage surge protection –
Part 341: Performance requirements and test circuits for thyristor surge
suppressors (TSS)**

**Composants pour parafoudres basse tension –
Partie 341: Exigences de performance et circuits d'essai pour parafoudres
à thyristor (TSS)**



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMPONENTS FOR LOW-VOLTAGE SURGE PROTECTION –**Part 341: Performance requirements and test circuits
for thyristor surge suppressors (TSS)**

FOREWORD

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International Standard IEC 61643-341 has been prepared by subcommittee 37B, Components for low-voltage surge protection, of IEC technical committee 37: Surge arresters.

This second edition of IEC 61643-341 cancels and replaces the first edition published in 2001. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition: Addition of performance values.

The text of this standard is based on the following documents:

FDIS	Report on voting
37B/218/FDIS	37B/220/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of IEC 61643 series, under the general title *Components for low-voltage surge protective devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

COMPONENTS FOR LOW-VOLTAGE SURGE PROTECTION –

Part 341: Performance requirements and test circuits for thyristor surge suppressors (TSS)

1 Scope

This part of IEC 61643 specifies standard test circuits and methods for thyristor surge suppressor (TSS) components. These surge protective components, SPCs, are specially formulated thyristors designed to limit overvoltages and divert surge currents by clamping and switching actions. These SPCs are used in the construction of surge protective devices (SPDs) and equipment used in Information & Communications Technologies (ICT) networks with voltages up to AC 1 000 V and DC 1 500 V. This document is applicable to gated or non-gated TSS components with third quadrant (-v and -i) characteristics of blocking, conducting or switching.

This document contains information on

- terminology;
- letter symbols;
- essential ratings and characteristics;
- rating verification and characteristic measurement;

This document does not apply to the conventional three-terminal thyristors as covered by IEC 60747-6.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-521, *International Electrotechnical Vocabulary – Chapter 521: Semiconductor devices and integrated circuits*

IEC 60068-2-20:2008, *Environmental testing – Part 2-20: Tests – Test T: Test methods for solderability and resistance to soldering heat of devices with leads*

3 Terms, definitions, abbreviated terms and symbols

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1 Parametric terms, letter symbols and definitions

Where appropriate, terms, letter symbols and definitions are used from conventional thyristor (IEC 60747-6) and rectifier diode (IEC 60747-2) standards. TSS definitions are the same or similar to conventional thyristor definitions. To avoid the proliferation of terms, the word “thyristor”, as used in the terms of this document, is synonymous with “TSS”.

NOTE 1 IEC 60747-1, clause 2.1.1 Basic letters, states “IEC 60027 recommends the letters V and v only as reserve symbols for voltage; however, in the field of semiconductor devices, they are so widely used that in this publication they are on the same plane as U and u .” This document uses the letters V and v for voltage with the letters U and u as alternatives.

NOTE 2 Where several distinctive forms of letter symbol exist, the most commonly used form is given first.

3.2 General terms

3.2.1 information and communications technologies

ICT

group of applications using information and communications (telecommunications) technologies

[SOURCE: ISO/IEC 24704:2004, 3.1.5]

3.2.2 overcurrent

any current having a peak value exceeding the corresponding peak value of maximum steady-state current at normal operating conditions

[SOURCE: IEC 60664-2-1, ed. 2.0 (2011-01), 3.21, modified by replacing voltage with current]

3.2.3 overvoltage

any voltage having a peak value exceeding the corresponding peak value of maximum steady-state voltage at normal operating conditions

[SOURCE: IEC 60664-2-1, ed. 2.0 (2011-01), 3.21]

3.2.4 surge protective device

SPD

device that restricts the voltage of a designated port or ports, caused by a surge, when it exceeds a predetermined level

Note 1 to entry: Secondary functions may be incorporated, such as a current limiting to restrict a terminal current.

Note 2 to entry: Typically, the protective circuit has at least one non-linear voltage-limiting surge protective component.

Note 3 to entry: An SPD is a complete assembly, having terminals to connect to the circuit conductors.

[SOURCE: IEC 61643-21:2008, 3.8]

3.3 Main terminal ratings

Listed ratings cover the appropriate requirements of the blocking, conducting and switching quadrants.

3.3.1**repetitive peak off-state voltage** V_{DRM}

highest instantaneous value of the off-state voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages

[SOURCE: IEC 60747-6:2000, 3.5.12[10]¹, modified (removal of NOTE)]

3.3.2**repetitive peak on-state current** I_{TRM}

peak value of the on-state current, including all repetitive transient currents

[SOURCE: IEC 60747-6:2000, 3.6.15[10], modified (removal of Figure)]

3.3.3**surge on-state current** I_{TSM}

on-state current pulse of short duration and specified waveshape, whose application causes or would cause the maximum rated virtual junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions

[SOURCE: IEC 60747-6:2000, 3.6.17[10], modified (removal of "(for example, a fault) (see figure 4)")]

3.3.4**non-repetitive peak impulse current** I_{PP}

rated maximum value of peak impulse current of specified amplitude and waveshape that may be applied

3.3.5**repetitive peak reverse voltage (of a unidirectional thyristor)** V_{RRM}

highest instantaneous value of the reverse voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages

[SOURCE: IEC 60747-6:2000, 3.5.6[10], modified (removal of NOTE)]

3.3.6**non-repetitive surge forward current** I_{FSM}

forward current pulse of short time duration and specified waveshape, whose application causes or would cause the maximum rated junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions (for example a fault)

[SOURCE: IEC 60747-2:2000, 3.3.6[9], modified (original term did not include "non-repetitive")]

3.3.7**repetitive peak forward current (diode)** I_{FRM}

peak value of the forward current including all repetitive transient currents

¹ Numbers in square brackets refer to the bibliography.

[SOURCE: IEC 60747-2:2000, 3.3.4[9]]

3.3.8

critical rate of rise of on-state current

di_T/dt_{cr}

highest value of the rate of rise of on-state current that a thyristor can withstand without deleterious effect

[SOURCE: IEC 60747-6:2000, 3.6.23[10]]

3.4 Main terminal characteristics

3.4.1

off-state voltage

V_D

anode, principal, or thyristor voltage when the thyristor is in the off state

[SOURCE: IEC 60747-6:2000, 3.5.9[10]]

3.4.2

off-state current

I_D

anode, principal, or thyristor current when the thyristor is in the off state

[SOURCE: IEC 60747-6:2000, 3.6.26[10]]

3.4.3

peak off-state current

I_{DRM}

maximum (peak) value of off-state current that results from the application of the repetitive peak off-state voltage, V_{DRM}

3.4.4

breakover voltage

$V_{(BO)}$

voltage at the breakover point

[SOURCE: IEC 60747-6:2000, 3.5.1[10]]

3.4.5

holding current

I_H

minimum anode, principal, or thyristor current that will maintain the thyristor in the on state

[SOURCE: IEC 60747-6:2000, 3.6.25[10]]

3.4.6

off-state capacitance

C_o, C_J

differential capacitance at the specified terminals in the off-state measured at specified frequency, f , amplitude, V_d and DC bias, V_D

3.4.7

repetitive peak reverse current

I_{RRM}

maximum (peak) value of reverse current that results from the application of the repetitive peak reverse voltage, V_{RRM}

3.4.8**forward recovery voltage (diode)** V_{FRM}

varying voltage occurring during the forward recovery time after instantaneous switching from zero or a specified reverse voltage to a specified forward current

[SOURCE: IEC 60747-2:2000, 3.2.3[9]]

3.5 Additional and derived parameters

The following derived and measured parameters may be necessary or useful for comparison, certain applications or statistical process controls.

3.5.1**breakover current** $I_{(BO)}$

anode, principal, or thyristor current at the breakover point

[SOURCE: IEC 60747-6:2000, 3.6.1[10]]

3.5.2**on-state voltage** V_T

anode, principal, or thyristor voltage when the thyristor is in the on state

[SOURCE: IEC 60747-6:2000, 3.5.8[10]]

3.5.3**on-state current** I_T

anode, principal, or thyristor current when the thyristor is in the on state

[SOURCE: IEC 60747-6:2000, 3.6.9[10]]

3.5.4**forward voltage (diode)** V_F

voltage across the terminals which results from the flow of current in the forward direction

[SOURCE: IEC 60747-2:2000, 3.2.1[9]]

3.5.5**forward current (diode)** I_F

current through the device in the forward conducting state

3.6 Temperature related parameters

All the semiconductor related TSS parameters are temperature dependent. The need for temperature dependence information can often be removed by specifying that a parameter's maximum or minimum value should be valid over the intended operating temperature range. Some common temperature related terms are shown hereafter.

3.6.1**variation of holding current with temperature**

change in holding current, I_H , with changes in temperature and shown as a graph

3.6.2**temperature derating**

derating with temperature above a specified base temperature, expressed as a percentage, such as may be applied to peak pulse current

3.6.3**thermal resistance**

R_{thJL} , R_{thJC} , R_{thJA} ($R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JA}$)

effective temperature rise per unit power dissipation of a designated junction, above the temperature of a stated external reference point (lead, case or ambient) under conditions of thermal equilibrium

Note 1 to entry: Thermal resistance is usually expressed as K/W with °C/W as an alternative.

3.6.4**transient thermal impedance**

$Z_{thJL}(t)$, $Z_{thJC}(t)$, $Z_{thJA}(t)$ ($Z_{\theta JL}(t)$, $Z_{\theta JC}(t)$, $Z_{\theta JA}(t)$)

change in the difference between the virtual junction temperature and the temperature of a specified reference point or region (lead, case, or ambient) at the end of a time interval, divided by the step function change in power dissipation at the beginning of the same time interval which causes the change of temperature difference

Note 1 to entry: Thermal impedance is usually expressed as K/W with °C/W as an alternative.

Note 2 to entry: It is the thermal impedance of the junction under conditions of change and is generally given in the form of a curve as a function of the duration of an applied power pulse.

3.6.5**(virtual) junction temperature**

T_J , T_{VJ}

theoretical temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behaviour of the device

Note 1 to entry: The term “virtual-junction temperature” is particularly applicable to multijunction semiconductors and is used to denote the temperature of the active semiconductor element when required in specifications and test methods. The term “junction temperature”, T_J , is used interchangeably with the term “virtual junction temperature”, T_{VJ} , in this standard.

3.6.6**maximum junction temperature**

T_{JM}

maximum value of permissible junction temperature, due to self-heating, which a TSS can withstand without degradation

3.6.7**storage temperature range**

T_{stgmin} to T_{stgmax}

temperature range over which the device can be stored without any voltage applied

3.7 Gate terminal parameters**3.7.1****gate trigger current**

I_{GT}

lowest gate current required to switch a device from the off-state to the on-state

3.7.2**gate trigger voltage**

V_{GT}

gate voltage required to produce the gate trigger current, I_{GT}

3.7.3

gate-to-adjacent terminal peak off-state voltage

V_{GDM}

maximum gate to cathode voltage for a P-gate component or gate to anode voltage for an N-gate component that may be applied such that a specified off-state current, I_{D} , at a rated off-state voltage, V_{D} , is not exceeded

3.7.4

peak off-state gate current

I_{GDM}

maximum gate current that results from the application of the peak off-state gate voltage, V_{GDM}

3.7.5

gate reverse current, adjacent terminal open

$I_{\text{GAO}}, I_{\text{GKO}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and the cathode terminal for a P-gate component or anode terminal for an N-gate component is open-circuited

3.7.6

gate reverse current, main terminals short-circuited

$I_{\text{GAS}}, I_{\text{GKS}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and the cathode terminal for a P-gate component or anode terminal for an N-gate component is short-circuited to the third terminal

Note 1 to entry: This definition only applies to components with integrated series gate blocking diodes.

3.7.7

gate reverse current, on-state

$I_{\text{GAT}}, I_{\text{GKT}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and a specified on-state current, I_{T} , is flowing

Note 1 to entry: This definition only applies to components with integrated series gate blocking diodes.

3.7.8

gate reverse current, forward conducting state

$I_{\text{GAF}}, I_{\text{GKF}}$

current through the gate terminal when a specified gate bias voltage, V_{G} , is applied and a specified forward conduction current, I_{F} , is flowing

Note 1 to entry: This definition only applies to conducting unidirectional components with integrated series gate blocking diodes.

3.7.9

gate switching charge

Q_{GS}

charge through the gate terminal, under impulse conditions, during the transition from the off-state to the switching point, when a specified gate bias voltage, V_{G} , is applied

3.7.10

peak gate switching current

I_{GSM}

maximum value of current through the gate terminal during the transition from the off state to the switching point, when a specified gate bias voltage, V_{G} , is applied

3.7.11**gate-to-adjacent terminal breakover voltage** $V_{GK(BO)}$, $V_{GA(BO)}$

gate-to-cathode voltage for a P-type component or gate to anode voltage for an N-gate component at the breakover point

Note 1 to entry: This is equivalent to the voltage difference between the breakover voltage, $V_{(BO)}$, and the specified gate voltage, V_G .

3.8 Abbreviated terms

AC Alternating Current

DC Direct Current

ICT Information & Communication Technology

TSS Thyristor Surge Suppressor

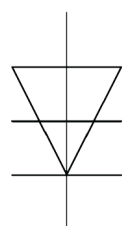
SPC Surge Protective Component

SPD Surge Protective Device

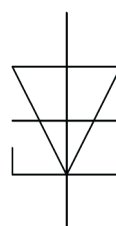
TRIAC TRIode for Alternating Current (bidirectional triode thyristor)

3.9 Circuit symbols

Thyristors can be made as two terminal components (fixed voltage) or with additional terminals connected to intermediate P or N layers (gated). In addition, they can be made with one switching quadrant or two switching quadrants. Figure 1 shows the circuit symbols for fixed voltage, one switching quadrant, two terminal TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams. The switching quadrant characteristic occurs when the top terminal is positive with respect to the bottom terminal (Figure 1 through Figure 3).



a) S00650



b) S00651

Figure 1 – Fixed voltage, two terminals: a) reverse blocking and b) reverse conducting

Figure 2 shows the circuit symbols for gated reverse blocking (one switching quadrant) TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams.

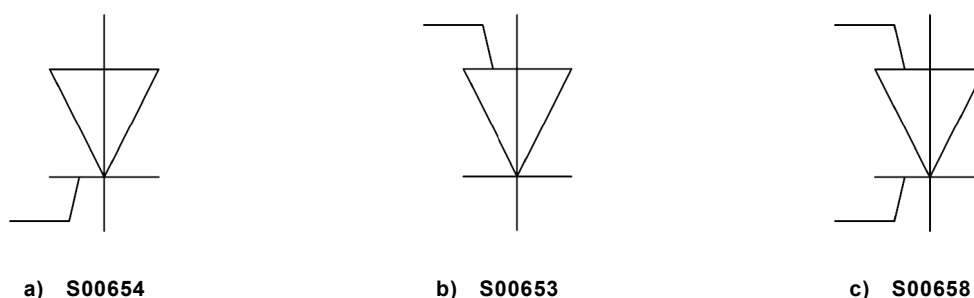


Figure 2 – Gated reverse blocking: a) P gate b) N gate and c) P & N gate

Figure 3 shows the circuit symbols for gated reverse conducting (one switching quadrant) TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams.



Figure 3 – Gated reverse conducting: a) P gate and b) N gate

Figure 4 shows the circuit symbols for bidirectional (two switching quadrant) TSSs based on the IEC 60617[5] S006XX series of graphical symbols for diagrams. The switching quadrant characteristic is for any top terminal polarity.



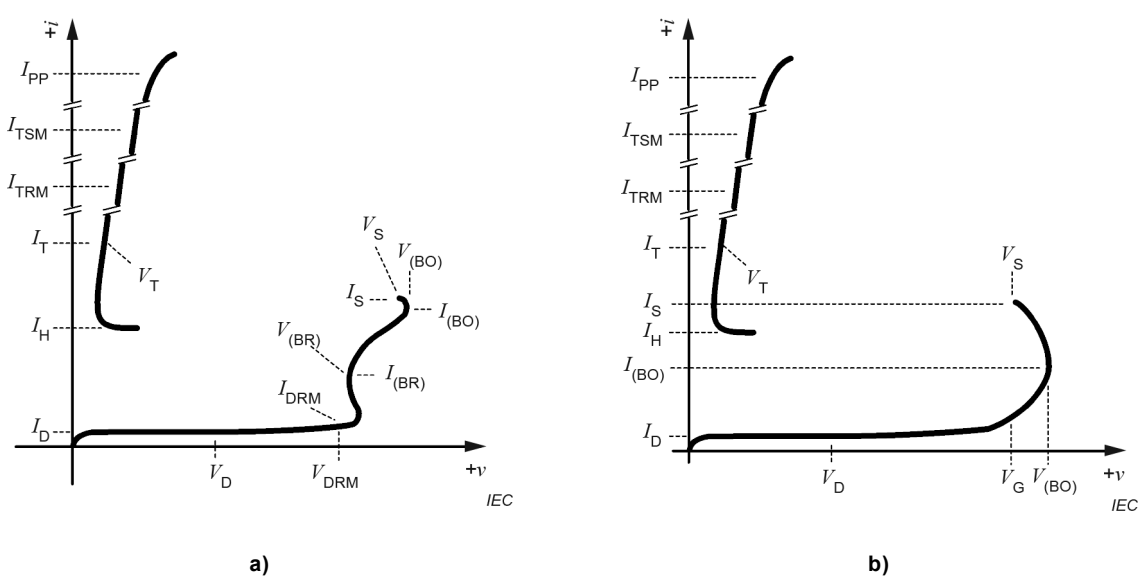
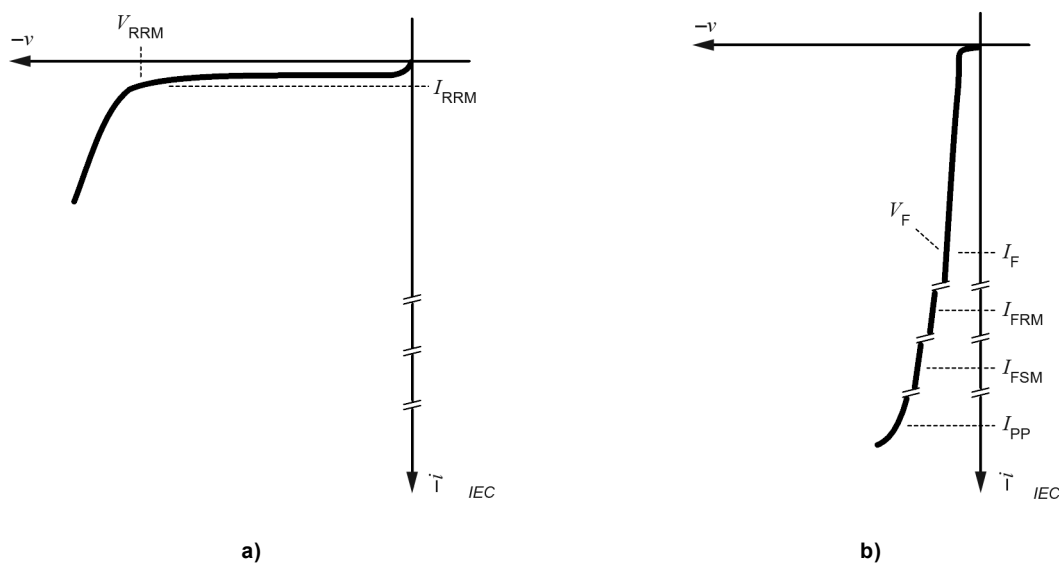
Figure 4 – Bidirectional: a) 2 terminal fixed voltage and b) gated

4 TSS types

The TSS is classified by the type of characteristic in the first and third quadrants, and the number of terminals (see Table 1). At least one quadrant will have a switching characteristic (see Figure 5). The other quadrant may have a switching, blocking or diode conduction characteristic (see Figure 5 and Figure 6). Thyristors with only one switching quadrant are called unidirectional and may have two (diode), three (triode) or four (tetraode) terminals. In addition, thyristors with two switching quadrants are called bidirectional.

Table 1 – Types of TSS

Number of terminals	Other quadrant characteristics		
	Blocking	Conducting	Switching
2 (diode)	Reverse blocking diode TSS Figure 1	Reverse conducting TSS Figure 1	Bidirectional diode TSS Figure 4
3 (triode)	Reverse blocking triode TSS P-gate or N-gate Figure 2	Reverse conducting triode TSS P-gate or N-gate Figure 3	Bidirectional triode TSS P-gate or N-gate or combined P-gate and N- gate (TRIAC) Figure 4
4 (tetraode)	Reverse blocking tetraode TSS P-gate and N-gate Figure 2		

**Figure 5 – Switching quadrant characteristics: a) fixed-voltage TSS and b) gated TSS****Figure 6 – TSS non-switching characteristics: a) reverse blocking b) reverse conducting**

5 Service conditions

5.1 Normal service conditions

The TSS is normally mounted inside an equipment or module which results in a micro-climate class condition (see IEC 60721-3-9[7]). A TSS which conforms to this document shall be suitable for stationary use at weather-protected locations (see IEC 60721-3-3[6]). In the absence of specific requirements, the TSS shall be suitable for operation under the following common service conditions and one or both of the two microclimates:

a) Normal microclimate

ambient air temperature within the range of 0 °C to 70 °C;

air pressure within the range of 80 kPa to 106 kPa;

relative humidity within the range of 25 % to 75 %.

b) Extended microclimate

ambient air temperature within the range of –40 °C to 85 °C;

air pressure within the range of 70 kPa to 106 kPa;

relative humidity 10 % to 95 %.

5.2 Storage temperature range, $T_{\text{stg min}}$ to $T_{\text{stg max}}$.

The temperatures over which the thyristor can be stored without any voltage applied has the following preferred temperature ranges (selected from IEC 60747-1[8] and IEC 60749[11])

0 °C to 125 °C

–55 °C to 125 °C

–65 °C to 150 °C

6 Mechanical requirements and identification

6.1 Robustness of terminations

If applicable, the user shall specify a suitable test from IEC 60068-2-21[3].

6.2 Solderability

Solder terminations shall meet the requirements of IEC 60068-2-20[2].

6.3 Marking

Legible and permanent marking shall be applied to the surge protective component, as necessary, to ensure that the user can determine the following information by inspection:

a) manufacturer;

b) year of manufacture;

c) component number or code.

If requested and agreed, the customer's identification should be marked on each component.

NOTE The necessary information can also be coded.

6.4 Documentation

Documents shall be provided by the manufacturer so that from the information in 6.3, the manufacturer can determine the following additional information:

a) appropriate component parameters as set out in this document;

- b) component mounting requirements and processes.
- c) ordering information

The following information should be supplied by the user:

- a) drawing giving all dimensions, finishes and termination details;
- b) type or model;
- c) quantity;
- d) quality assurance requirements.

7 Standard test methods

7.1 Failure rates

Sampling size, electrical characteristics to be tested, etc. should be covered by the quality assurance requirements, which are not covered by this document.

7.2 Test conditions

7.2.1 General

The rating and characteristic tests shall be performed on the TSS either as required by the application or as detailed in the component specification. The TSS shall be tested with the specified environmental conditions, such as temperature range and mounting configuration.

7.2.2 Standard atmospheric conditions

All room temperature electrical measurements, as well as recoveries followed by measurements, shall be carried out under the following conditions as recommended in Subclause 4.1 of IEC 60749-1:2002[11]:

- temperature: 20°C to 30°C;
- relative humidity 25 % to 75 %, where appropriate;
- air pressure 80 kPa to 106 kPa

Referee tests shall be carried out under the following standard atmospheric conditions (see 4.1 of IEC 60749-1:2002[11]):

- temperature: 24°C to 26°C;
- relative humidity 25 % to 75 %;
- air pressure 80 kPa to 106 kPa

Where the TSS parameters are tested over a temperature range, suitable values should be chosen from the list of recommended temperature values in IEC 60721-3-3:2019[6].

In the absence of special requirements, one of the following preferred semiconductor ambient temperature ranges should be used:

- normal 0 °C to 70 °C;
- extended –40 °C to 85 °C.

7.2.3 Measurement errors

Measurement errors can be caused by ground loops, common impedances, magnetic induction, electric induction and electromagnetic radiation. The voltage error caused by a circulating ground-loop current can be reduced by increasing the loop impedance. Normally this is done by clipping ferrite cores on to the probe cables. Common impedances can be avoided by using Kelvin contacts to the TSS for power and sense connections. Magnetic induction and inductive effects can be reduced by short lead lengths and minimizing the wiring loop area, possibly by using twisted wires. Electric induction (capacitive pick-up) can be removed by interposing a Faraday shield connected to a non-signal ground. Electromagnetic pick-up can be reduced by shielding and the techniques used for magnetic induction.

7.2.4 Measurement accuracy

Analogue oscilloscopes shall have rise times five times faster than the signal rise time. This ensures less than 2 % error in the displayed rise time. Digital oscilloscopes (refer to IEC 61083-1) shall have sample times at least $30/T_X$ where T_X is the time interval to be measured. A rated resolution of 0,4 % of full-scale deviation (2^{-8} full-scale deviation) or better is recommended for tests where only the impulse parameters are to be evaluated. For referee tests which require comparison of records, a rated resolution of 0,2 % of full-scale deviation (2^{-9} full-scale deviation) or better shall be used.

7.2.5 Designated impulse shape and values

The waveshape of an impulse is designated by a combination of two numbers. The first, represents the virtual front time (T_1) and the second the virtual time to half value on tail (T_2). It is written as T_1/T_2 , both in microseconds, the sign "/" having no mathematical meaning, see Annex A.

The quoted TSS current ratings are the short-circuit test generator values. Under test conditions, the actual thyristor current will be different, due to the interaction of the generator with the thyristor characteristic.

7.2.6 Multiple TSS

Where multiple TSS are packaged together, the application may simultaneously operate them. If the individual TSS parameters are significantly affected by the operation of the other TSS, then the testing shall emulate this condition as well as the single TSS operation.

7.2.7 Gated TSS testing

All fixed-voltage TSS tests shall be performed on a gated TSS to verify and determine the protection terminal performance. Gated TSS shall be tested with the appropriate values of gate bias voltage, V_{GG} , and of the network. Unless otherwise specified, the gate bias voltages used for testing shall be the maximum and minimum values of the intended application. For any tests where the gated TSS limits the voltage, the gate supply shall be low impedance (decoupled) and a TSS without internal gate blocking shall have an appropriately poled blocking diode connected directly in series with the gate terminal. When a gated TSS has been designed to give gate controlled and fixed-voltage protection, the fixed-voltage TSS tests shall also be performed with the gate open-circuited (i.e. $I_G = 0$).

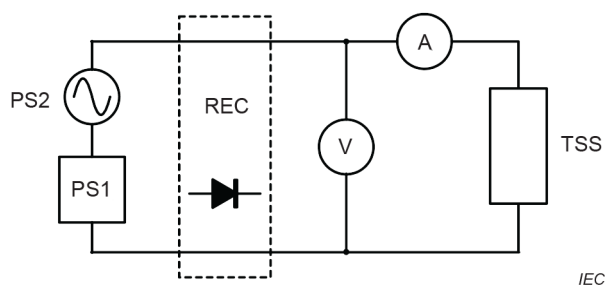
7.3 Rating test procedures

7.3.1 General

The overvoltage and overcurrent test levels used shall be from one or more of the IEC and ITU-T bibliographic references cited in the bibliography. These test levels may be modified to the final equipment level by including in the test circuit any of the surge coordinating components from the equipment.

7.3.2 Repetitive peak off-state voltage, V_{DRM}

The purpose of this test is to verify that the TSS maintains a high impedance off-state condition when continuously subjected to the rated repetitive peak off-state voltage. The rated value of repetitive peak off-state voltage, V_{DRM} , shall be applied across the TSS and the value of repetitive peak off-state current, I_{DRM} , measured during the test, conducted with a circuit functionally equivalent to Figure 7.



Key

TSS	TSS under test
A	ammeter, peak reading current monitor
V	voltmeter, mean, peak and AC reading
PS1	DC power supply set to the DC component of V_{DRM}
PS2	AC power supply set to the AC component of V_{DRM}
REC	full or half-wave rectifier circuit, used for unidirectional testing when the AC component of V_{DRM} reverses the polarity

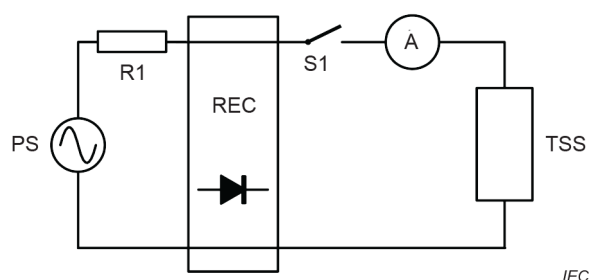
The measured current shall not exceed the maximum specified value of I_{DRM} . After the V_{DRM} test the TSS shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in TSS reliability. Each switching quadrant of the TSS shall be separately tested and measured.

Figure 7 – Test circuit for verifying repetitive peak off-state voltage (V_{DRM})

NOTE Large changes between pre- and post-test characteristics are a possible indication of TSS degradation.

7.3.3 Repetitive peak on-state current, I_{TRM}

The purpose of this test is to verify that the TSS can continuously conduct its rated repetitive peak (quasi-sinusoidal) on-state current without failure or exceeding the maximum rated junction temperature (see Figure 8).



Key

TSS	TSS under test
A	ammeter, peak reading current monitor
PS	AC power supply, set at specified voltage
R1	resistor, defines peak short-circuit current
S1	switch, closed to perform test
REC	full or half-wave rectifier circuit, connected for unidirectional testing

Figure 8 – Test circuit for verifying repetitive peak on-state current, I_{TRM}

The AC test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of waveshape and waveshape peak value. The capability of the generator shall ensure that the TSS will always switch into the on-state. Unidirectional TSS which are not rated for bidirectional current operation will require a bridge or half-wave rectifier to be added to the AC voltage source for full or half wave testing. During the I_{TRM} test, a temperature sensitive TSS parameter, such as I_H , can be monitored by means of an oscilloscope whose current and voltage probes are connected to the TSS in the manner shown in Figure 9.

The average working junction temperature can be calculated from the measured parameter values, the parameter temperature coefficient and the TSS initial temperature. After the I_{TRM} test, the TSS shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in TSS reliability.

NOTE Large changes between pre- and post-test characteristics are a possible indication of TSS degradation.

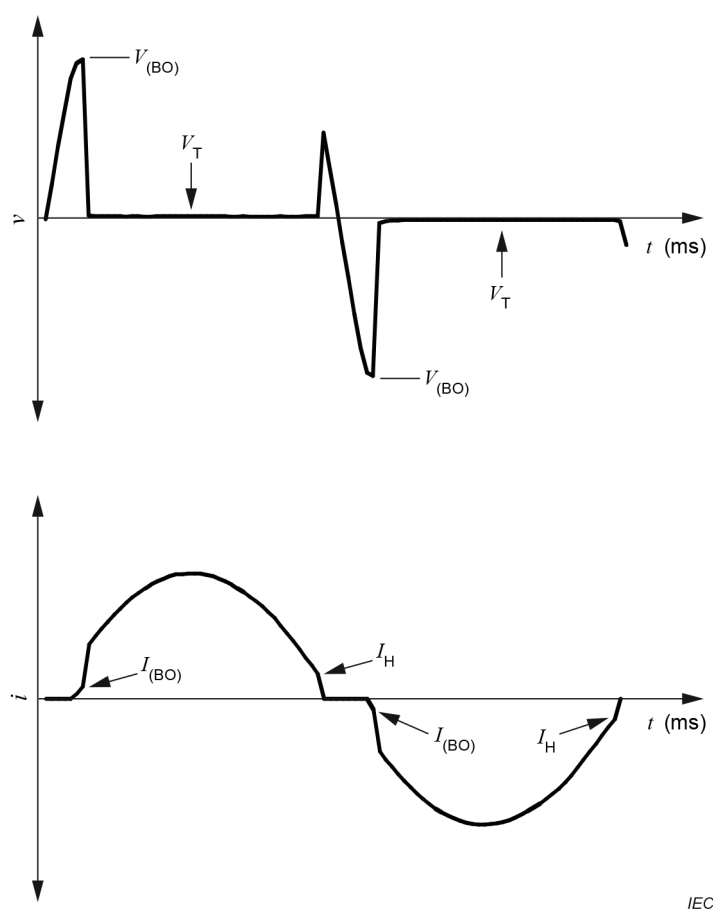
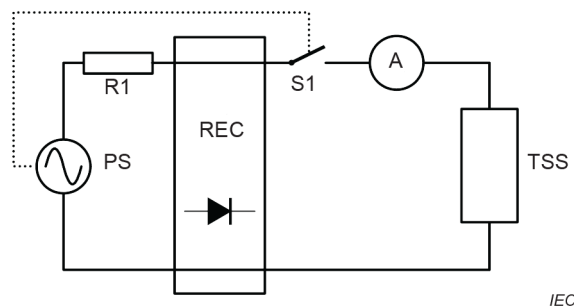


Figure 9 – Repetitive peak on-state current waveforms

7.3.4 Non-repetitive peak on-state current, I_{TSM}

The purpose of this test is to verify that the TSS can survive a specified duration of (quasi-sinusoidal) AC surge current without failure. The test circuit used shall be functionally equivalent to Figure 10.



Key

TSS	TSS under test
A	ammeter, peak reading current monitor
PS	AC power supply, set at specified voltage
R1	resistor, defines peak short-circuit current
S1	switch, closes for specified duration, operation synchronised to AC voltage zero crossings
REC	full or half-wave rectifier circuit, connected for unidirectional testing

Figure 10 – Test circuit for verifying non-repetitive peak on-state current, I_{TSM}

Switch S1 only opens or closes at the zero voltage crossings of the AC voltage source. This ensures that the TSS will be tested with half or full AC cycles. The AC test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of waveshape, waveshape peak value, and duration for which the switch S1 closes. The capability of the generator shall ensure that the TSS will always switch to the on-state. Unidirectional TSS which are not rated for bidirectional current operation, will require a bridge or half-wave rectifier to be added to the AC voltage source for full or half-wave testing. After switch S1 has operated for the specified test duration and the TSS has returned to thermal equilibrium conditions, the TSS shall not fail any of its specified characteristics.

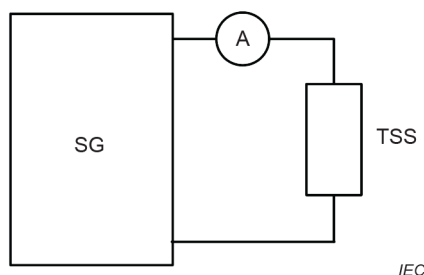
NOTE Large changes between pre- and post-test characteristics are a possible indication of TSS degradation.

The test duration may be specified as a time or number of AC cycles at a specified power frequency. A non-repetitive current rating test shall not be repeated until the TSS has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the TSS be capable of withstanding up to 100 such tests without failure during its lifetime. The I_{TSM} rating will vary with test duration time and several values may be needed to fulfil an application need; recommended time durations are one cycle at 0,1 s, 1 s and 10 s.

7.3.5 Non-repetitive peak pulse current, I_{PP}

The purpose of this test is to verify that a TSS can survive a specified impulse waveshape of short-circuit current amplitude I_{PP} without failure. The test circuit used shall be functionally equivalent to Figure 11. The impulse test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of waveshape and waveshape peak value. The capability of the generator shall ensure that the TSS will always switch to the on-state. After the impulse and after the TSS has returned to thermal equilibrium conditions, the TSS shall not fail any of its specified characteristics.

NOTE Large changes between pre- and post-test characteristics are a possible indication of TSS degradation.



Key

TSS	TSS under test
A	peak reading current monitor
SG	impulse generator with specified characteristics

Figure 11 – Test circuit for verifying non-repetitive peak pulse current, I_{PP}

Each switching quadrant of the TSS shall be separately tested and measured. A non-repetitive current rating test shall not be repeated until the thyristor has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the thyristor be capable of withstanding up to 100 such tests without failure during its lifetime. For the purpose of verification, a smaller number of tests may be preferred. The I_{PP} rating will vary with waveshape and several waveshape values may be needed to fulfil an application need. Annex A lists some waveshapes commonly used to test the TSS in telecommunication applications.

7.3.6 Repetitive peak reverse voltage, V_{RRM}

The purpose of this test is to verify that the TSS maintains a high impedance blocking state condition when continuously subjected to the rated repetitive peak reverse voltage. The rated value of repetitive peak reverse voltage, V_{RRM} , shall be applied across the TSS in its blocking direction and the value of repetitive peak reverse current, I_{RRM} , measured during the test using a circuit functionally equivalent to Figure 7. The measured current shall not exceed the maximum specified value of I_{RRM} . After the V_{RRM} test the TSS shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in TSS reliability.

NOTE Large changes between pre- and post-test characteristics are a possible indication of TSS degradation.

7.3.7 Non-repetitive surge forward current, I_{FSM}

The purpose of this test is to verify that the diode section of a forward or reverse conducting TSS can survive a specified duration of AC surge current without failure. The test method for non-repetitive peak on-state current, I_{TSM} (see 7.3.4 and Figure 10), shall be used for verifying the non-repetitive surge forward current, I_{FSM} . If the conduction period used is one full cycle or longer, then I_{TSM} (see 7.3.4) rather than I_{FSM} , is applicable. (I_{TSM} includes both diode and TSS conduction) After the I_{FSM} test and after the TSS has returned to thermal equilibrium conditions, the TSS shall not fail any of its specified characteristics.

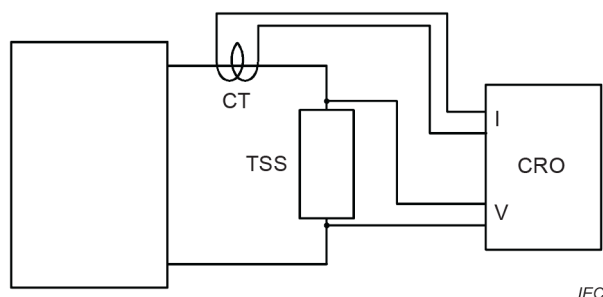
NOTE Large changes between pre- and post-test characteristics are a possible indication of TSS degradation.

7.3.8 Repetitive peak forward current, I_{FRM}

The purpose of this test is to verify that the diode section of a forward or reverse conducting TSS can continuously conduct the rated repetitive peak forward current without failure or exceeding the maximum rated junction temperature. The test method for repetitive peak on-state current, I_{TRM} (see 7.3.3 and Figure 8), shall be used for verifying the repetitive peak forward current, I_{FRM} . In the absence of special requirements, it is recommended that I_{TRM} shall be specified instead of I_{FRM} , where I_{TRM} includes both diode and thyristor conduction.

7.3.9 Critical rate of rise of on-state current, di/dt

The purpose of this test is to verify that a TSS can survive a fast rising current, as may occur on the wavefront of an impulse. The test circuit used shall be functionally equivalent to Figure 12.



Key

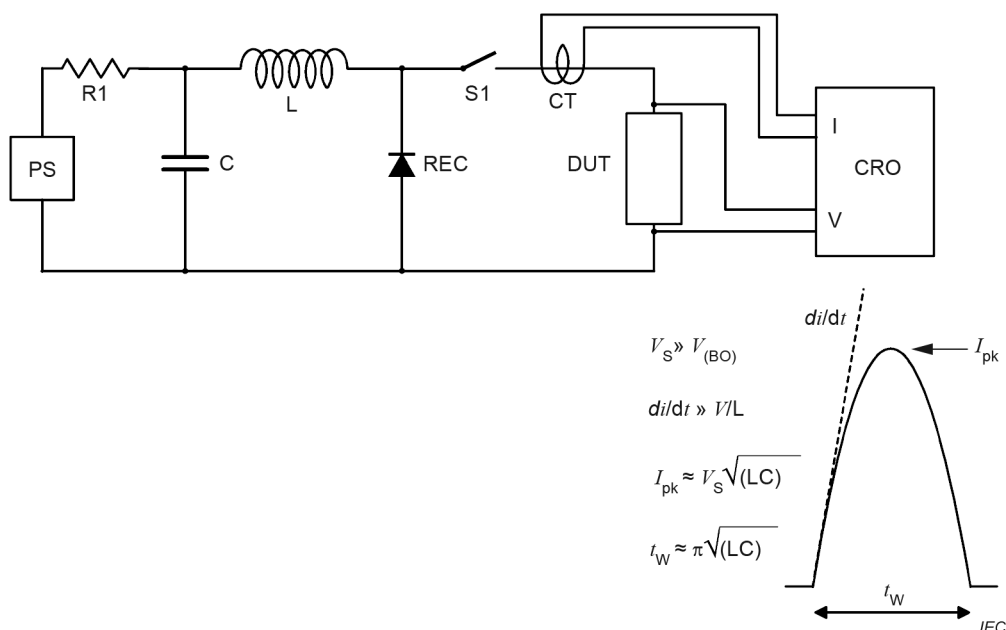
TSS	TSS under test
CT	current transformer or equivalent
RG	ramp generator with specified di/dt
CRO	dual-channel oscilloscope or equivalent

Figure 12 – Test circuit for verifying critical rate of rise of on-state current (di/dt)

Voltage, V , and current, I , monitors (typically a digital or storage oscilloscope with voltage and current probes) are used to record the circuit conditions. After applying the di/dt impulse to the thyristor, and when it has returned to thermal equilibrium conditions, the thyristor shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of thyristor degradation.)

The di/dt test generator shall be specified for wavefront di/dt and peak (crest) current and waveshape (normally the wave tail will be relatively short). It is essential that the correct waveform is used for this test and the thyristor manufacturer should be contacted for the test circuit and waveform details. In the absence of special requirements, it is recommended that a generator based on the standard thyristor di/dt test circuit be used. The basic circuit diagram and its waveforms are shown in Figure 13.

Each switching quadrant of the TSS shall be separately tested and measured. A non-repetitive current rating test shall not be repeated until the thyristor has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the thyristor shall be capable of withstanding up to 100 such tests, in each test polarity, without failure, during its lifetime. For the purpose of verification a smaller number of tests may be preferred.



Key

TSS	TSS under test
CT	current transformer or equivalent
PS	DC power supply, set to V_S
R1	resistor, limits charging current
S1	switch, closes to start test; opens at current zero crossing
REC	rectifier circuit, conducts negative current
C	capacitor, energy storage and timing
L	inductor, sets di/dt
CRO	dual-channel oscilloscope or equivalent

Figure 13 – Half sine-wave di/dt test circuit

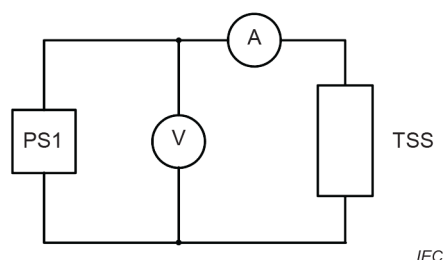
7.4 Characteristic test procedures

7.4.1 General

The overvoltage and overcurrent test levels used to establish the protection voltage shall be from one or more of the IEC and ITU-T bibliographic references cited in Annex E. These test levels may be modified to the final equipment level by including in the test circuit any of the surge coordinating components from the equipment.

7.4.2 Off-state current, I_D

The purpose of this test is to determine the off-state current of a TSS when biased at a specified DC off-state voltage. The test circuit used shall be functionally equivalent to Figure 14. The voltage output of the DC supply shall be ramped from zero to the specified value of DC off-state voltage, V_D , at a rate below the minimum value of the critical rate of rise of off-state voltage. The DC voltage is applied until the value of off-state current, I_D , stabilises. The final value of I_D shall be measured. Unless specified otherwise, each switching quadrant of the TSS shall be separately tested and measured.

**Key**

TSS	TSS under test
A	microammeter
V	DC voltmeter
PS1	DC power supply ramped to V_D

Figure 14 – Test circuit for off-state current, I_D at V_D **7.4.3 Repetitive peak off-state current, I_{DRM}**

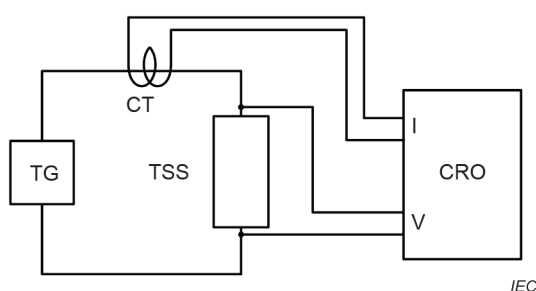
The purpose of this test is to determine the peak off-state current of a TSS when biased at the specified repetitive peak off-state voltage. The rated value of the repetitive peak off-state voltage, V_{DRM} , shall be impressed across the thyristor and the value of thyristor repetitive peak off-state current, I_{DRM} , measured during the test using a circuit functionally equivalent to Figure 7. Unless specified otherwise, each switching quadrant of the TSS shall be separately tested and measured.

7.4.4 Repetitive peak reverse current, I_{RRM}

The purpose of this test is to determine the peak reverse current of a reverse blocking TSS when biased at the specified repetitive peak reverse voltage. The rated value of repetitive peak reverse voltage, V_{RRM} , shall be applied across the thyristor in its blocking quadrant and the peak value of thyristor repetitive peak reverse current, I_{RRM} , measured during a test using a circuit functionally equivalent to Figure 7.

7.4.5 Breakover voltage, $V_{(BO)}$ and current, $I_{(BO)}$

The purpose of this test is to determine the breakover of a TSS at a specified ramp rate. The test circuit used shall be functionally equivalent to Figure 15. The test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of rate of rise, waveshape, waveshape peak value, and, for AC testing, duration. Alternatively, the test generator circuit diagram shall be given. The peak voltage, $V_{(BO)}$, that occurs across the TSS in switching from the off-state to the on-state shall be measured (see Figure 16 to Figure 19). For multiple cycle AC testing, the measured value shall be the highest value of all individual cycle $V_{(BO)}$ values. The corresponding instantaneous thyristor current, $I_{(BO)}$, at $V_{(BO)}$ shall also be measured for a power frequency voltage ramp rate (see Figure 17 and Figure 19).



Key

TSS	TSS under test
CT	DC current probe or equivalent
TG	test generator with specified characteristics switching TSS from off-state to on-state
CRO	dual channel oscilloscope or equivalent

EXAMPLE The test generator, TG, used to obtain figures 16 to 19 consists of a current source and a shunt 300 Ω resistor. Starting from zero, the current source ramped to 3 A at 3, 33 A/ms (1 000 V/ms open-circuit voltage); the current then stepped to 5 A for 200 μ s before dropping down to 2 A, after which the current ramped to zero at a rate of 0,2 A/ms. This “sequence” test exercises the component around its characteristic, enabling measurement of $V_{(BO)}$, $I_{(BO)}$, V_S , I_S , V_T and I_H values, as appropriate, for the component.

Figure 15 – Test circuit for breakover, $V_{(BO)}$ and $I_{(BO)}$ and on-state voltage, V_T

Figure 16 to Figure 19 show the switching quadrant voltage and current waveforms of the two TSS types: fixed-voltage and gated. Expanded sections of the overall wave form detail the clamping, on-state and switch-off conditions. (Figure 5 shows the two thyristor types (fixed voltage and gated) in terms of the principal voltage-current switching characteristic) The waveforms shown illustrate the thyristor type generic waveshapes and these should not be taken as typical values.

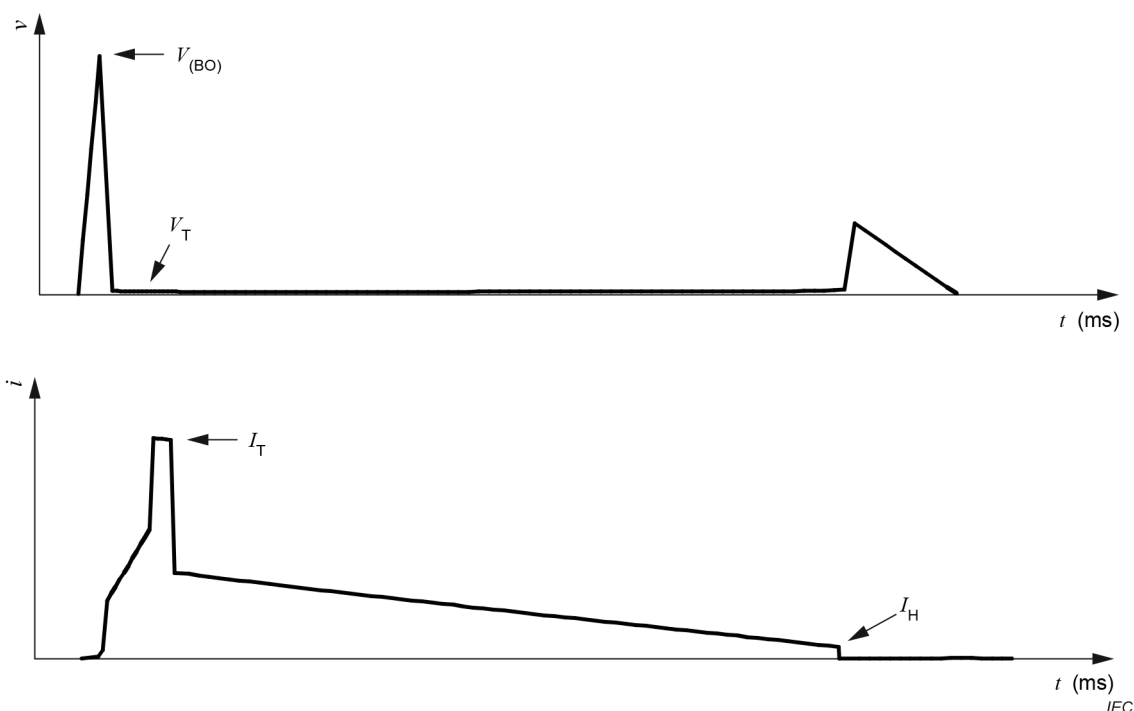


Figure 16 – Voltage and current waveforms versus time for a fixed-voltage TSS showing switch-on, on-state and switch-off events

Each switching quadrant of the TSS shall be separately tested and measured. Multiple cycle AC testing of unidirectional TSS shall be carried out with either full wave or half wave rectified AC, as required by the application. The $V_{(BO)}$ and $I_{(BO)}$ values will vary with rate of rise and several ramp rates may be needed to fulfil an application need. In the absence of special requirements, it is recommended that one or more of the rates of rise shown in Table 2 be used for testing.

Table 2 – Breakover ramp rate test values

Application	dv/dr (open-circuit)	Source resistance R	di/dr (short-circuit)
Slow ramp	4 V/ms	500 Ω (positive slope) 4 000 Ω (negative slope)	8 mA/ms 1 mA/ms
AC	250 V/ms	250 Ω	1 A/ms
Slow wavefront impulse	100 V/ μ s	100 Ω	1 A/ μ s
Fast wavefront impulse	1 000 V/ μ s	100 Ω	10 A/ μ s

7.4.6 On-state voltage, V_T

The purpose of this test is to determine the on-state voltage of a TSS at a specified current; this voltage value is used to calculate the on-state power loss. The test circuit used shall be functionally equivalent to Figure 15. The test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of waveshape and waveshape peak value. Alternatively, the test generator circuit diagram shall be given.

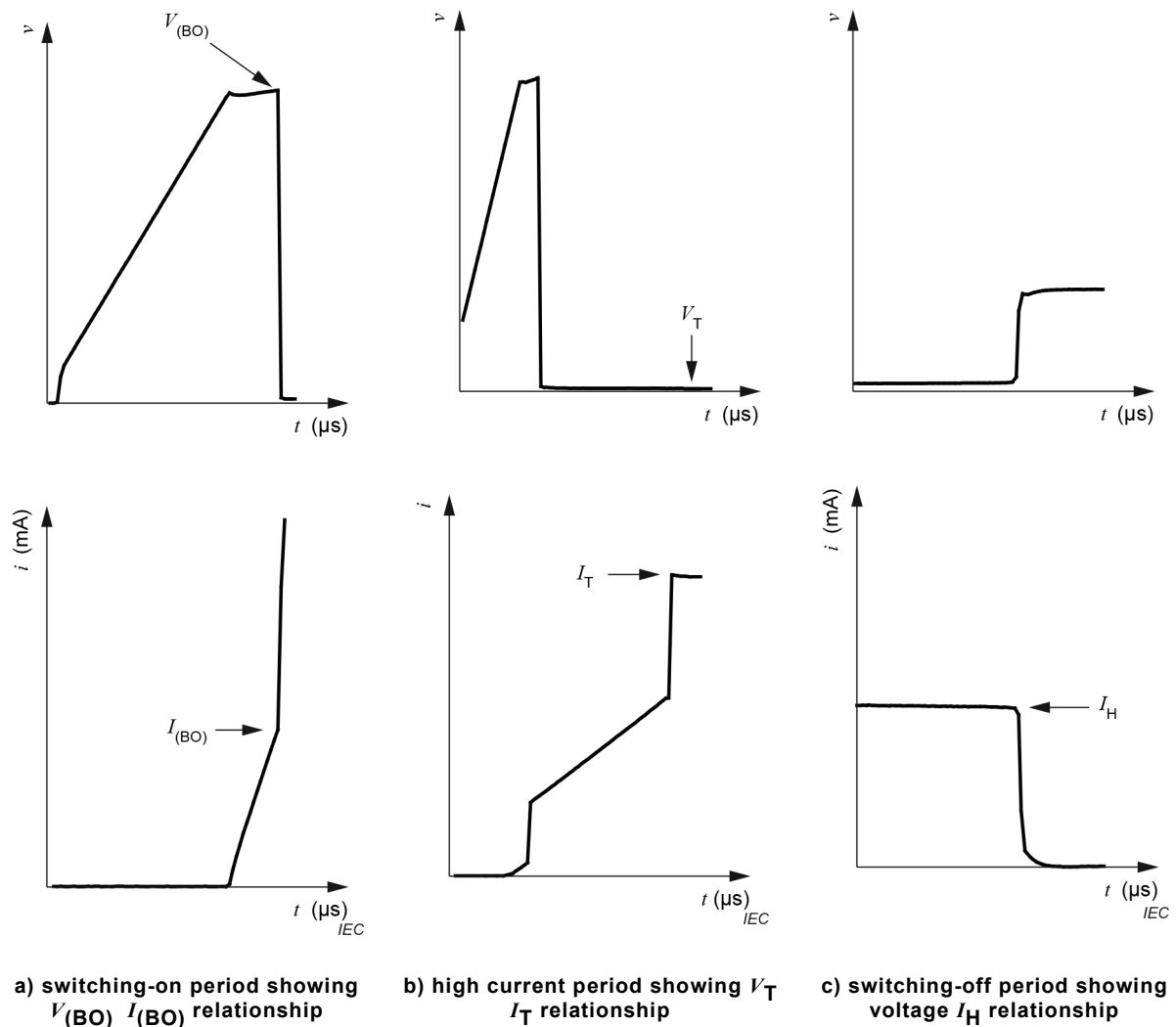


Figure 17 – Waveform expansions of Figure 16

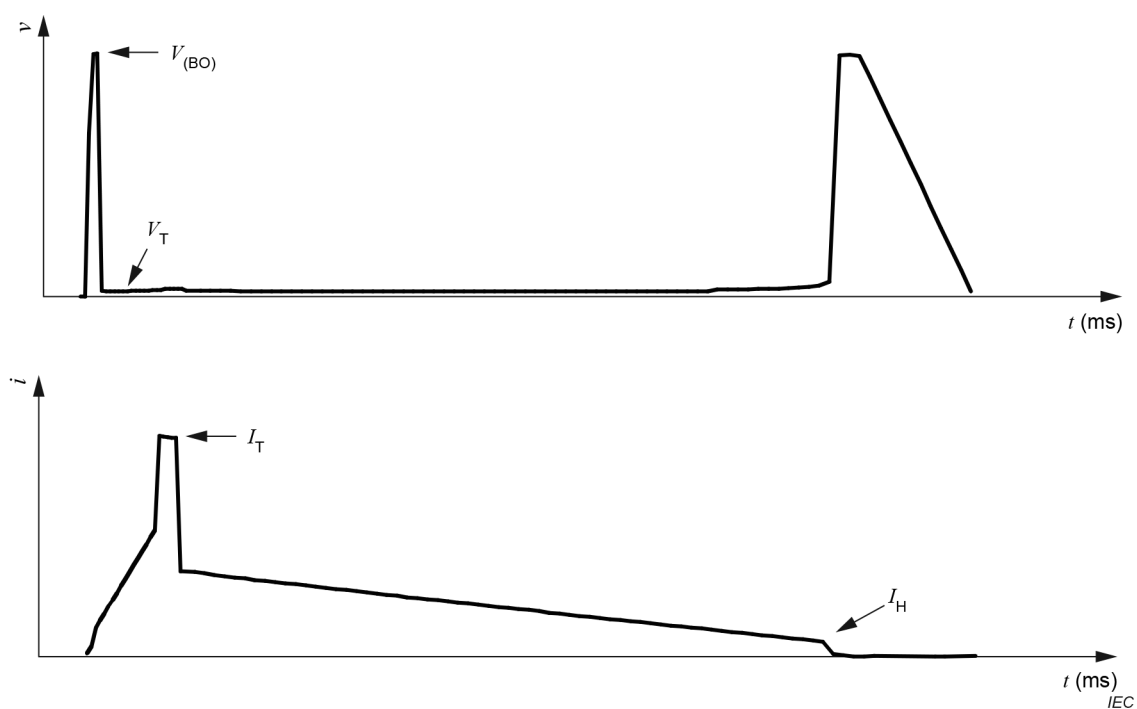


Figure 18 – Voltage and current waveforms versus time for a gated TSS showing switch-on, on-state and switch-off events

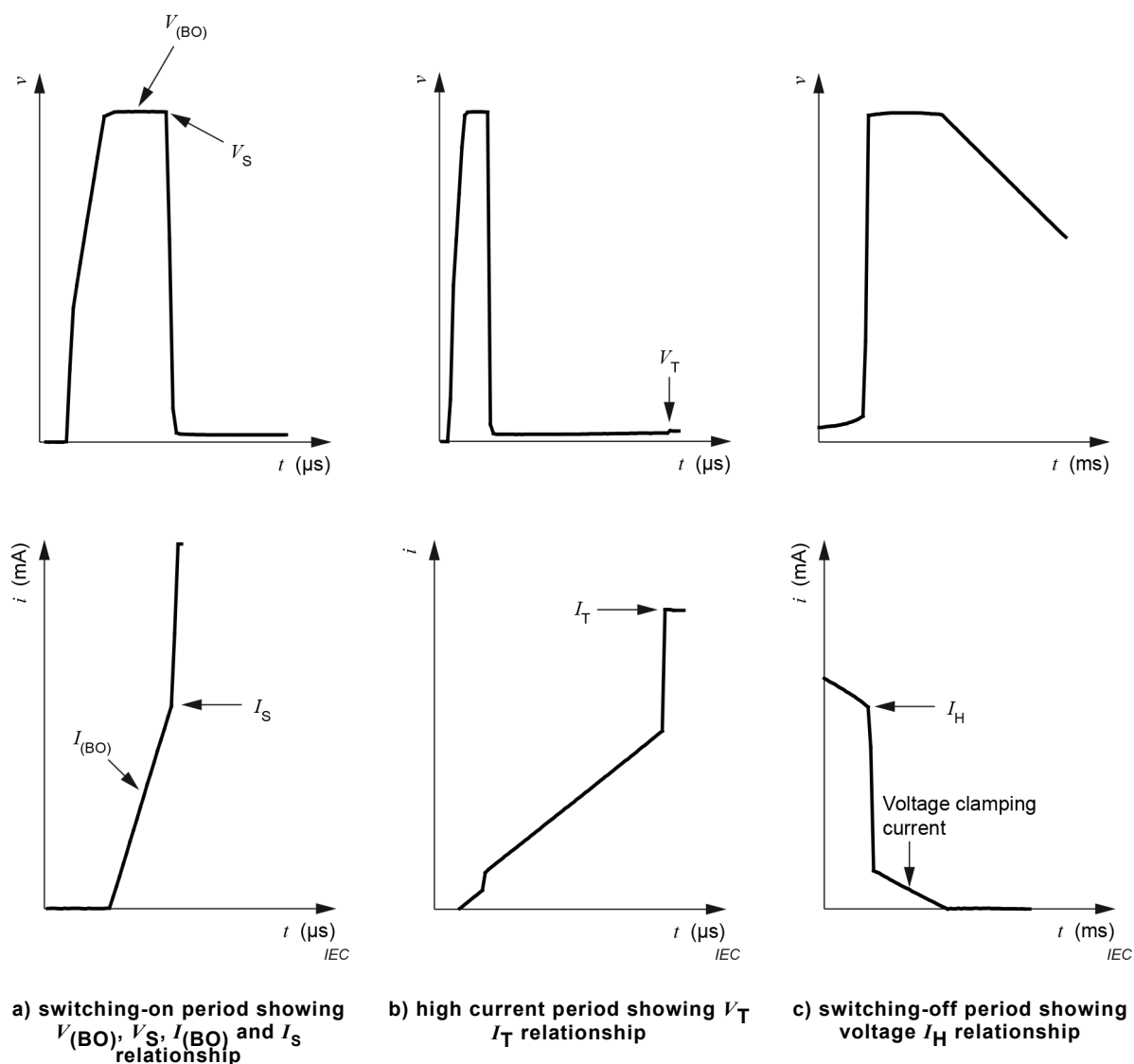
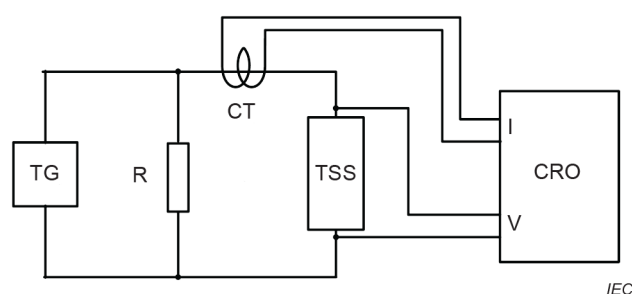


Figure 19 – Waveform expansions of Figure 18

The generator shall switch the TSS into the on-state condition and the value of on-state voltage, V_T , shall be measured at a specified time and value of on-state current, I_T (see V_T waveforms of Figure 17 and Figure 19).

Each switching polarity of the TSS shall be separately tested and measured. The value of V_T will vary with the value of I_T and time. A low and high current value of V_T may be required to cover AC and impulse operation.

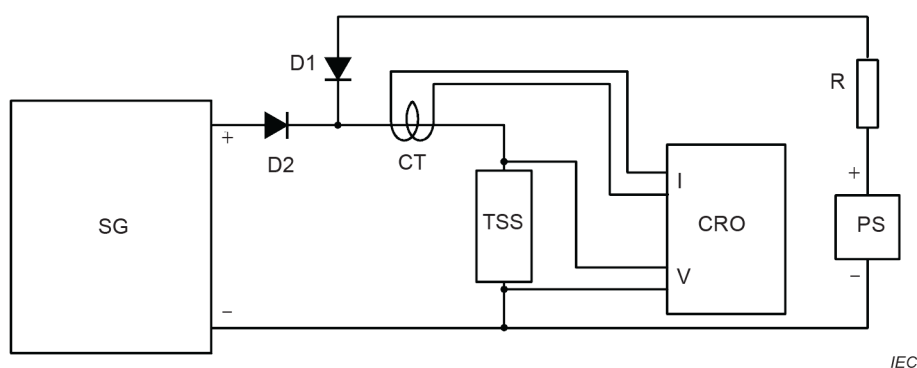
**Key**

TSS	TSS under test
CT	DC current probe or equivalent
TG	test generator with specified characteristics switching TSS to a specified on-state current, I_T , and then reducing the current at a specified di/dt to cause switch-off
R	resistor to define source resistance (if required)
CRO	dual channel oscilloscope or equivalent

Figure 20 – Test circuit for holding current, I_H **7.4.7 Holding current, I_H**

The purpose of this test is to determine the holding current of a TSS. The test circuit used shall be functionally equivalent to Figure 20. The test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of waveshape, and waveshape peak value. The generator shall switch the TSS into a specified on-state condition and then ramp down the on-state current until the thyristor switches off (see I_H waveforms of Figure 17 and Figure 19). Switch-off is determined when the thyristor voltage value exceeds a specified threshold level. The instantaneous value of the extrapolated ramp when this occurs is measured as the holding current. This established approach measures the current at which the thyristor switches off, rather than the current at which the thyristor just maintains its on-state. In most applications, the need is for a switching value rather than a holding value.

When an impulse generator is used as the test generator, its output voltage may be too low at the holding current level for adequate discrimination of the switch-off point. To increase the switch-off voltage level, the generator and a current (less than the minimum specified value of I_H) from a DC voltage supply ($< V_{DRM}$) should be connected via diodes D2 and D1 respectively to the TSS (see Figure 21, diodes D2 and D1 prevent any reverse current flow into either the PS or SG). Each switching quadrant of the TSS shall be separately tested and measured.



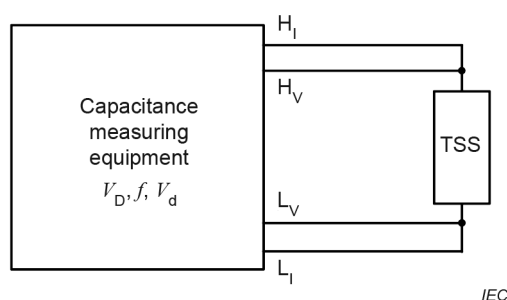
Key

TSS	TSS under test
CT	DC probe or equivalent
SG	impulse generator with specified characteristics
PS	DC voltage power supply, set to specified voltage
R	resistor to define DC source resistance
D1	isolating diode for PS
D2	isolating diode for SG
CRO	dual channel oscilloscope or equivalent

Figure 21 – Test circuit for holding current with additional DC bias

7.4.8 Off-state capacitance, C_o

The purpose of this test is to determine the off-state capacitance of a TSS under specified conditions. The test circuit used shall be functionally equivalent to Figure 22. The TSS off-state capacitance, C_o , shall be measured at specified DC (V_D) and AC (V_d and f) bias levels. In the absence of special requirements, it is recommended that an AC bias level of $V_d = 1$ V rms at a frequency of $100 \text{ kHz} < f < 1 \text{ MHz}$ be used. The DC bias level should be -2 V and any other levels that are representative of the intended application.

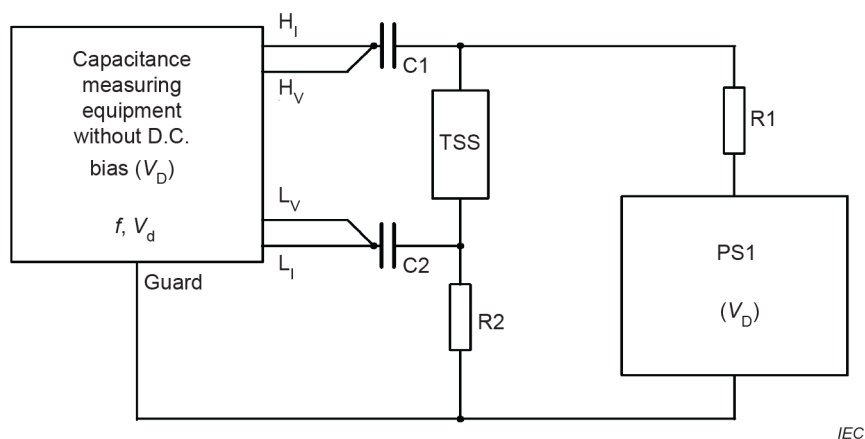


Key

TSS	TSS under test
H_v	H_v , voltage sense
H_i	H_i , current feed
L_v	L_v , voltage sense
L_i	L_i , current return

Figure 22 – Test circuit for capacitance measurement

If the capacitance measuring equipment cannot supply the required DC bias voltage, the circuit arrangement shown in Figure 23 can be used.

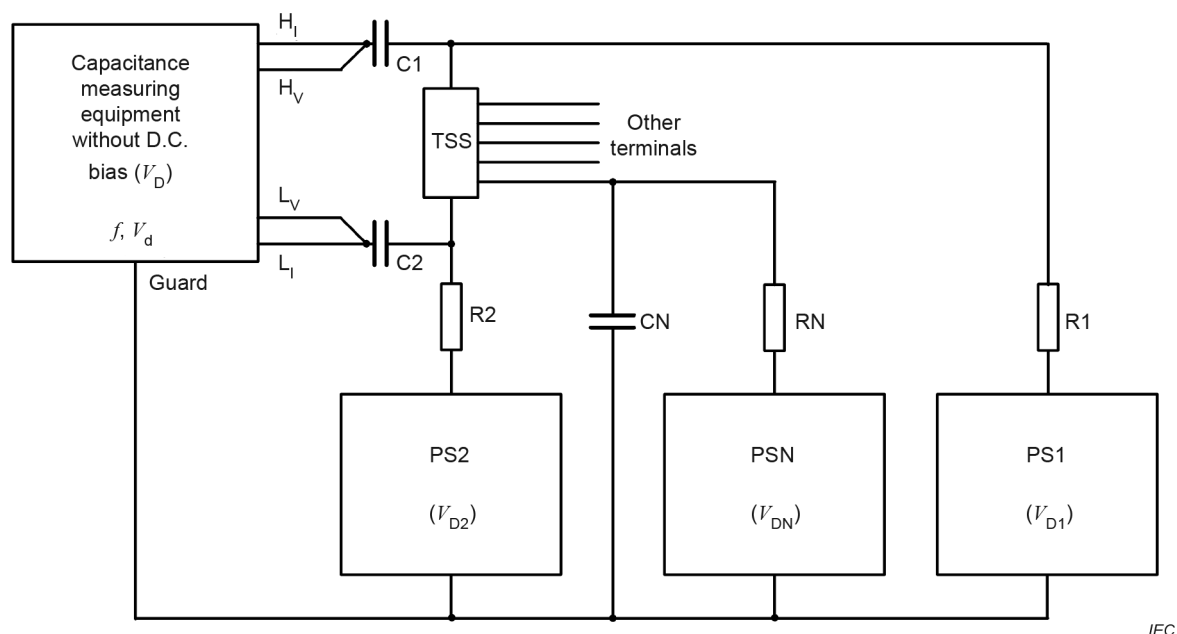


Key

- TSS TSS under test
- $C1, C2$ DC blocking capacitors, $C1 = C2 \gg C_o$
- $R1, R2$ DC feed resistors, $R1 = R2 \ll V_D / I_D$
- $PS1$ variable voltage DC power supply set to V_D
- H_V H_I , voltage sense
- H_{II} H_I , current feed
- L_V L_X , voltage sense
- L_I L_O , current return
- Guard Guard ground terminal (nulls components connected to the terminal from the measurement)

Figure 23 – Test circuit for capacitance measurement with external DC bias

Where a TSS has three terminals, the unmeasured terminal shall be nulled from the capacitance measurement and DC biased at levels that are representative of the intended application (see Figure 24). The same measurement technique may be used for multiple TSS, which are packaged together and have four or more terminals, provided the nulled elements are directly between the measured and nulled terminals (see Figure 24). This measurement technique will not work if more than one of the nulled elements connect to an internal (non-terminal) node of the measured terminal pair.



IEC

Key

TSS	TSS under test
C1, C2...C _N	DC blocking capacitors, $C_1 = C_2 \dots = C_N \gg C_O$
R1, R2...R _N	DC feed resistors, $R_1 = R_2 \dots = R_N \ll V_D / I_D$
PS1, PS2...PS _N	variable voltage DC power supply set for V_{D1} , V_{D2} , ... V_{DN}
H _V	H _I , voltage sense
H _I	H _X , current feed
L _V	L _O , voltage sense
L _I	L _O , current return
Guard	guard ground terminal (nulls components connected to the terminal from the measurement)

Figure 24 – Test circuit for capacitance measurement of multi-terminal TSS

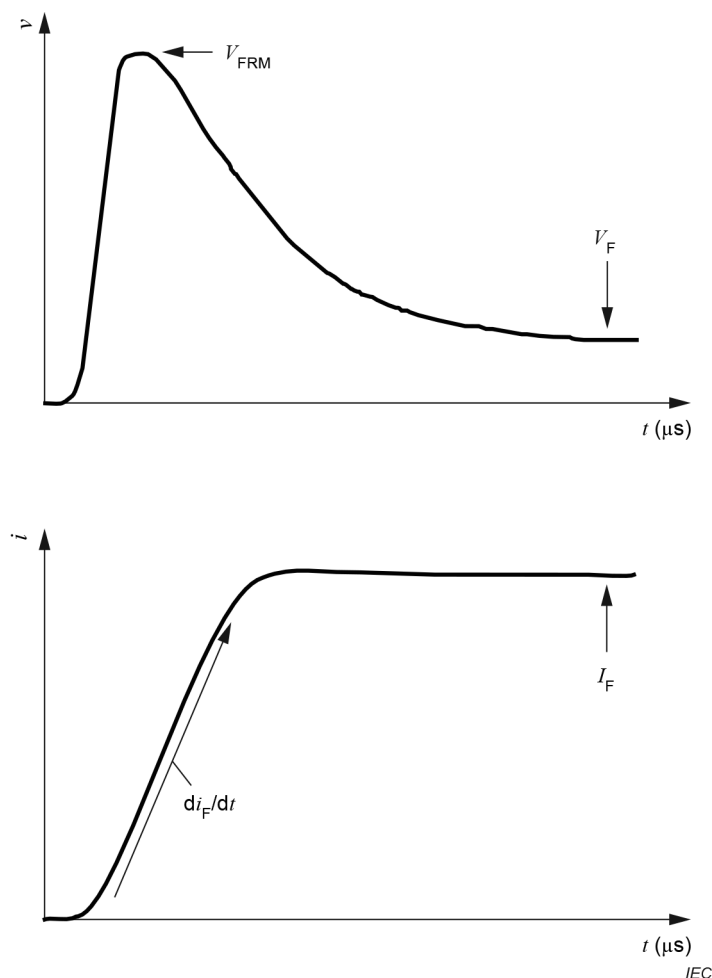


Figure 25 – Diode voltage and current waveforms versus time showing V_{FRM} and rising current di/dt

7.4.9 Forward voltage, V_F

The purpose of this test is to determine the forward voltage of a forward conducting TSS at a specified current; this voltage value is used to calculate the forward power loss. The test circuit and waveforms used shall be consistent with those used for the determination of on-state voltage, V_T (Figure 15). The generator shall switch the TSS into forward conduction and the value of forward voltage, V_F , shall be measured at a specified time or value of forward current, I_F . Rapidly rising current waveforms may generate an additional forward recovery voltage; this should not be included in the V_F measurement (see Figure 25).

A low and high current value of V_F may be required to cover AC and impulse operation.

7.4.10 Peak forward recovery voltage, V_{FRM}

The purpose of this test is to determine the peak forward voltage of a forward conducting TSS under the condition of a fast rising current wavefront; this voltage value is the maximum stress on the protected circuitry. The test circuit and levels used shall be consistent with those used for the determination of fast impulse breakover voltage, $V_{(BO)}$ (see Figure 15). The generator shall switch the diode section on at a specified rate of forward current rise, dI_F/dt , and the value of peak forward recovery voltage, V_{FRM} , shall be measured (see Figure 25). In the absence of special requirements, it is recommended that the fast impulse rate of rise shown in Table 2, 1 000 V/μs and 10 A/μs, shall be used for testing.

7.4.11 Critical rate of off-state voltage rise, dv/dt

The purpose of this test is to verify that the TSS will not turn on as a result of fast rising system voltages with peak amplitudes less than the V_{DRM} rating. A specified voltage ramp equal to the minimum value of critical dv/dt and of amplitude V_{DRM} shall be applied to the unenergized TSS. The peak ramp voltage shall be maintained for a period of at least 50 μs . The TSS shall not switch on, even partially, during the test. The voltage ramp can be of exponential or linear. For the exponential ramp of Figure 26, the dv/dt value is calculated as $0,632 \cdot V_{\text{DRM}}/t$.

where

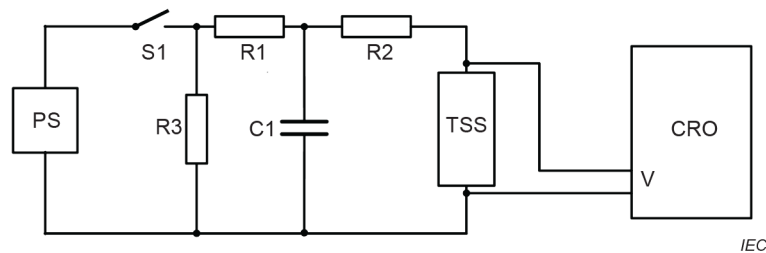
t is the time from the ramp start until the voltage rises to $0,632 \cdot V_{\text{DRM}}$.

For a linear ramp, the dv/dt value is calculated as $0,8 \cdot V_{\text{DRM}} / (t_{90} - t_{10})$

where

t_{10} and t_{90} are the times at which the voltage has risen to $0,1 \cdot V_{\text{DRM}}$ and $0,9 \cdot V_{\text{DRM}}$, respectively.

Each switching polarity of the TSS shall be separately tested and measured



Key

TSS	TSS under test	R2	current limit resistor if TSS switches
PS	DC voltage power supply	R3	discharge resistor after S1 opens
S1	start test switch	C1	charging capacitor
R1	charging resistor	CRO	oscilloscope or equivalent

Figure 26 – Test circuit for exponential critical rate of off-state voltage rise, dv/dt

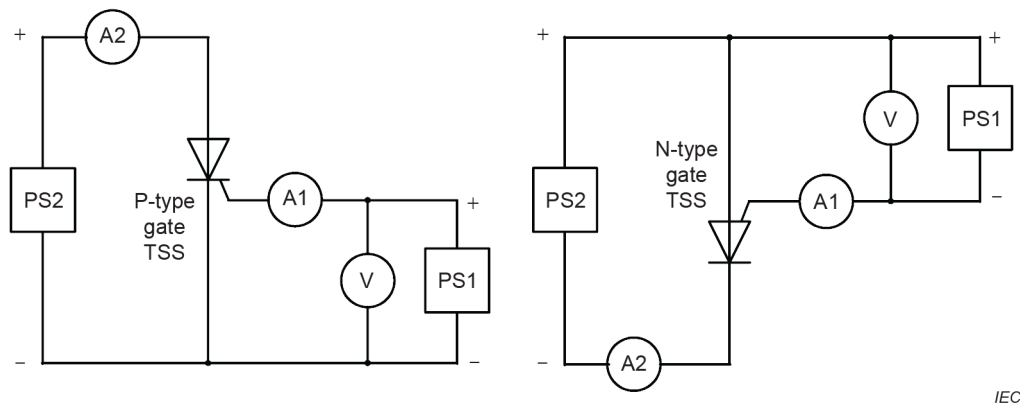
7.4.12 Variation of holding current with temperature

The purpose of this test is to determine how the holding current, I_H of a TSS, varies with temperature to ensure that the thyristor will always switch off. The value of I_H (see 7.4.7) shall be measured over the specified operating temperature range and expressed as a graph of current versus temperature.

7.4.13 Gate-to-adjacent terminal peak off-state voltage and peak off-state gate current, V_{GDM} , I_{GDM}

The purpose of this test is to determine the maximum value of gate-to-adjacent terminal voltage of a TSS that will maintain the protection terminals in a high impedance off-state condition at a specified voltage. Using the appropriate circuit of Figure 27, the specified value of V_D shall be applied across the thyristor protection terminals and the value of gate-to-adjacent terminal voltage increased from zero until the protection terminal current, I_D , reaches its specified value. The measured value of gate-to-adjacent terminal voltage is V_{GDM} and the measured gate current is I_{GDM} .

Each gated switching polarity of the TSS shall be separately tested and measured. The repetitive peak off-state voltage of a gated TSS is $V_{GG} + V_{GDM}$; this is equivalent to a fixed-voltage TSS V_{DRM} .



IEC

Key

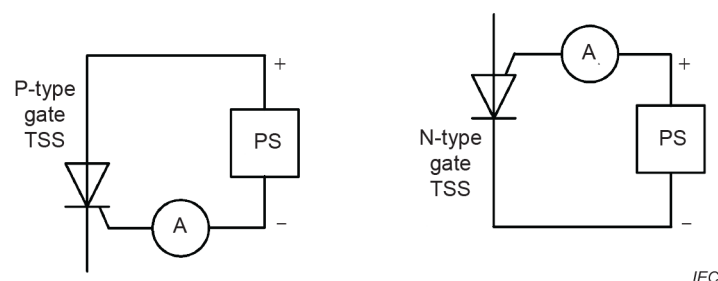
TSS	TSS under test
A1	ammeter, measures gate current
A2	ammeter, I_D monitor
V	voltmeter, measures gate to adjacent terminal voltage
PS1	variable DC voltage supply, set for a specified value of I_D
PS2	DC voltage power supply, set to V_D

Figure 27 – Test circuit for gate-to-adjacent terminal peak off-state voltage and current, V_{GDM} and I_{GDM}

7.4.14 Gate reverse current, adjacent terminal open, I_{GAO} , I_{GKO}

The purpose of this test is to determine the current drain on the gate terminal voltage supply when the adjacent terminal is open-circuited. Using the appropriate circuit of Figure 28, the specified value of gate bias, V_{GG} , shall be applied to the gate and the current through the gate measured. This test determines the reverse gate to anode off-state current, I_{GAO} , of a P-gate thyristor with the cathode terminal open or the reverse gate to cathode off-state current, I_{GKO} , of an N-gate thyristor with the anode open.

Each gated switching polarity of the TSS shall be separately tested and measured.



IEC

Key

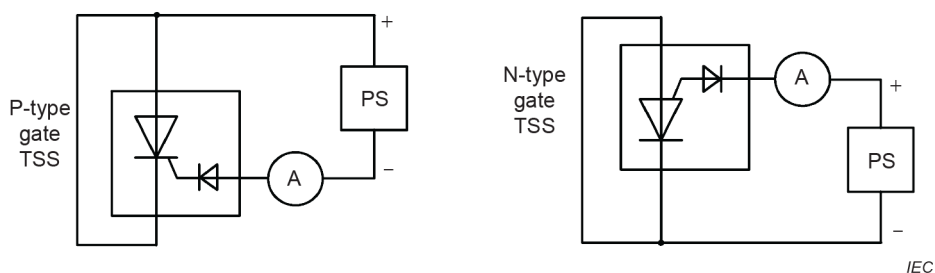
TSS	TSS under test
A	ammeter, for reverse gate current
PS	DC power supply, set at specified gate voltage, V_{GG}

Figure 28 – Test circuit for gate reverse current, adjacent terminal open, I_{GAO} , I_{GKO}

7.4.15 Gate reverse current, main terminals short-circuited, I_{GAS} , I_{GKS}

The purpose of this test is to determine the current drain on the gate terminal voltage supply when the adjacent terminal is shorted to the other protection terminal. Using the appropriate circuit of Figure 29, the specified value of gate bias, V_{GG} , shall be applied to the gate and the current through the gate measured. This test determines the reverse gate off-state current, I_{GAS} , of a P-gate thyristor with the cathode shorted to the anode or the reverse gate off-state current, I_{GKS} , of an N-gate thyristor with the anode shorted to the cathode.

Each gated switching polarity of the TSS shall be separately tested and measured. This test is specific to thyristors with integrated gate blocking diodes.



Key

TSS	TSS under test
A	ammeter, for reverse gate current
PS	DC power supply, set at specified gate voltage, V_{GG}

Figure 29 – Test circuit for gate reverse current, main terminals short-circuited, I_{GAS} , I_{GKS}

Annex A (informative)

Common impulse waveshapes

A.1 General

This Annex covers:

- Types of impulse generator
- Impulse generator parameters
- Impulse generators typically used for surge protector testing

A.2 Types of impulse generator

Impulse generators can be classified into three types:

- Generators with a defined voltage waveform typically used for high-voltage insulation testing
- Generators with a defined current waveform typically used for high-current component and thyristor testing
- Generators with defined voltage and current waveforms. These generators can be subdivided into:
 - Circuit defined generators
 - Waveform defined generators

A.3 Impulse generator parameters

A.3.1 Glossary of terms

The following terms are used in this Annex to describe the impulse and generator parameters.

A.3.1.1

virtual front time

T_1

<voltage impulse> 1/0,6 times the interval T between the instants when the impulse is 30 % and 90 % of the peak value [1]

<surge current impulse> 1,25 times the interval T between the instants when the impulse is 10 % and 90 % of the peak value [16]

Note 1 to entry: Some standards use the 10 % and 90 % front time measurement for the voltage impulse.

A.3.1.2

virtual origin

O_1

<impulse voltage waveform> instant at which a straight line drawn through the 30 % and 90 % amplitude values crosses the time axis [1]

<impulse current waveform> instant at which a straight line drawn through the 10 % and 90 % amplitude values crosses the time axis [16]

A.3.1.3**virtual time to half-value** T_2

interval of time between the instant of virtual origin O_1 and the instant when the voltage or current has decreased to half the peak value [1], [16]

A.3.1.4**designation of an impulse shape**

combination of two numbers, the first representing the virtual front time (T_1) and the second the virtual time to half-value on the tail (T_2) [4]

Note 1 to entry: It is written as T_1/T_2 , both in microseconds, the sign "/" having no mathematical meaning.

Note 2 to entry: Some standards use alternative designations such as A/B or $T_1 \times T_2$.

Note 3 to entry: Combination wave generators have both voltage and current impulse designations given separated by a hyphen e.g. 1,2/50-8/20.

Note 4 to entry: Waveshapes defined as maximum front time and minimum time to half value are expressed as $<T_1/> T_2$.

A.3.1.5**undershoot**

peak value of an impulse voltage or current that passes through zero in the opposite polarity of the initial peak [17]

A.3.1.6**charge (impulse)**

time integral of the impulse current

A.3.1.7 **I^2t (impulse)**

time integral of the square of the impulse current

Note 1 to entry: I^2t is called the action integral for atmospheric lightning, joule integral for fuses and specific energy (W/R) for AC surge protectors.

Note 2 to entry: The units for I^2t are A^2s , but assuming the current flows in a virtual 1 Ω resistor may be expressed in energy units J (fuses) or W/Ω (AC surge protectors).

A.3.1.8**combination wave generator**

generator with 1,2/50 μs open-circuit voltage waveform and respectively 8/20 μs short-circuit current waveform

A.3.1.9**effective impedance (impulse generator)**

quotient of the generator open-circuit peak voltage value and the generator short-circuit peak current value

Note 1 to entry: Some standards use the alternative term fictive impedance.[15]

A.3.2 Virtual parameters

This clause covers the virtual (calculated) waveform parameters and their applicability. Figure A.1 shows an impulse designation based on the extrapolation of the 10 % to 90 % front-time levels. All current lightning surge impulses in this document use the 10 % to 90 % front-time designation. The Telcordia $<2/>10$, $<10/>250$, $<10/>360$ and $<10/>1\ 000$ [21] impulse generators uniquely use the 10 % to 90 % front-time designation for the voltage impulse. All other impulse generators use a 30 % to 90 % front-time designation for the voltage impulse. The 8/20 current waveform is not necessarily unidirectional and has a maximum undershoot value specified.

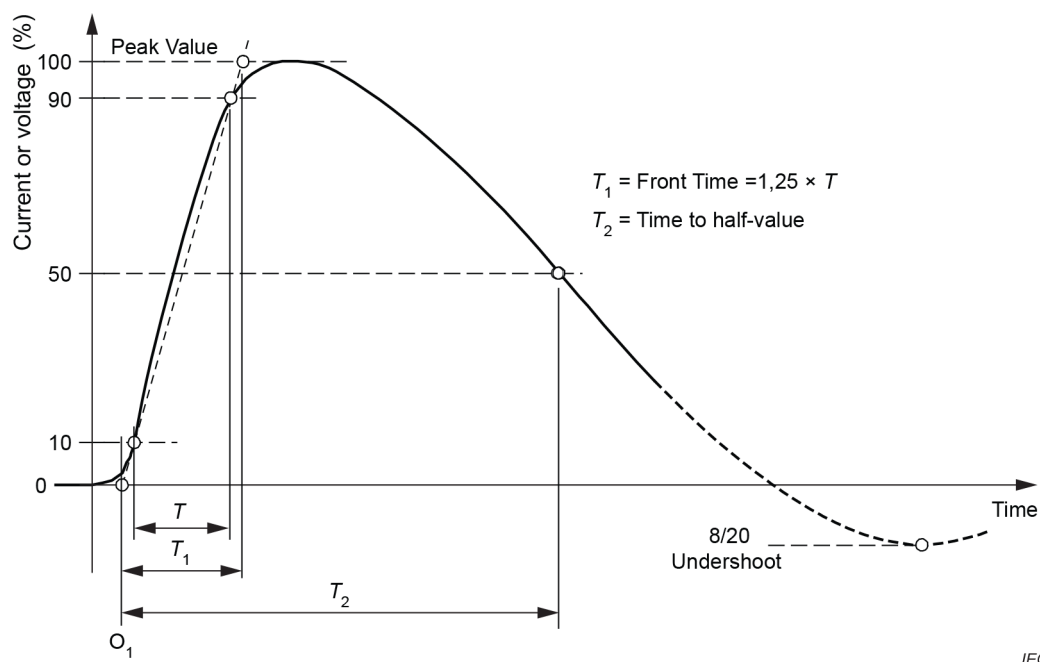


Figure A.1 – Current or voltage impulse amplitude versus time showing a 10 % to 90 % T_1 front time and T_2 time to half value

Figure A.2 shows a voltage impulse designation based on the extrapolation of the 30 % to 90 % front-time. All 30 % to 90 % front-time designated voltage impulses use nominal time values. The 30 % to 90 % front-time measurement is used to give more consistent measurement values. The start of the voltage impulse often includes high frequency noise resulting from the generator switch closure. The waveform ringing could extend into the 10 % amplitude region, causing variations in the 10 % to 90 % front-time measurement. Moving the 10 % level to 30 % avoided these initial aberrations.

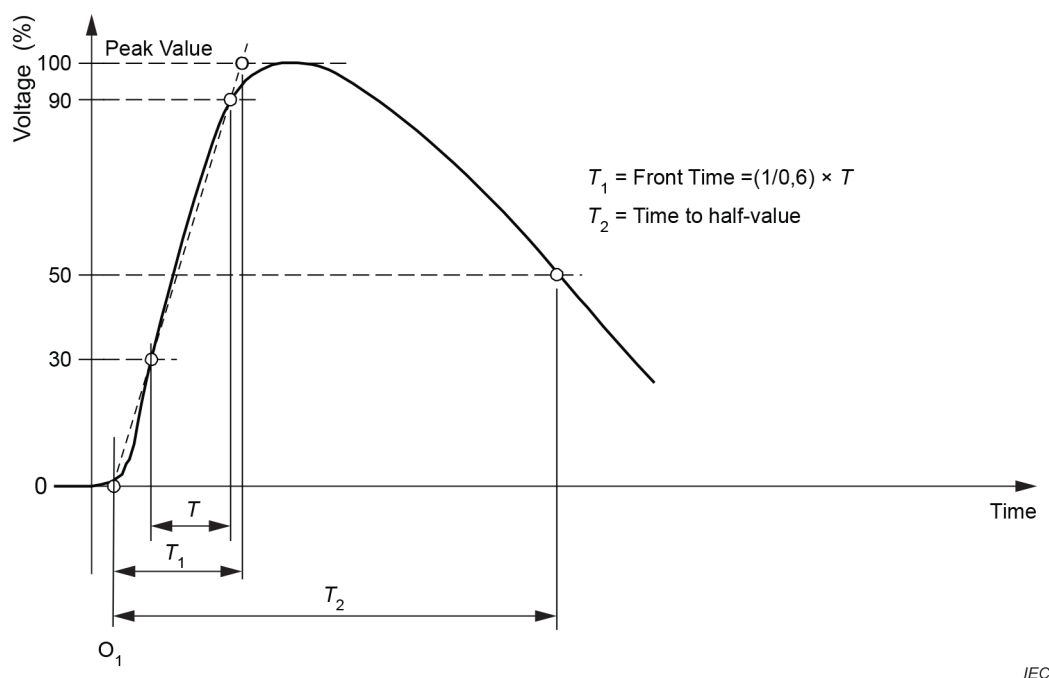


Figure A.2 – Voltage impulse amplitude versus time showing a 30 % to 90 % T_1 front time and T_2 time to half value

A.4 Impulse generators typically used for surge protector testing

A.4.1 General

This clause lists commonly used or referenced impulse generators. Table A.1, Table A.2 and Table A.3 cover generator types with voltage, current and voltage & current defined waveforms. A bibliographic reference is given for each designation of generator. Where there are duplicate designations, the most commonly used one is indicated.

A.4.2 Impulse generators with a defined voltage waveform

These generators are used for the high-voltage insulation/dielectric testing of components, devices and equipment. Capacitive loads will slow down the voltage front time. To compensate for capacitive loads above 5 nF, some generators have a selectable output resistance value and may even change the generator discharging capacitor value. Inductive loads, such as transformers, motor windings and electrical generator windings require the careful design of the waveshaping network to avoid ringing on the voltage impulse. The generator design objective is to produce a precision voltage impulse. The generator design must be robust enough to survive the discharge current caused by any insulation breakdown. Generator #1 is the most commonly used variant of generators #1 and #2.

Table A.1 – Voltage impulse generators

Number	Designation	Condition	Edge	Time and Tolerance	Amplitude
1	1,2/50 [17] [1]	Open-Circuit Voltage	Front	1.2 μs ±30 %	±3 %
			Decay	50 μs ±20 %	
		Short-Circuit Current	See NOTE		
2	1,2/50 [18] [12]	Open-Circuit Voltage	Generator circuit defined		−0% to +5%
		Short-Circuit Current	See NOTE		
NOTE Current waveshape not defined.					

A.4.3 Impulse generators with a defined current waveform

These generators are used for high-current component and component testing.

The 8/20 waveform is typically produced by an LCR series circuit that has a damping factor of less than one. Such a design requires that the load voltage is kept to be much smaller than the charging voltage, e.g. a 1:10 voltage ratio. These generators produce a current through the load with an 8/20 waveshape, unlike the 1,2/50-8/20 generator which has its current waveform measured into a short-circuit.

The amount of energy developed in an MOV or fuse is governed by the applied waveform. The possible range in developed energy is reduced by tighter waveform tolerances. Generator #3 is the preferred and most commonly used one because it has a $\pm$ 10 % waveform tolerance compared the $\pm$ 20 % of generator #4.

Generator #5 has its current waveform expressed as charge and I^2t values which can be simulated by a 10/350 waveform.

Table A.2 – Current impulse generators

Number	Designation	Condition	Edge	Time and Tolerance	Amplitude
3	8/20 [17] [16] [14]	Open-Circuit Voltage	See NOTE		
		Short-Circuit Current	Front	8 μs ±10 %	±10 % 0 to -20 % undershoot
			Decay	20 μs ±10 %	
4	8/20 [16]	Open-Circuit Voltage	See NOTE		
		Short-Circuit Current	Front	8 μs ±20 %	±10 % 0 to -30 % undershoot
			Decay	20 μs ±20 %	
5	10/350 [14]	Open-Circuit Voltage	See NOTE		
		Short-Circuit Current, I_{imp}	Waveform charge 0,5* I_{imp} C –10 % to +20 %		±10 %
			Waveform I^2t 0,25*(I_{imp}) ² A ² s –10 % to +45 %.		
NOTE Voltage waveshape not defined. Usually the peak charging voltage for the specified current value is given.					

A.4.4 Generators with defined voltage and current waveforms

The 1.2/50-8/20 generator #7 is commercially available and established in test laboratories. Although generator #8 might be referenced most people would use generator #7 for testing.

A similar situation exists for the 10/1000 impulse generators #11 and #12. Generator #11 is commercially available and established in test laboratories. Although generator #12 might be referenced most people would use generator #11 for testing.

For the 10/700 generators, #9 and #10, the choice is application dependent. For telecommunications applications the ITU-T generator #10 [19] is the automatic choice and most commonly available both commercially and in test laboratories. General EMC work will often reference the IEC generator #9 [13]. The IEC generator #10 is available commercially, but is possible to use the ITU-T generator with extra series resistors.

Table A.4 lists additional generators from Telcordia [21] and the TIA [22]. There are two different versions of the <2/>10 generator and a third variant of the “10/700” generator #19, which in practice is similar to the ITU-T #10 [19].

Table A.3 – Voltage and current impulse generators

Number	Designation	Condition	Edge	Time and Tolerance	Amplitude
6	1,2/50-8/20 (1,2/50-7,3/22) [20] See NOTE 1	Open-Circuit Voltage	Front	1,2 μs ± 30 % μs	± 10 %
			Decay	50 μs ± 20 %	
		Short-Circuit Current	Front	8 μs -31 % to +13 %	± 10 %
			Decay	20 μs -20 % to +40 %	
7	1,2/50-8/20 [21] [13] See NOTE 2	Open-Circuit Voltage	Front	1,2 μs ± 30 %	± 10 %
			Decay	50 μs ± 20 %	
		Short-Circuit Current	Front	8 μs ± 20 %	± 10 % 0 to -30 % undershoot
			Decay	20 μs ± 20 %	
8	<10/>250 [21]	Open-Circuit Voltage	Front	10 μs -60 % to 0	0 % to +16 %
			Decay	250 μs 0 to +60 %	
		Short-Circuit Current	Front	10 μs -30 % to 0	0 % to +16 %
			Decay	250 μs 0 to +20 %	
9	10/700 [13] See NOTE 3	Open-Circuit Voltage	Front	10 μs ± 30 %	0 % to +15 %
			Decay	700 μs ± 20 %	
		Short-Circuit Current	Front	5 μs ± 20 %	0 % to +15 %
			Decay	320 μs ± 20 %	
10	10/700 [19] [12] See NOTE 4	Open-Circuit Voltage	Front	10 μs ± 30 %	± 10 %
			Decay	700 μs ± 20 %	
		Short-Circuit Current	Front	5 μs ± 20 %	± 10 %
			Decay	320 μs ± 20 %	
11	<10/>1000 [21]	Open-Circuit Voltage	Front	10 μs -40 % to 0	0 to +15 %
			Decay	1000 μs 0 to +50 %	
		Short-Circuit Current	Front	10 μs -40 % to 0	0 to +15 %
			Decay	1000 μs 0 to +50 %	
12	10/1000 [20]	Open-Circuit Voltage	Front	10 μs -50 % to 0	± 10 %
			Decay	1000 μs 0 to +100 %	
		Short-Circuit Current	Front	10 μs -50 % to 0	± 10 %
			Decay	1000 μs ± 20 %	

NOTE 1 The #6 1,2/50-8/20 generator effective impedance is $2 \Omega \pm 12,5$ % [20].

NOTE 2 The #7 1,2/50-8/20 generator effective impedance is $2 \Omega \pm 10$ % [13].

NOTE 3 The #9 10/700 generator [19] short-circuit current waveshape is 5/320 for single output and 5/320 for dual output. The dual output current tolerance is 5 μs ± 20 % front, 320 μs ± 20 % duration and ± 10 % amplitude.

NOTE 4 The #10 10/700 generator [19] short-circuit current waveshape is 5/320 for single output and 4/250 for dual output. The dual output current tolerance is 4 μs ± 20 % front, 250 μs ± 20 % duration and ± 10 % amplitude.

Table A.4 – Other voltage and current impulse generators

Number	Designation	Condition	Edge	Time and Tolerance	Amplitude
13	<2/>10 [21] See NOTE 1	Open-Circuit Voltage	Front	2 μs -50 % to 0	0 % to +20 %
			Decay	10 μs 0 to +70 %	
		Short-Circuit Current	Front	2 μs -50 % to 0	0 % to +20 %
			Decay	10 μs 0 to +70 %	
14	<2/>10 [22] See NOTE 2	Open-Circuit Voltage	Front	2 μs -50 % to 0	0 % to +10 %
			Decay	10 μs 0 to +90 %	
		Short-Circuit Current	Front	2 μs -50 % to 0	0 % to +25 %
			Decay	10 μs 0 to +90 %	
15	<10/>160 [22] See NOTE 3	Open-Circuit Voltage	Front	10 μs -40 % to 0	0 % to +10 %
			Decay	160 μs 0 to +63 %	
		Short-Circuit Current	Front	10 μs -50 % to 0	0 % to +15 %
			Decay	160 μs 0 to +31 %	
17	<10/>360 [21]	Open-Circuit Voltage	Front	10 μs -25 % to 0	0 % to +15 %
			Decay	360 μs 0 to +30 %	
		Short-Circuit Current	Front	10 μs -25 % to 0	0 % to +15 %
			Decay	360 μs 0 to +30 %	
18	<10/>560 [22] See NOTE 4	Open-Circuit Voltage	Front	10 μs -40 % to 0	0 % to +10 %
			Decay	560 μs 0 to +54 %	
		Short-Circuit Current	Front	10 μs -50 % to 0	0 % to +15 %
			Decay	560 μs 0 to +36 %	
19	“10/700” [22]	Open-Circuit Voltage	Front	9 μs ±30 %	0 to +10 %
			Decay	720 μs ±20 %	
		Short-Circuit Current	Front	5 μs ±30 %	0 to +10 %
			Decay	320 μs ±20 %	
NOTE 1 The #13 <2/>10 generator effective impedances are 5 Ω, 8 Ω, 10 Ω or 15 Ω depending on application [21].					
NOTE 2 The #14 <2/>10 generator effective impedance is 2.5 Ω [22].					
NOTE 3 The #15 <10/>160 generator effective impedance is 7.5 Ω to each output [22]					
NOTE 4 The #17 <10/>560 generator effective impedance is 8 Ω [22]					