

INTERNATIONAL STANDARD



**Fibre optic active components and devices – Package and interface standards –
Part 21: Design guidelines of electrical interface of PIC packages using silicon
fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array
(S-FLGA)**



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CONTENTS

FOREWORD	3
1 Scope	5
2 Normative references	5
3 Terms and definitions	5
4 Terminal position numbering	6
5 Code of package nominal dimensions	6
6 Symbols and drawings	6
7 Dimensions and tolerances	9
Bibliography	14
Figure 1 – S-FBGA and S-FLGA outline	8
Figure 2 – Mechanical gauge drawing	9
Figure 3 – Array of terminal-existence areas	9
Table 1 – Dimensions and tolerances	10
Table 2 – Combination list of D , E , M_D , and M_E for $e = 0,30$ mm pitch S-FBGA (informative)	12
Table 3 – Combination list of D , E , M_D , and M_E for $e = 0,25$ mm pitch S-FLGA	13

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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PACKAGE AND INTERFACE STANDARDS –****Part 21: Design guidelines of electrical interface of PIC
packages using silicon fine-pitch ball grid array (S-FBGA)
and silicon fine-pitch land grid array (S-FLGA)**

FOREWORD

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This redline version of the official IEC Standard allows the user to identify the changes made to the previous edition IEC 62148-21:2019. A vertical bar appears in the margin wherever a change has been made. Additions are in green text, deletions are in strikethrough red text.

IEC 62148-21 has been prepared by subcommittee 86C: Fibre optic systems and active devices, of IEC technical committee 86: Fibre optics. It is an International Standard.

This second edition cancels and replaces the first edition published in 2019. This edition constitutes a technical revision.

This edition includes the following significant technical change with respect to the previous edition: specification of an electric guard band area around the optical terminal area, so as to allow applications with electric signals at higher symbol rates (e.g. 50 Gbaud and 100 Gbaud).

The text of this International Standard is based on the following documents:

CDV	Report on voting
86C/1684/CDV	86C/1710/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62148 series, published under the general title *Fibre optic active components and devices – Package and interface standards*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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FIBRE OPTIC ACTIVE COMPONENTS AND DEVICES – PACKAGE AND INTERFACE STANDARDS –

Part 21: Design guidelines of electrical interface of PIC packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA)

1 Scope

This part of IEC 62148 covers the design guidelines of the electrical interface for photonic integrated circuit (PIC) packages using silicon fine-pitch ball grid array (S-FBGA) and silicon fine-pitch land grid array (S-FLGA). In this document, the electrical interface for the S-FBGA package is informative.

The purpose of this document is to specify adequately the electrical interface of PIC packages composed of optical transmitters and receivers that enable mechanical and electrical interchangeability of PIC packages.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-731, *International Electrotechnical Vocabulary – Chapter 731: Optical fibre communication* (available at www.electropedia.org)

IEC TR 61931, *Fibre optic – Terminology*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-731, IEC TR 61931 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1

silicon fine-pitch ball grid array S-FBGA

device composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer balls on the dielectric layer(s), and outer balls with heights more than 0,1 mm

~~Note to entry: This note only applies to the French language.~~

3.2

silicon fine-pitch land grid array

S-FLGA

device composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer lands on the dielectric layer(s), and outer lands with heights of 0,1 mm or less

~~Note to entry: This note only applies to the French language.~~

4 Terminal position numbering

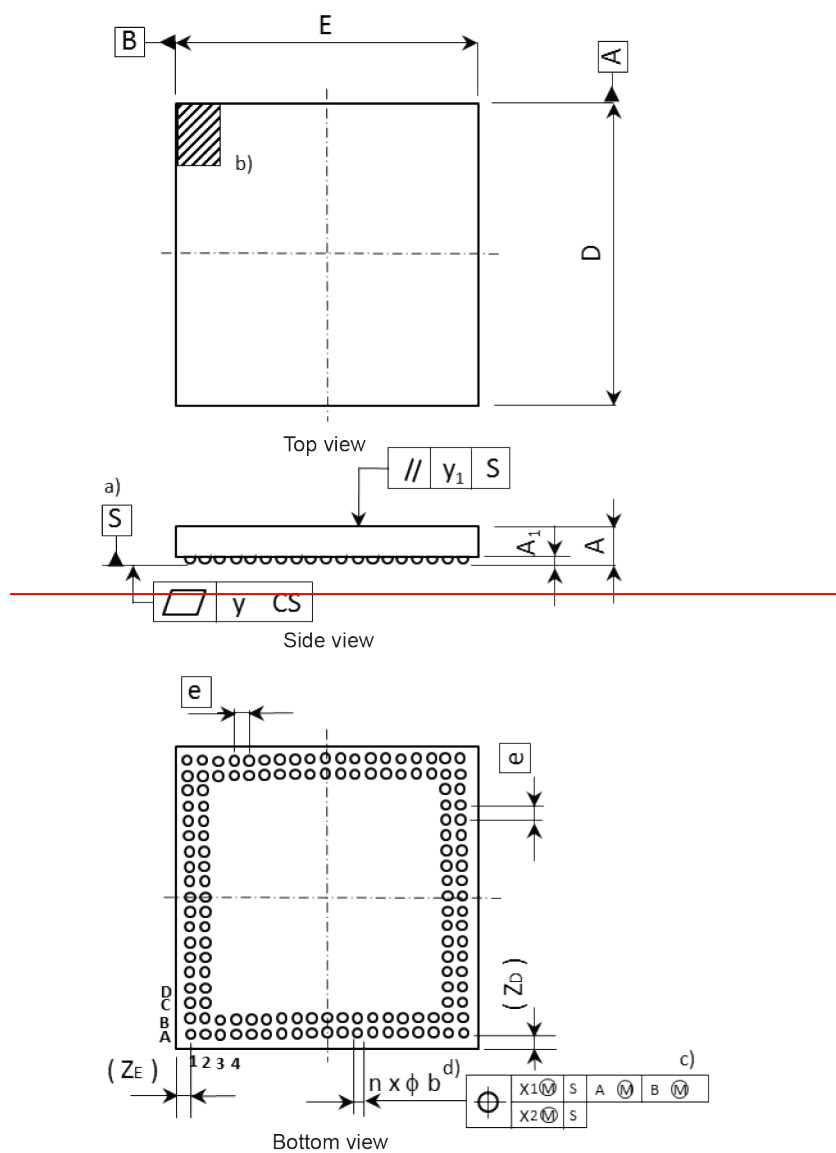
When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C..., AA, AB, etc.; whereas terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, for example A1, B1. The letters I, O, Q, S, X and Z shall not be used for naming the terminal rows.

5 Code of package nominal dimensions

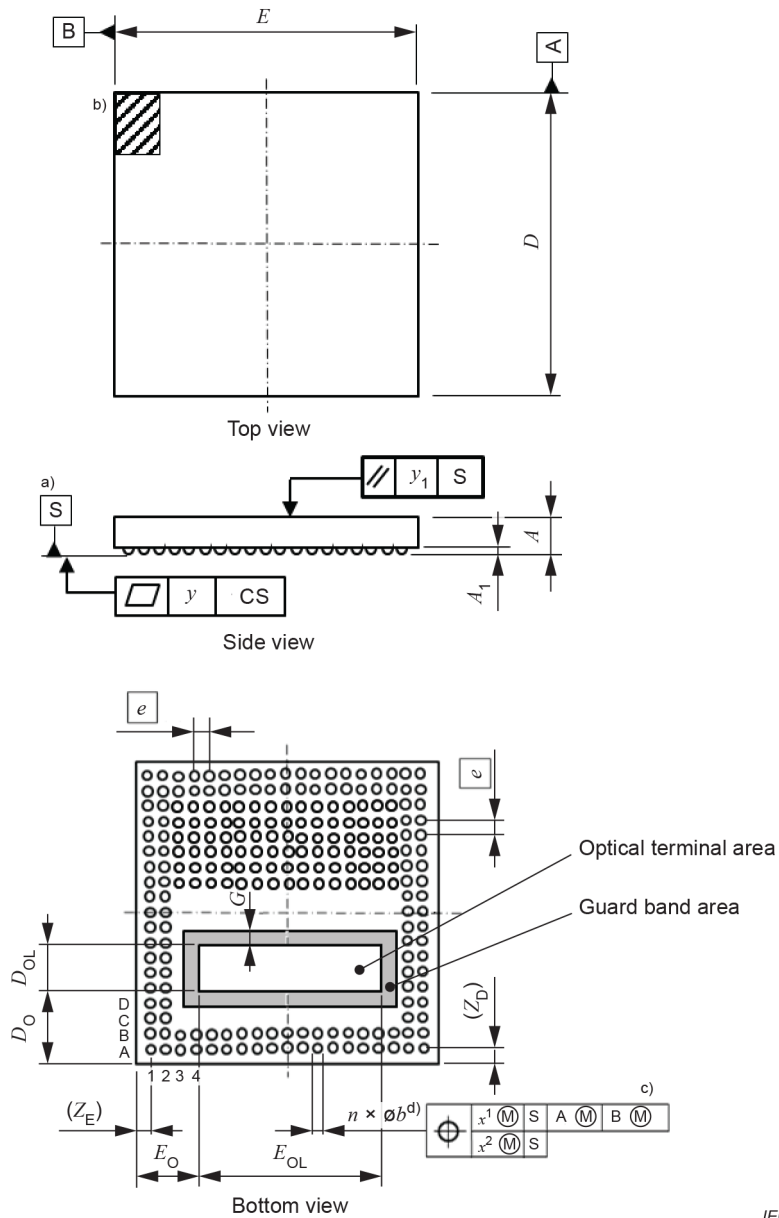
A code of package nominal dimensions is defined as the combination of package length E and width D , which are shown to the second decimal place in millimetres.

6 Symbols and drawings

Figure 1 shows the dimensions of the package and the outline of the electrical interface for S-FBGA and S-FLGA. Figure 1 also shows the dimensions of the optical terminal area and its guard band area. The electrical terminal is freely allocated to the terminal positions defined by the cross points of the row-column grid numbers, as long as its position is outside of the optical terminal guard band area. The optical interface shall be designed within the optical terminal area. Figure 2 and Figure 3 indicate the mechanical gauge drawing and its array of electrical terminal existence area. Figure 2 shows the electrical terminal existing area referred to ~~Datum~~ data S, A and B. Figure 3 shows the electrical terminal existing area referred to datum S.



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NOTE The letter symbols used in the figure are listed and described in Table 1.

- a) Datum S is the seating plane on which a package stays.
- b) The hatched zone is an index-marking area indicating A1 corner.
- c) True positional tolerances of terminals x1 and x2 are applied to all terminals.
- d) The terminal diameter b is the maximum diameter of the ball as measured in a plane parallel to the seating plane.

Figure 1 – S-FBGA and S-FLGA outline